

01\_S3C6410(addr\_data)  
01\_S3C6410(addr\_data)



02\_S3C6410(IO 1)  
02\_S3C6410(IO 1)



03\_S3C6410(IO 2)  
03\_S3C6410(IO 2)



04\_S3C6410(Power)  
04\_S3C6410(Power)



05\_Memory  
05\_Memory

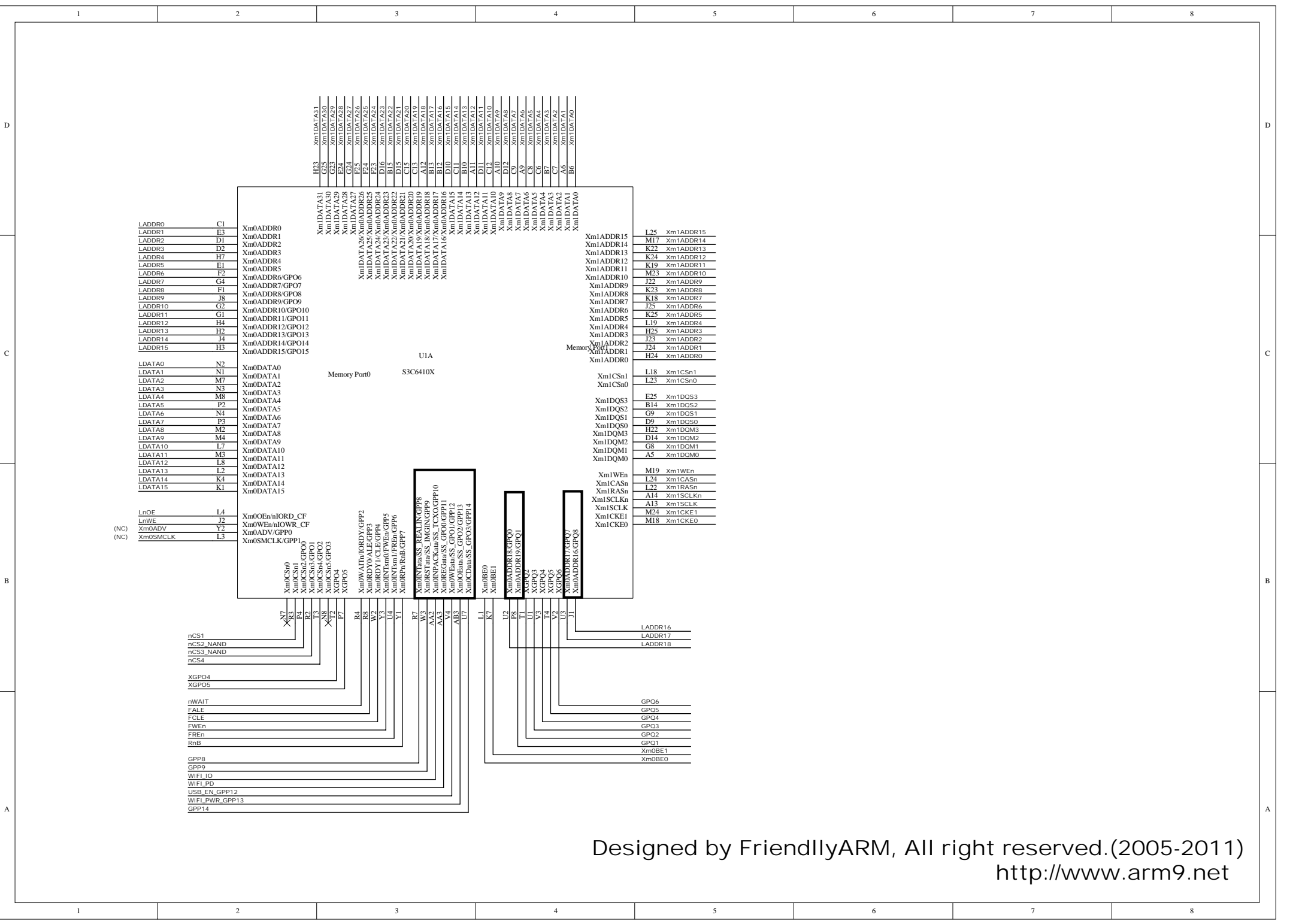


07\_Power  
07\_Power\_etc



Tiny6410-1107

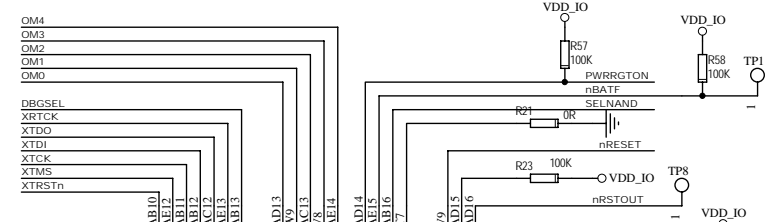
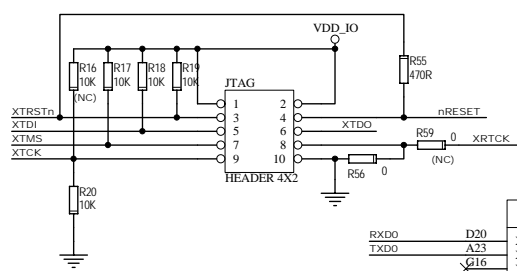
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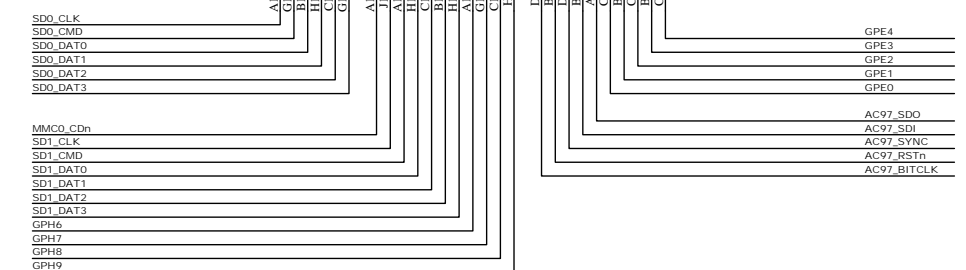
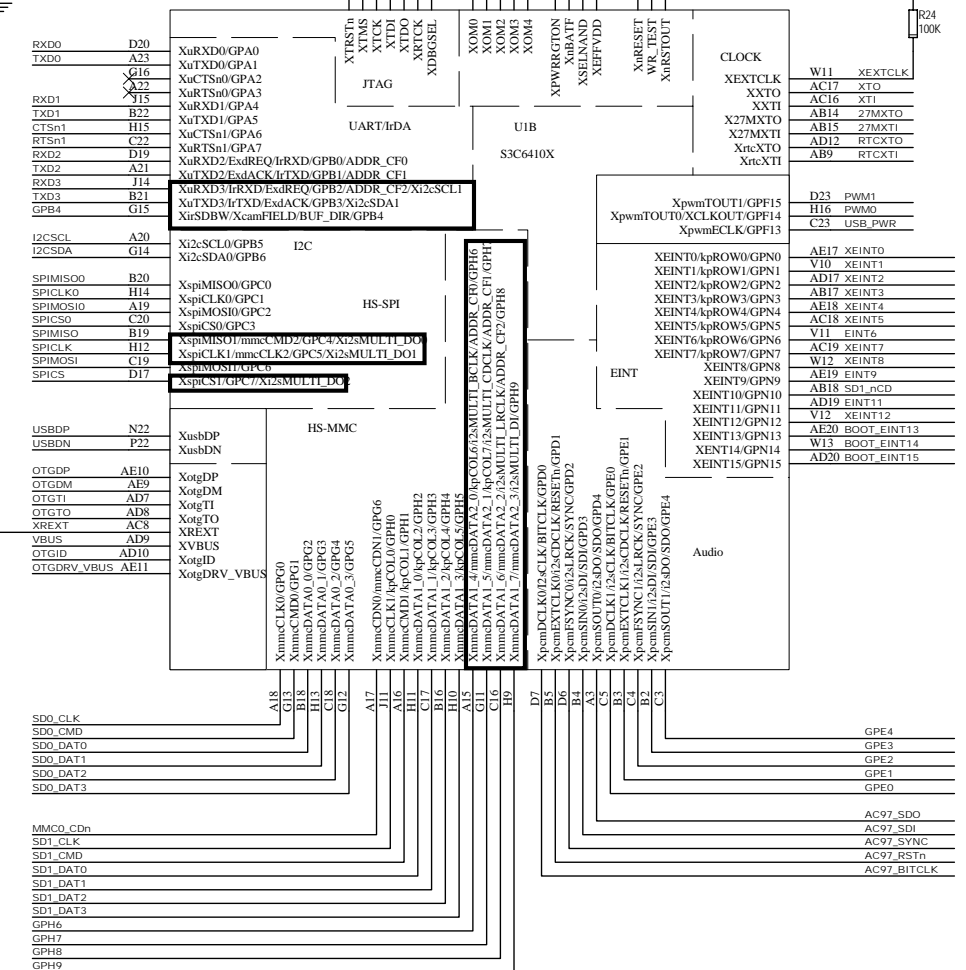
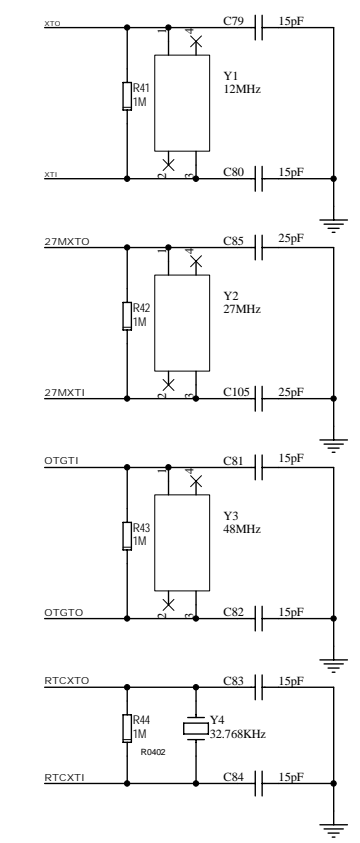
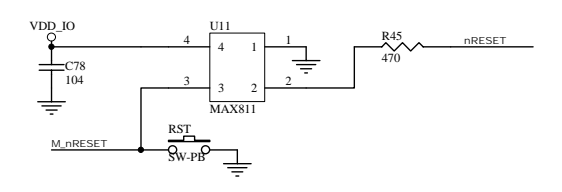
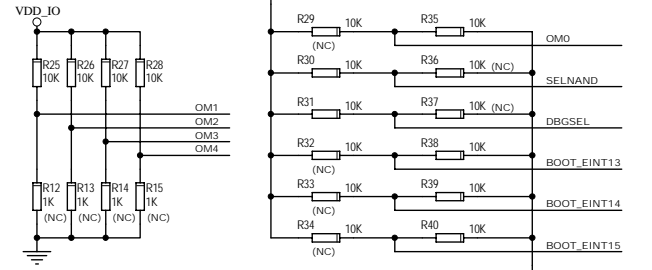
LADDR0	C1	Xm0ADDR0	Xm1DATA31	H23	Xm1DATA31
LADDR1	E3	Xm0ADDR1	Xm1DATA30	G25	Xm1DATA30
LADDR2	D1	Xm0ADDR2	Xm1DATA29	G23	Xm1DATA29
LADDR3	D2	Xm0ADDR3	Xm1DATA28	E24	Xm1DATA28
LADDR4	H7	Xm0ADDR4	Xm1DATA27	G24	Xm1DATA27
LADDR5	E1	Xm0ADDR5	Xm1DATA26	F25	Xm1DATA26
LADDR6	F2	Xm0ADDR6/GPO6	Xm1DATA25	E23	Xm1DATA25
LADDR7	G4	Xm0ADDR7/GPO7	Xm1DATA24	F24	Xm1DATA24
LADDR8	F1	Xm0ADDR8/GPO8	Xm1DATA23	D16	Xm1DATA23
LADDR9	J8	Xm0ADDR9/GPO9	Xm1DATA22	D15	Xm1DATA22
LADDR10	G2	Xm0ADDR10/GPO10	Xm1DATA21	C15	Xm1DATA21
LADDR11	G1	Xm0ADDR11/GPO11	Xm1DATA20	C13	Xm1DATA20
LADDR12	H4	Xm0ADDR12/GPO12	Xm1DATA19	B15	Xm1DATA19
LADDR13	H2	Xm0ADDR13/GPO13	Xm1DATA18	B12	Xm1DATA18
LADDR14	J4	Xm0ADDR14/GPO14	Xm1DATA17	B11	Xm1DATA17
LADDR15	H3	Xm0ADDR15/GPO15	Xm1DATA16	D10	Xm1DATA16
LDATA0	N2	Xm0DATA0	Xm1DATA15	C11	Xm1DATA15
LDATA1	N1	Xm0DATA1	Xm1DATA14	B10	Xm1DATA14
LDATA2	M7	Xm0DATA2	Xm1DATA13	A11	Xm1DATA13
LDATA3	N3	Xm0DATA3	Xm1DATA12	A10	Xm1DATA12
LDATA4	M8	Xm0DATA4	Xm1DATA11	C13	Xm1DATA11
LDATA5	F2	Xm0DATA5	Xm1DATA10	A11	Xm1DATA10
LDATA6	N4	Xm0DATA6	Xm1DATA9	A10	Xm1DATA9
LDATA7	P3	Xm0DATA7	Xm1DATA8	C9	Xm1DATA8
LDATA8	M2	Xm0DATA8	Xm1DATA7	A9	Xm1DATA7
LDATA9	M4	Xm0DATA9	Xm1DATA6	C8	Xm1DATA6
LDATA10	L7	Xm0DATA10	Xm1DATA5	B6	Xm1DATA5
LDATA11	M3	Xm0DATA11	Xm1DATA4	C7	Xm1DATA4
LDATA12	L8	Xm0DATA12	Xm1DATA3	A6	Xm1DATA3
LDATA13	L2	Xm0DATA13	Xm1DATA2	A6	Xm1DATA2
LDATA14	K4	Xm0DATA14	Xm1DATA1	B6	Xm1DATA1
LDATA15	K1	Xm0DATA15	Xm1DATA0	B6	Xm1DATA0
LnOE	L4	Xm0OEEn/IORD_CF	Xm1ADDR15	L25	Xm1ADDR15
LnWE	J2	Xm0WEEn/IOWR_CF	Xm1ADDR14	M17	Xm1ADDR14
Xm0ADV	Y2	Xm0ADV/GPP0	Xm1ADDR13	K22	Xm1ADDR13
Xm0SMCLK	L3	Xm0SMCLK/GPP1	Xm1ADDR12	K24	Xm1ADDR12
Xm0CSn0	XN7	Xm0CSn0	Xm1ADDR11	K19	Xm1ADDR11
Xm0CSn1	XK3	Xm0CSn1	Xm1ADDR10	M23	Xm1ADDR10
Xm0CSn2	P4	Xm0CSn2/GPO0	Xm1ADDR9	J22	Xm1ADDR9
Xm0CSn3	P2	Xm0CSn3/GPO1	Xm1ADDR8	K23	Xm1ADDR8
Xm0CSn4	X12	Xm0CSn4/GPO2	Xm1ADDR7	K18	Xm1ADDR7
Xm0CSn5	X13	Xm0CSn5/GPO3	Xm1ADDR6	J25	Xm1ADDR6
XGPO4	X17	XGPO4	Xm1ADDR5	K25	Xm1ADDR5
XGPO5	P7	XGPO5	Xm1ADDR4	L19	Xm1ADDR4
Xm0WAITn/ORDY/GPP2	R4	Xm0WAITn/ORDY/GPP2	Xm1ADDR3	H25	Xm1ADDR3
Xm0RDY0/ALE/GPP3	W8	Xm0RDY0/ALE/GPP3	Xm1ADDR2	J23	Xm1ADDR2
Xm0RDY1/CLE/GPP4	W5	Xm0RDY1/CLE/GPP4	Xm1ADDR1	J24	Xm1ADDR1
Xm0INTn0/FWEEn/GPP5	Y4	Xm0INTn0/FWEEn/GPP5	Xm1ADDR0	H24	Xm1ADDR0
Xm0INTn1/FWEEn/GPP6	Y1	Xm0INTn1/FWEEn/GPP6	Xm1CSn1	L18	Xm1CSn1
Xm0INTn2/FWEEn/GPP7	Y1	Xm0INTn2/FWEEn/GPP7	Xm1CSn0	L23	Xm1CSn0
Xm0INTn3/SS_REALING/GPP8	R7	Xm0INTn3/SS_REALING/GPP8	Xm1DQS3	E25	Xm1DQS3
Xm0RSTn/SS_IMGIN/GPP9	A3	Xm0RSTn/SS_IMGIN/GPP9	Xm1DQS2	B14	Xm1DQS2
Xm0NPACn/SS_TCXO/GPP10	AA3	Xm0NPACn/SS_TCXO/GPP10	Xm1DQS1	G9	Xm1DQS1
Xm0REGn/SS_GPO0/GPP11	V4	Xm0REGn/SS_GPO0/GPP11	Xm1DQS0	D9	Xm1DQS0
Xm0REGn/SS_GPO1/GPP12	V4	Xm0REGn/SS_GPO1/GPP12	Xm1DQM3	H22	Xm1DQM3
Xm0REGn/SS_GPO2/GPP13	AB3	Xm0REGn/SS_GPO2/GPP13	Xm1DQM2	D14	Xm1DQM2
Xm0REGn/SS_GPO3/GPP14	AB3	Xm0REGn/SS_GPO3/GPP14	Xm1DQM1	G8	Xm1DQM1
Xm0BE0	L1	Xm0BE0	Xm1DQM0	A5	Xm1DQM0
Xm0BE1	K7	Xm0BE1	Xm1WEEn	M19	Xm1WEEn
Xm0ADDR18/GPO0	U2	Xm0ADDR18/GPO0	Xm1CASn	L24	Xm1CASn
Xm0ADDR19/GPO1	P8	Xm0ADDR19/GPO1	Xm1RASn	L22	Xm1RASn
XGPO3	T1	XGPO3	Xm1SCLKa	A14	Xm1SCLKn
XGPO4	U1	XGPO4	Xm1SCLKB	A13	Xm1SCLKB
XGPO5	T3	XGPO5	Xm1CKE1	M24	Xm1CKE1
XGPO6	V2	XGPO6	Xm1CKE0	M18	Xm1CKE0
Xm0ADDR17/GPO0	U3	Xm0ADDR17/GPO0			
Xm0ADDR16/GPO0	J1	Xm0ADDR16/GPO0			
			LADDR16		
			LADDR17		
			LADDR18		
			GPO6		
			GPO5		
			GPO4		
			GPO3		
			GPO2		
			GPO1		
			Xm0BE1		
			Xm0BE0		
nCS1					
nCS2_NAND					
nCS3_NAND					
nCS4					
XGPO4					
XGPO5					
nWAIT					
FALE					
FCLE					
FWEEn					
FREn					
RnB					
GPP8					
GPP9					
WiFi_I0					
WiFi_PD					
USB_EN_GPP12					
WiFi_PWR_GPP13					
GPP14					

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# JTAG



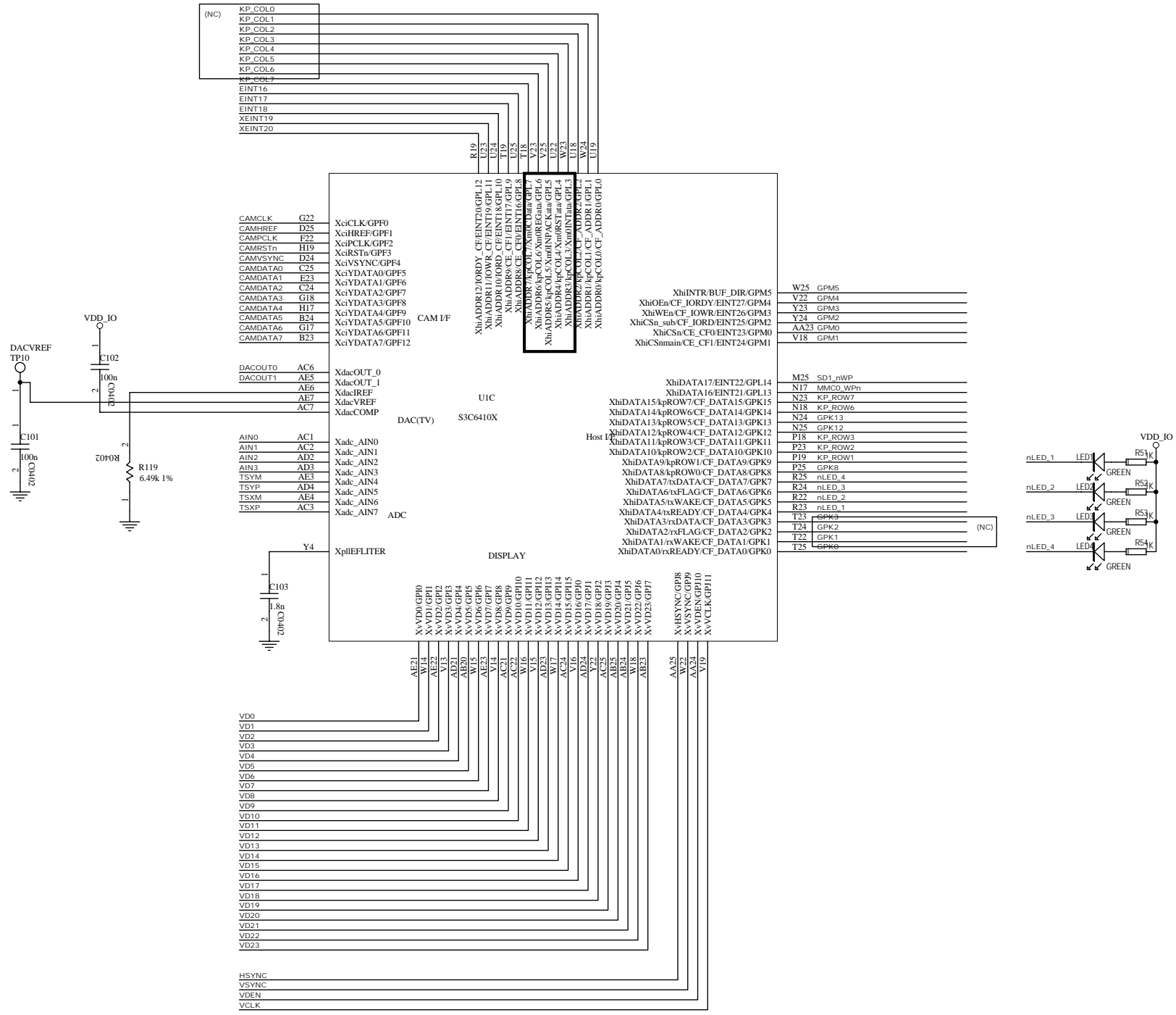
# BOOTSET

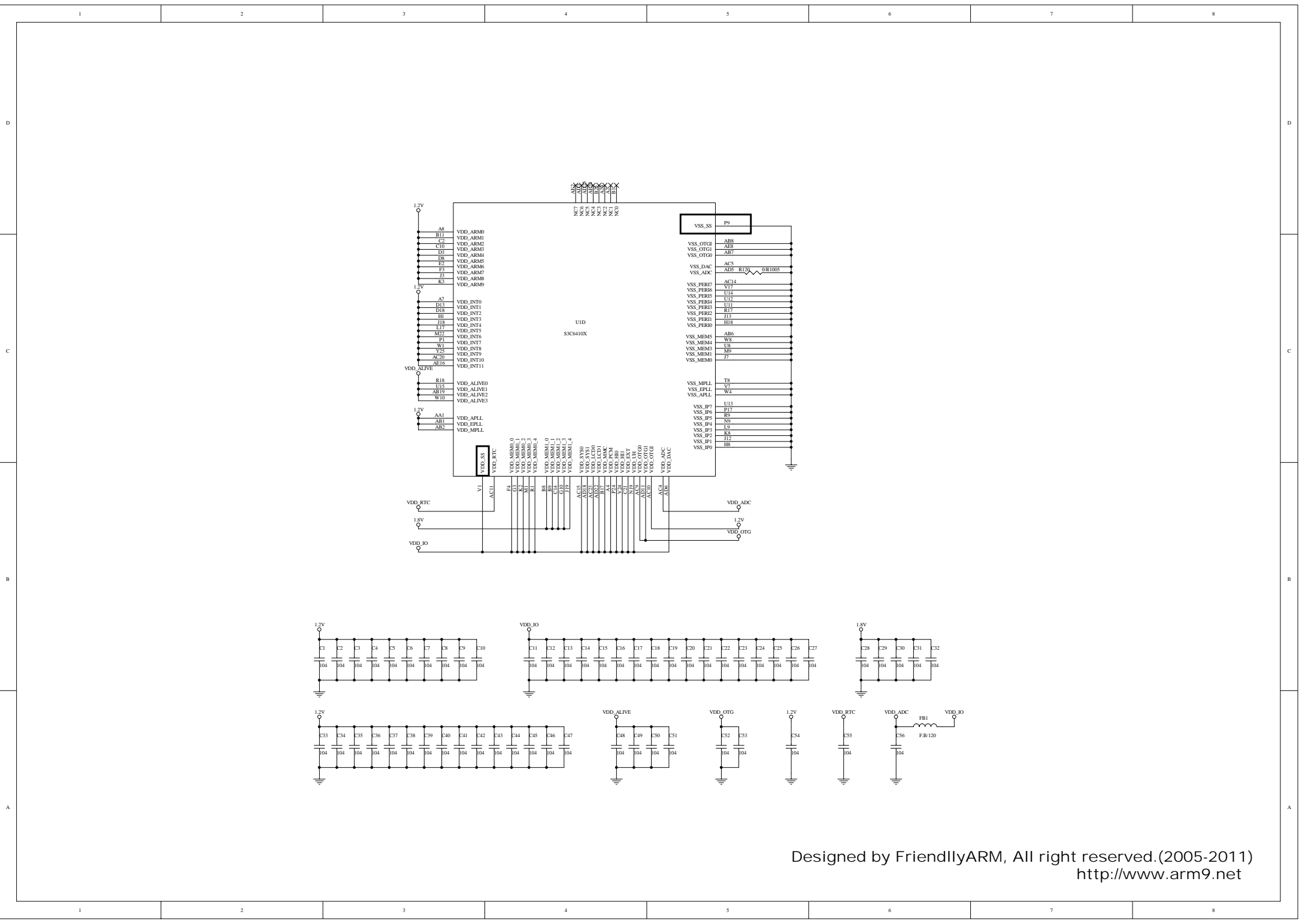


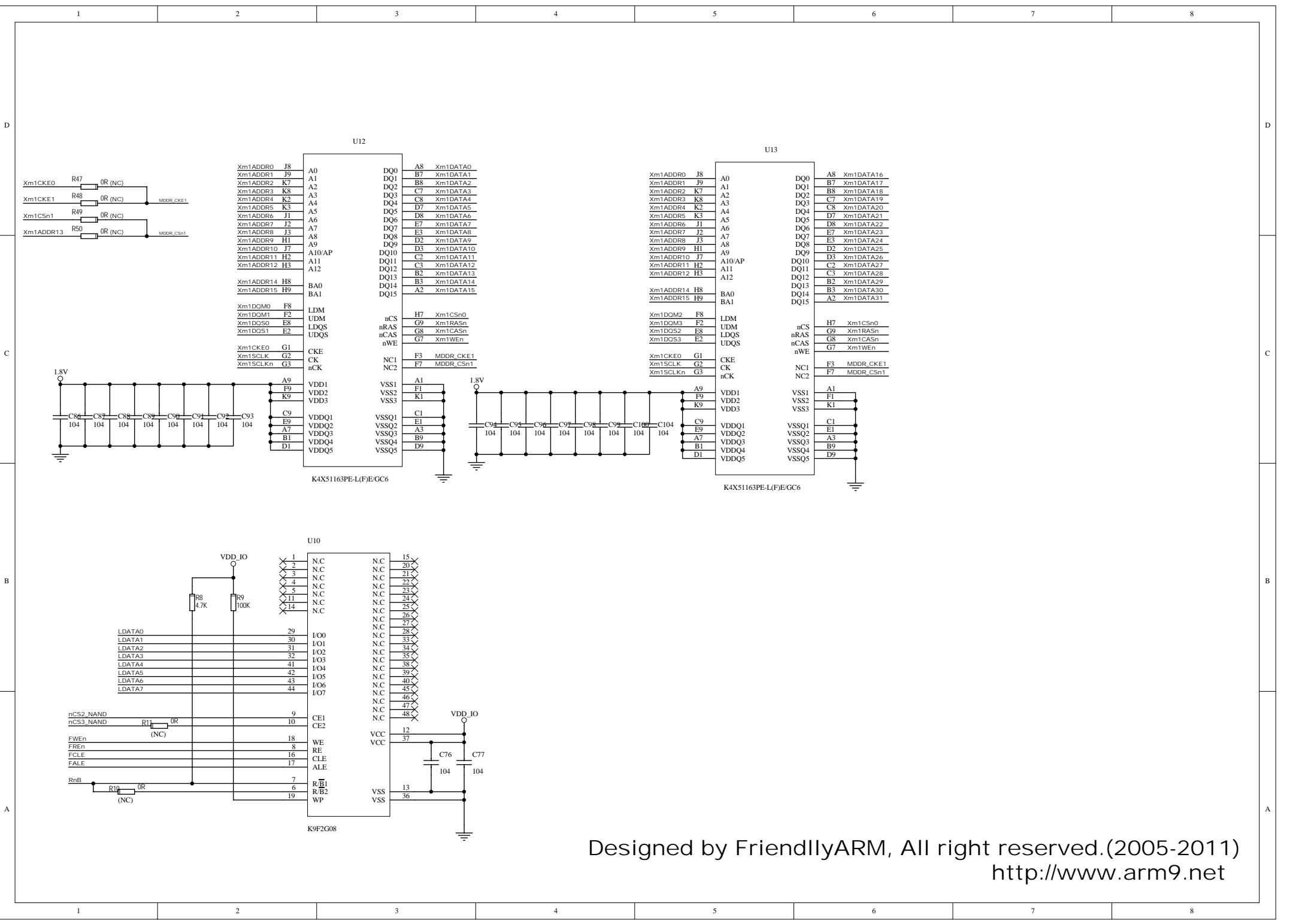
D  
C  
B  
A

D  
C  
B  
A

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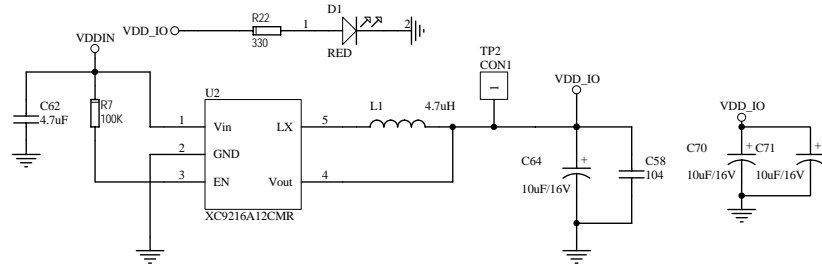




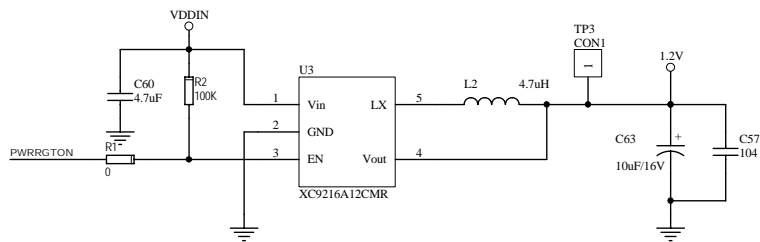


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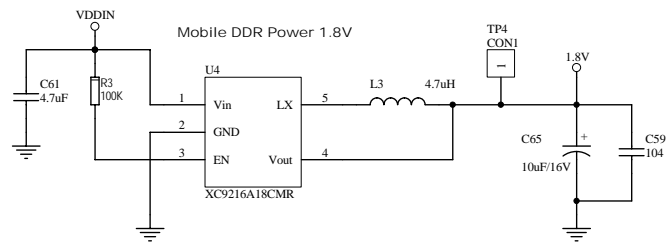
# Power Supply



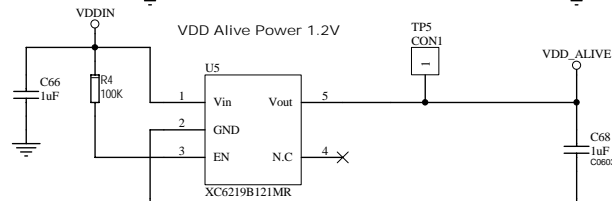
VDD INT Power 1.2V  
(ARM Core, Internal block, MPLL, APLL, EPLL, VDD\_OTGI)



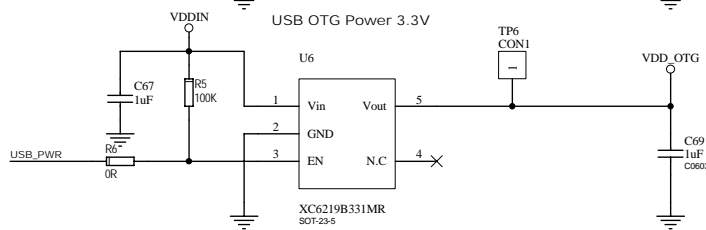
Mobile DDR Power 1.8V



VDD Alive Power 1.2V



USB OTG Power 3.3V



P1		GND	
VDDIN	1	VD22	2
VD23	3	VD20	4
VD21	5	VD18	6
VD19	7	VD14	8
VD15	9	VD12	10
VD13	11	VD10	12
VD11	13	VD6	14
VD7	15	VD4	16
VD5	17	VD2	18
VDEN	19	PWM1	20
VSYN	21	HSYN	22
VCLK	23	GPEQ	24
VBUS	25	OTGDRV_VBUS	26
OTGID	27	XEINT8	28
OTGDM	29	USBDN	30
OTGDP	31	USBDP	32
TSXP	33	TSXM	34
TSYP	35	TSYM	36
AIN0	37	AIN1	38
WiFi_IO	39	WiFi_PD	40
SD1_CLK	41	SD1_CMD	42
SD1_nCD	43	SD1_nWP	44
SD1_DAT0	45	SD1_DAT1	46
SD1_DAT2	47	SD1_DAT3	48
DACOUT0	49	PWM0	50
XEINT0	51	XEINT1	52
XEINT2	53	XEINT3	54
XEINT4	55	XEINT5	56
XEINT19	57	XEINT20	58
	59		60

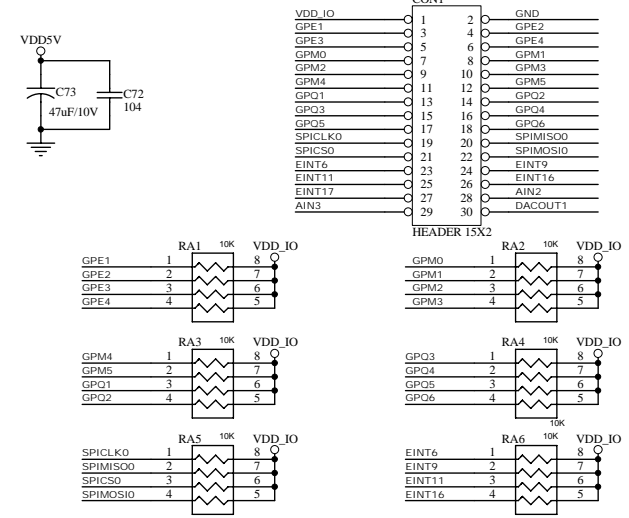
HEADER 30X2

P2		OM3		OM4	
M_nRESET	1	VDD_RTC	3	CTSn1	5
RTSn1	2	RXD0	6	RXD1	7
TXD0	3	RXD2	8	RXD3	9
TXD1	4	SPIMISO	10	SPIC3	11
TXD2	5	SPIC5	12	I2CSDA	13
TXD3	6	SDO_CMD	14	SDO_DATA	15
SPIMOSI	7	MMCO_WPn	16	SDO_DATA3	17
SPIC3	8	SDO_CMD	18	AC97_RSTn	19
I2CSCL	9	AC97_SYNC	20	AC97_SDO	21
SDO_CMD	10	XEINT12	22	LADDR1	23
MMCO_WPn	11	LADDR2	24	LADDR3	25
SDO_DATA	12	XEINT7	26	XEINT17	27
SDO_DATA3	13	nWAIT	28	nRESET	29
AC97_RSTn	14	LnWE	30	LnOE	31
AC97_SYNC	15	LDATA0	32	LDATA1	33
AC97_SDO	16	LDATA2	34	LDATA3	35
LADDR1	17	LDATA4	36	LDATA5	37
LADDR2	18	LDATA6	38	LDATA7	39
LADDR3	19	LDATA8	40	LDATA9	41
XEINT12	20	LDATA10	42	LDATA11	43
XEINT7	21	LDATA12	44	LDATA13	45
nWAIT	22	LDATA14	46	LDATA15	47
nRESET	23				
LnWE	24				
LnOE	25				
LDATA0	26				
LDATA1	27				
LDATA2	28				
LDATA3	29				
LDATA4	30				
LDATA5	31				
LDATA6	32				
LDATA7	33				
LDATA8	34				
LDATA9	35				
LDATA10	36				
LDATA11	37				
LDATA12	38				
LDATA13	39				
LDATA14	40				
LDATA15	41				

HEADER 30X2

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## GPIO(兼容Mini6410的GPIO口CON6)



## GPIO2(包含CMOS, 中断等)

