Block Diagram

《iCore REV.0》

REV	DATE	PAGES	DESCRIPTION
0.0.0	09/05/2012	ALL	Created

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Engineer:

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Title: iCore

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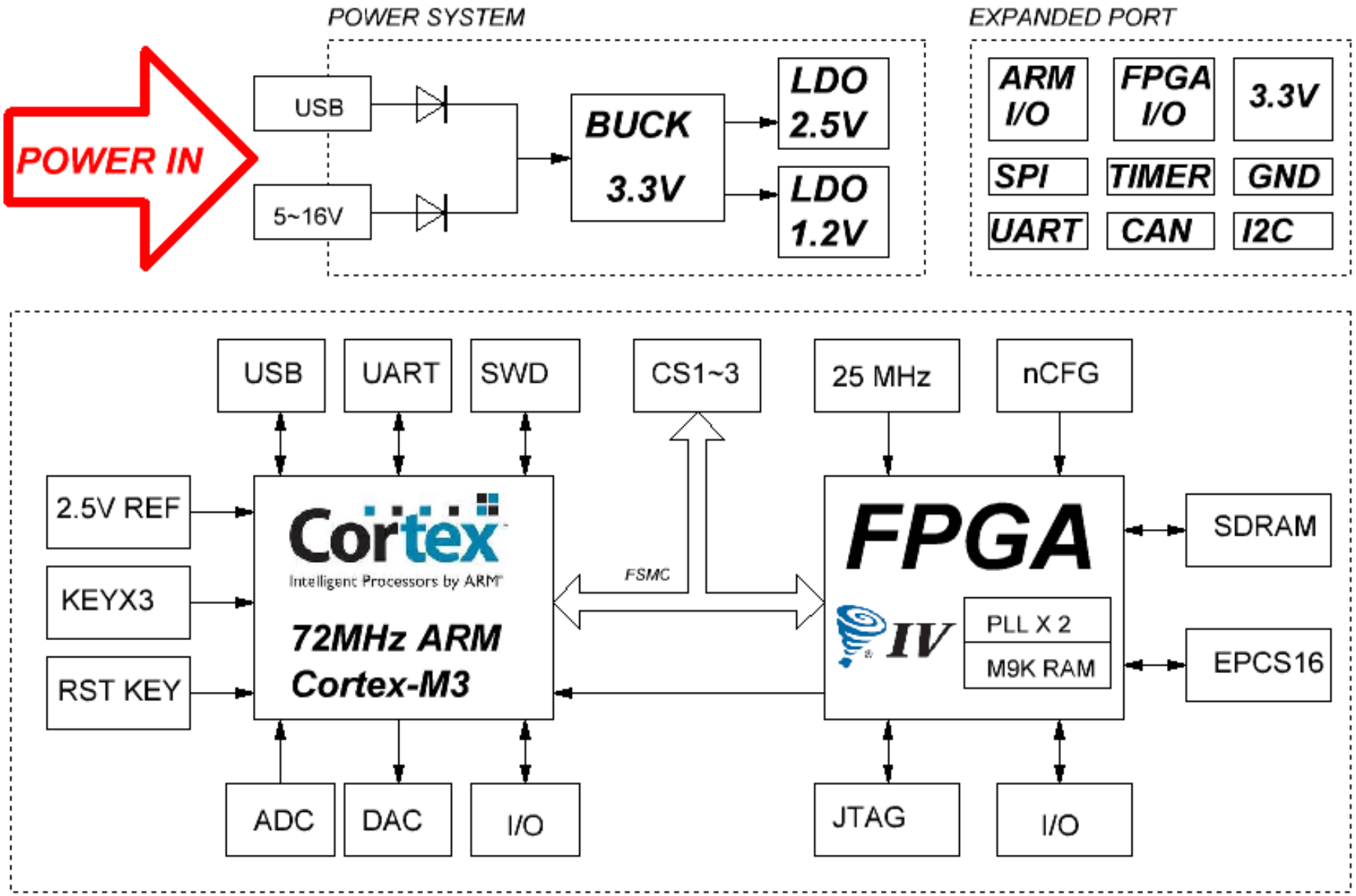

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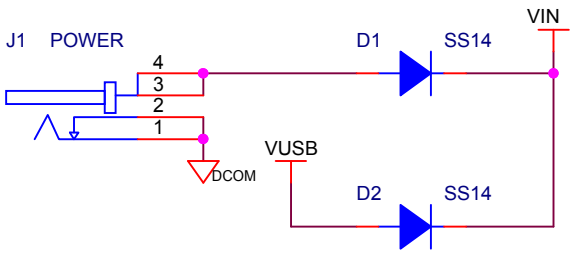
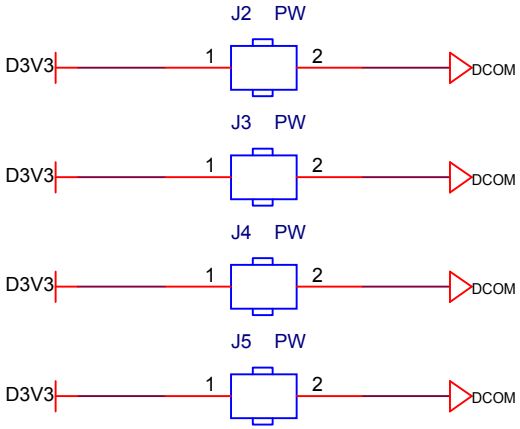
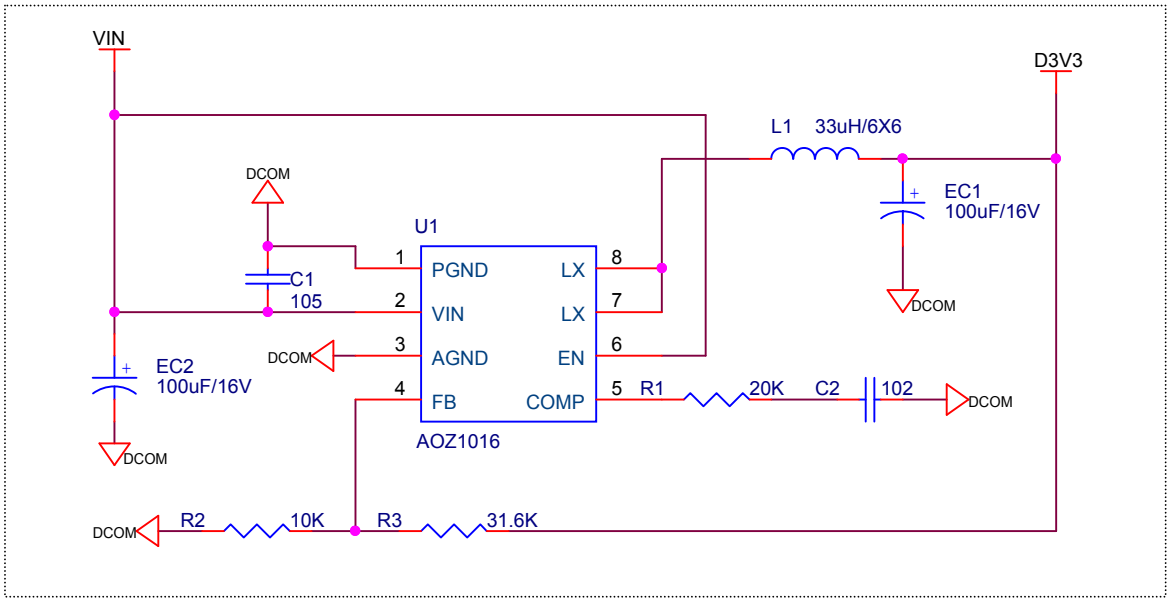
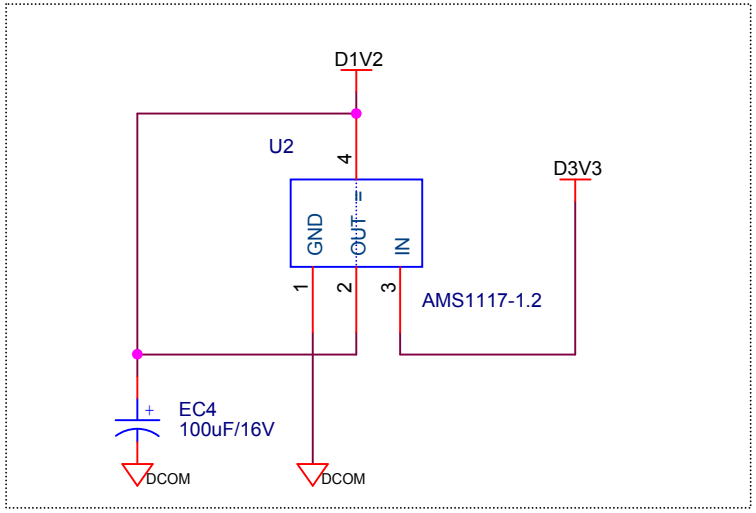




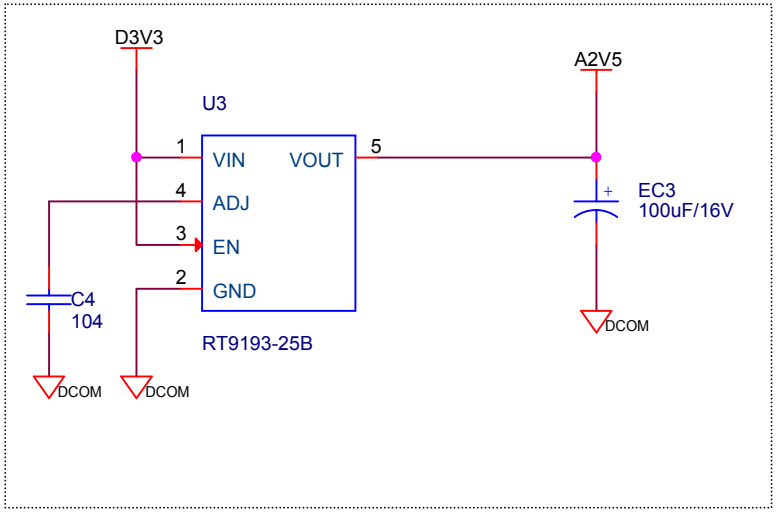
3.3V (BUCK)



1.2V (LDO)



2.5V (LDO)



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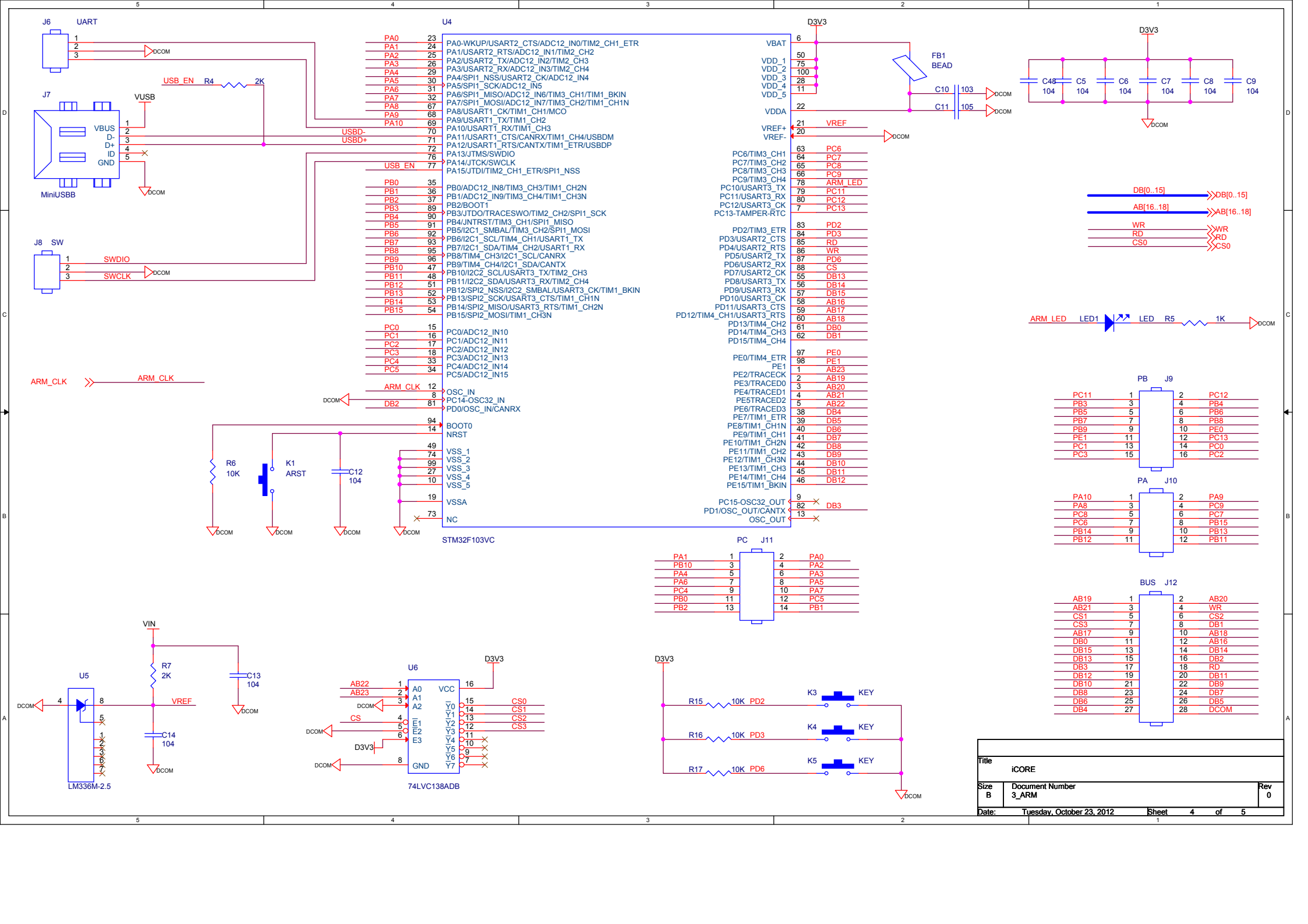
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J7 MiniUSBB
J8 SW
U4 STM32F103VC
U5 LM336M-2.5
U6 74LVC138ADB
PB J9
PA J10
BUS J12
PC J11
K1 ARST
FB1 BEAD
LED1
K3 KEY
K4 KEY
K5 KEY
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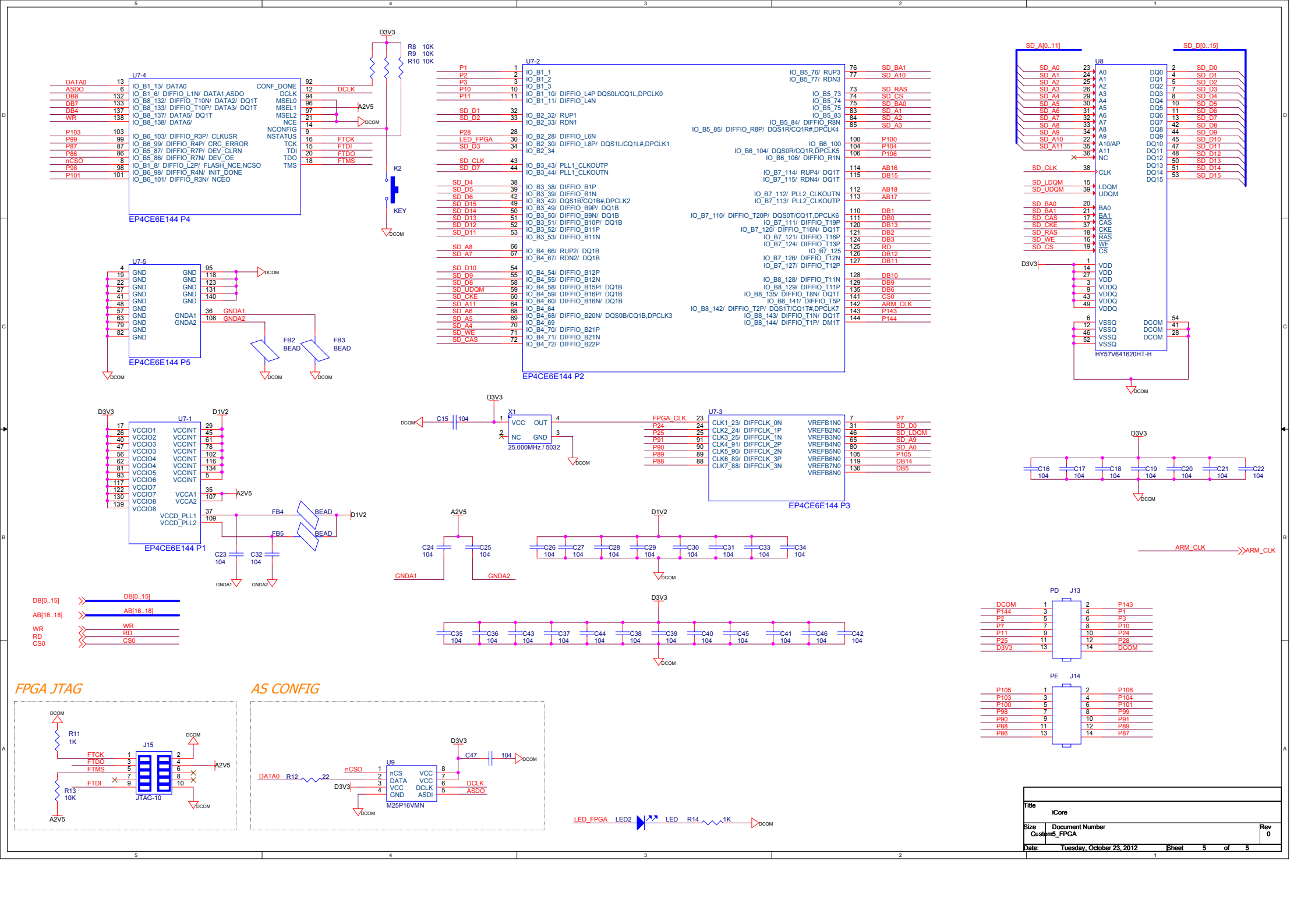
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U7-5
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U7-2
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HY57V641620HT-H
U7-1
EP4CE6E144 P1
U7-3
EP4CE6E144 P3
X1
25.000MHz / 5032
PD J13
PE J14
FPGA JTAG
AS CONFIG
JTAG-10
M25P16VMN
Title
iCore
Size Custom5_FPGA
Document Number
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