

# Design Considerations for In-Circuit Programming

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This chapter presents signal requirements for in-circuit programming of the MSP430.

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### 3.1 Signal Connections for In-System Programming and Debugging, MSP-FET430PIF, MSP-FET430UIF, GANG430, PRGS430

With the proper connections, you can use the C-SPY debugger and an FET hardware JTAG interface such as the MSP-FETP430IF and MSP-FET430UIF to program and debug code on your own target board. In addition, the connections will also support the GANG430 or PRGS430 production programmers, thus providing an easy way to program prototype boards, if desired.

Figure 3-1 shows the connections between the 14-pin FET Interface module connector and the target device required to support in-system programming and debugging using C-SPY for 4-wire JTAG communication. Figure 3-2 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire). While 4-wire JTAG mode is generally supported on all MSP430 devices, 2-wire JTAG mode is available on selected devices only. Refer to Table 2-1 above for information on which interfacing method can be used on which device.

The connections for the FET Interface module and the GANG430 or PRGS430 are identical. Both the FET Interface module and GANG430 can supply  $V_{CC}$  to your target board (via pin 2). In addition, the FET Interface module and GANG430 have a  $V_{CC}$ -sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The  $V_{CC}$ -sense feature senses the local  $V_{CC}$  (present on the target board, i.e., a battery or other local power supply) and adjusts the output signals accordingly. If the target board is to be powered by a local  $V_{CC}$ , then the connection to pin 4 on the JTAG should be made, and not the connection to pin 2. This utilizes the  $V_{CC}$ -sense feature and prevents any contention that might occur if the local on-board  $V_{CC}$  were connected to the  $V_{CC}$  supplied from the FET Interface module or the GANG430. If the  $V_{CC}$ -sense feature is not necessary (i.e., the target board is to be powered from the FET Interface module or the GANG430) the  $V_{CC}$  connection is made to pin 2 on the JTAG header and no connection is made to pin 4. Figure 3-1 and Figure 3-2 show a jumper block which supports both scenarios of supplying  $V_{CC}$  to the target board. If this flexibility is not required, the desired  $V_{CC}$  connections may be hard-wired eliminating the jumper block. Pins 2 and 4 must not be connected simultaneously.

Note that in 4-Wire JTAG communication mode (Figure 3-1), the connection of the target RST signal to the JTAG connector is optional and not required. The MSP430 development tools and device programmers perform a target reset through issuing a JTAG command to gain control over the device. However, in the case this should be unsuccessful, the RST signal of the JTAG connector may be used by the development tool or device programmer as an additional way to assert a device reset.

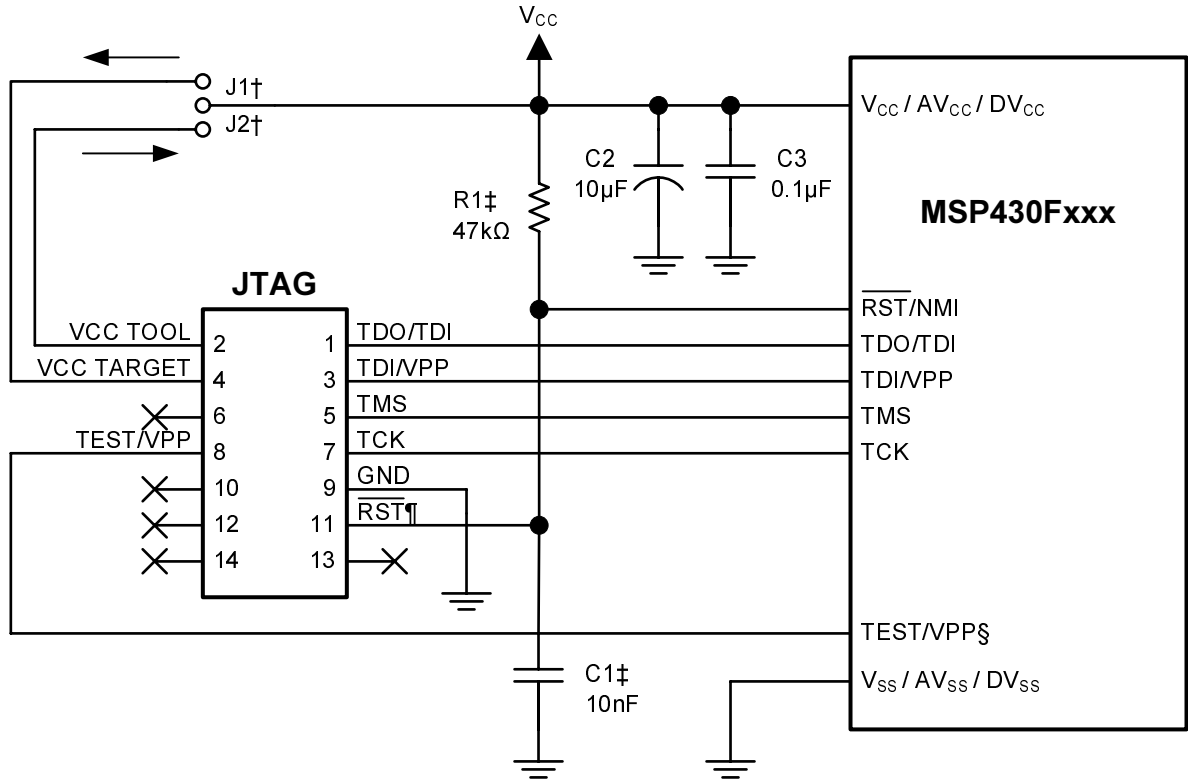


Figure 3-1. Signal Connections for 4-Wire JTAG Communication

- † Make either connection J1 to power target from the debug/programming adapter OR connection J2 in case a local target power supply is used.
- ‡ The RST/NMI pin R1/C1 configuration is device family dependent. Refer to the respective MSP430 Family User's Guide for the recommended configuration.
- § The TEST/VPP pin is only available on MSP430 family members with multiplexed JTAG pins. Refer to the device data sheet to see if this pin is available.
- ¶ The connection to the JTAG connector RST pin is optional and not required for device programming or debugging.

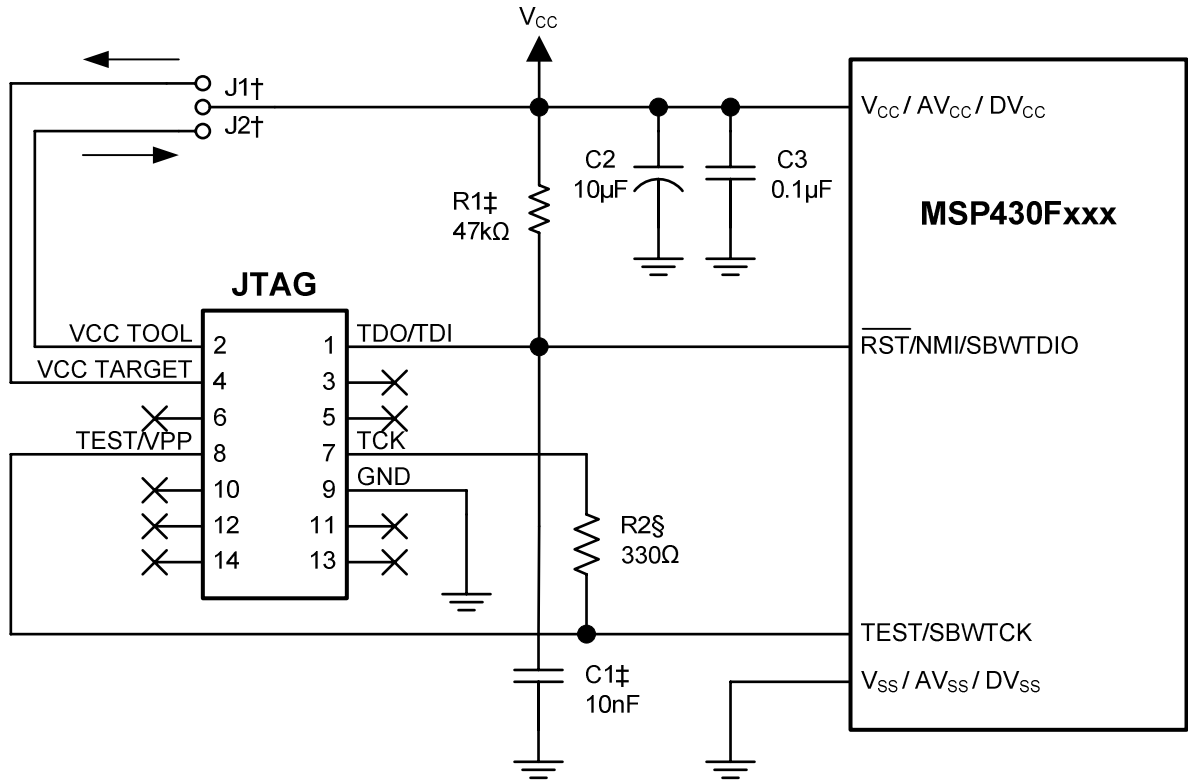


Figure 3-2. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

- † Make either connection J1 to power target from the debug/programming adapter OR connection J2 in case a local target power supply is used.
- ‡ The RST pin R1/C1 configuration is device family dependent. Refer to the respective MSP430 Family User's Guide for the recommended configuration. Note that the device RST/NMI/SBWTIO pin is used in 2-wire mode for bi-directional communication with the device during JTAG access and that increased capacitance (C1) may affect the ability to establish a connection with the device.
- § R2 is used to protect the JTAG debug interface TCK signal against the JTAG security fuse blow voltage that is supplied by the TEST/VPP pin during the fuse blow process. In the case that fuse blow functionality is not needed, R2 is not required (becomes 0 $\Omega$ ) and the connection TEST/VPP must not be made.

### 3.2 External Power

The PC parallel port can only source a limited amount of current. Owing to the ultra low power capability of the MSP430, a stand-alone FET does not exceed the available current. However, if additional circuitry is added to the tool, this current limit could be exceeded. In this case, external power can be supplied to the tool via connections provided on the MSP-FET430X110 and the Target Socket modules. Refer to the schematics and pictorials of the MSP-FET430X110 and the Target Socket modules presented in 38) to locate the external power connectors.

The MSP-FET430UIF can supply targets with up to 100mA through pin 2 of the 14-pin connector.  $V_{CC}$  for the target can be selected between 1.8V and 5.0V in steps of 0.1V. Alternatively the target can be supplied externally. In this case, the external voltage should be connected to pin 4 of the 14-pin connector. The MSP-FET430UIF then adjusts the level of

the JTAG signals to external  $V_{CC}$  automatically. Only pin 2 (MSP-FET430UIF supplies target) OR pin 4 (target is externally supplied) must be connected, not both at the same time.

When an MSP-FET430X110 is powered from an external supply, an on-board device regulates the external voltage to the level required by the MSP430.

When a Target Socket module is powered from an external supply, the external supply powers the device on the Target Socket module and any user circuitry connected to the Target Socket module, and the FET Interface module continues to be powered from the PC via the parallel port. If the externally supplied voltage differs from that of the FET Interface module, the Target Socket module must be modified so that the externally supplied voltage is routed to the FET Interface module (so that it may adjust its output voltage levels accordingly). Again, refer to the Target Socket module schematics in 38).

### 3.3 Bootstrap Loader

The JTAG pins provide access to the Flash memory of the MSP430Fxxx devices. On some devices, these pins are shared with the device port pins, and this sharing of pins can complicate a design (or it may simply not be possible to do so). As an alternative to using the JTAG pins, most MSP430Fxxx devices contain a program (a “Bootstrap Loader”) that permits the Flash memory to be erased and programmed simply, using a reduced set of signals. Application Notes SLAA089 and SLAA096 fully describe this interface. TI does not produce a BSL tool. However, customers can easily develop their own BSL tools using the information in the Application Notes, or BSL tools can be purchased from 3<sup>rd</sup> parties. Refer to the MSP430 web site for the Application Notes and a list of MSP430 3<sup>rd</sup> party tool developers.

Texas Instruments suggests that MSP430Fxxx customers design their circuits with the BSL in mind (i.e., we suggest providing access to these signals, e.g. via a header).

Refer to FAQ, Hardware #9) for a second alternative to sharing the JTAG and port pins.

The BSL tool requires the following device signals:

- RST/NMI
- TEST†
- TCK†
- GND
- VCC
- P1.1
- P2.2 or P1.0‡

† If present on device.

‡ '1xx / '2xx devices use pins P1.1 and P2.2 for the BSL. '4xx devices use pins P1.0 and P1.1 for the BSL.