NAND Flash with LP-DRAM
137-Ball Multiple-Chip Package (MCP)

MT29CxGxxMAxxxJA

Current Production Part Numbers: Table 1 on page 2

Features

- All-Micron® NAND Flash and LP-DRAM components
- RoHS compliant, "green" package
- Separate NAND Flash and LP-DRAM interfaces
- Space-saving multi-chip package
- Low-voltage operation (1.70–1.95V)
- Industrial temperature range: –40C° to +85C°

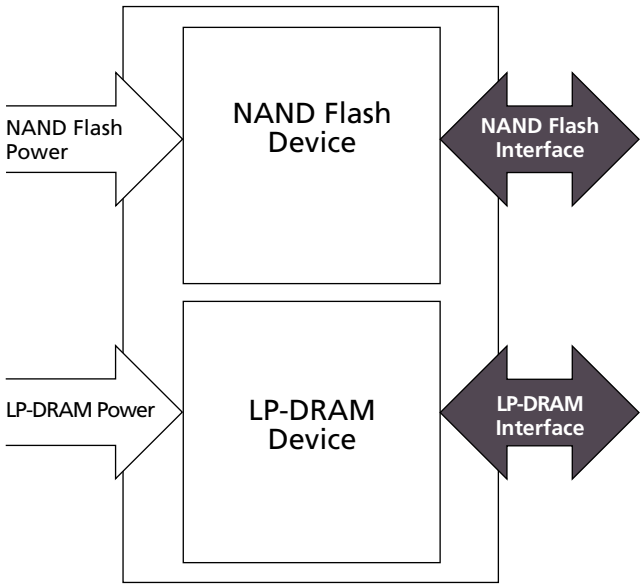
NAND Flash-Specific Features

- Organization:
  - Page size:
    x8: 2,112 bytes (2,048 + 64 bytes)
    x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size:
    1Gb: 1,024 blocks
    2Gb: 2,048 blocks
    4Gb: 4,096 blocks
    8Gb: 8,192 blocks

LP-DRAM-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- STATUS REGISTER READ (SRR) supported[2]

Figure 1: MCP Block Diagram



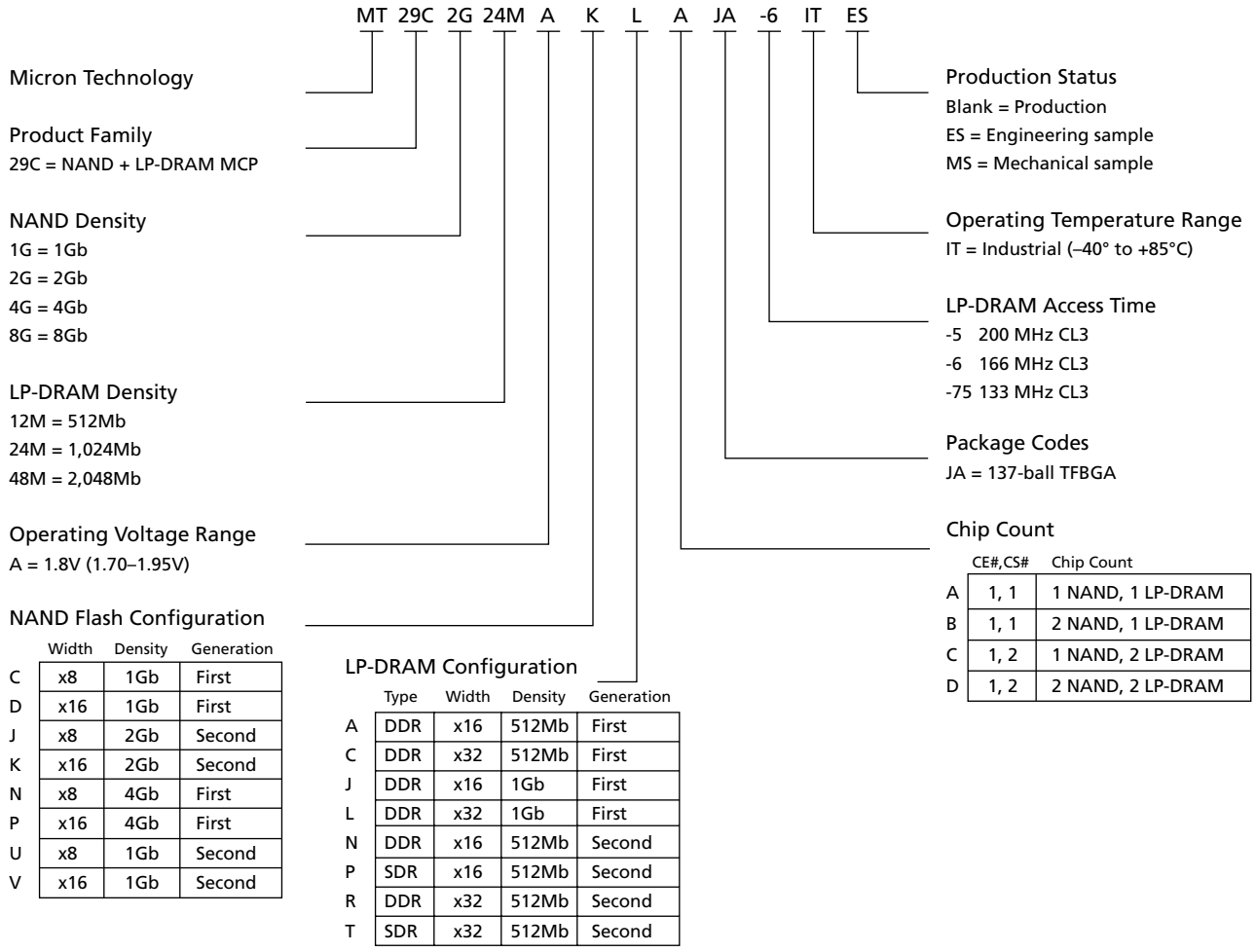
Options	Marking
• LP-DRAM	
200 MHz CL3[3]	-5
166 MHz CL3	-6
133 MHz CL3	-75

Notes: 1. For part numbering and physical part markings, see Figure 2 and Table 1 on page 2.
2. Contact factory for remapped SRR output.
3. CL = CAS (READ) latency.

Part Numbering

Micron NAND Flash and LP-DRAM devices are available in several different configurations and densities (see Figure 2).

Figure 2: 137-Ball Marketing Part Number Example



Note: Not all possible combinations are available. Contact factory for availability.

Table 1: Production Part Numbers for 137-Ball MCP Package

Production Marketing Part Numbers	NAND Flash Product	Mobile SDRAM Product	Physical Part Marking
MT29C1G24MADLAJA-6 IT	MT29F1G16ABBHC-ET	MT46H32M32LFCM-6 IT	JW181
MT29C1G24MADLAJA-75 IT	MT29F1G16ABBHC-ET	MT46H32M32LFCM-75 IT	JW182
MT29C2G24MAKLAJA-6 IT	MT29F2G16ABDHC-ET	MT46H32M32LFCM-6 IT	JW190
MT29C2G24MAKLAJA-75 IT	MT29F2G16ABDHC-ET	MT46H32M32LFCM-75 IT	JW191
MT29C4G24MAPLAJA-6 IT	MT29F4G16ABCHC-ET	MT46H32M32LFCM-6 IT	JW215
MT29C4G24MAPLAJA-75 IT	MT29F4G16ABCHC-ET	MT46H32M32LFCM-75 IT	JW212
MT29C4G48MAPLCJA-6 IT	MT29F4G16ABCHC-ET	MT46H32M32LFCM-6 IT	JW258
MT29C4G48MAPLCJA-75 IT	MT29F4G16ABCHC-ET	MT46H32M32LFCM-75 IT	JW257

MCP General Description

The Micron® multiple-chip package (MCP) family of products includes both NAND Flash and LP-DRAM devices, in a single MCP. These products target applications with low-power, high-performance, and minimal package footprint design requirements. The NAND Flash and LP-DRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and LP-DRAM devices are packaged with separate interfaces (no shared address, control, data, or power pins). This bus architecture supports an optimized interface to processors with separate NAND Flash and LP-DRAM buses. The NAND Flash and LP-DRAM devices have separate core power connections and share a common ground (i.e., V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and LP-DRAM functionality, without concern for device interaction. Operational characteristics for the NAND Flash and LP-DRAM devices are found in the standard Micron data sheets for each of the discrete devices.

For device specifications and complete Micron NAND Flash features documentation, please refer to the component data sheet at www.micron.com/products/nand or contact your local Micron sales office.

For device specifications and complete LP-DRAM features documentation, please refer to the component data sheet at www.micron.com/products/mobiledram, or contact your local Micron sales office.

Figure 3: Ball Assignment: 137-Ball TFBGA (LPDDR-SDRAM)

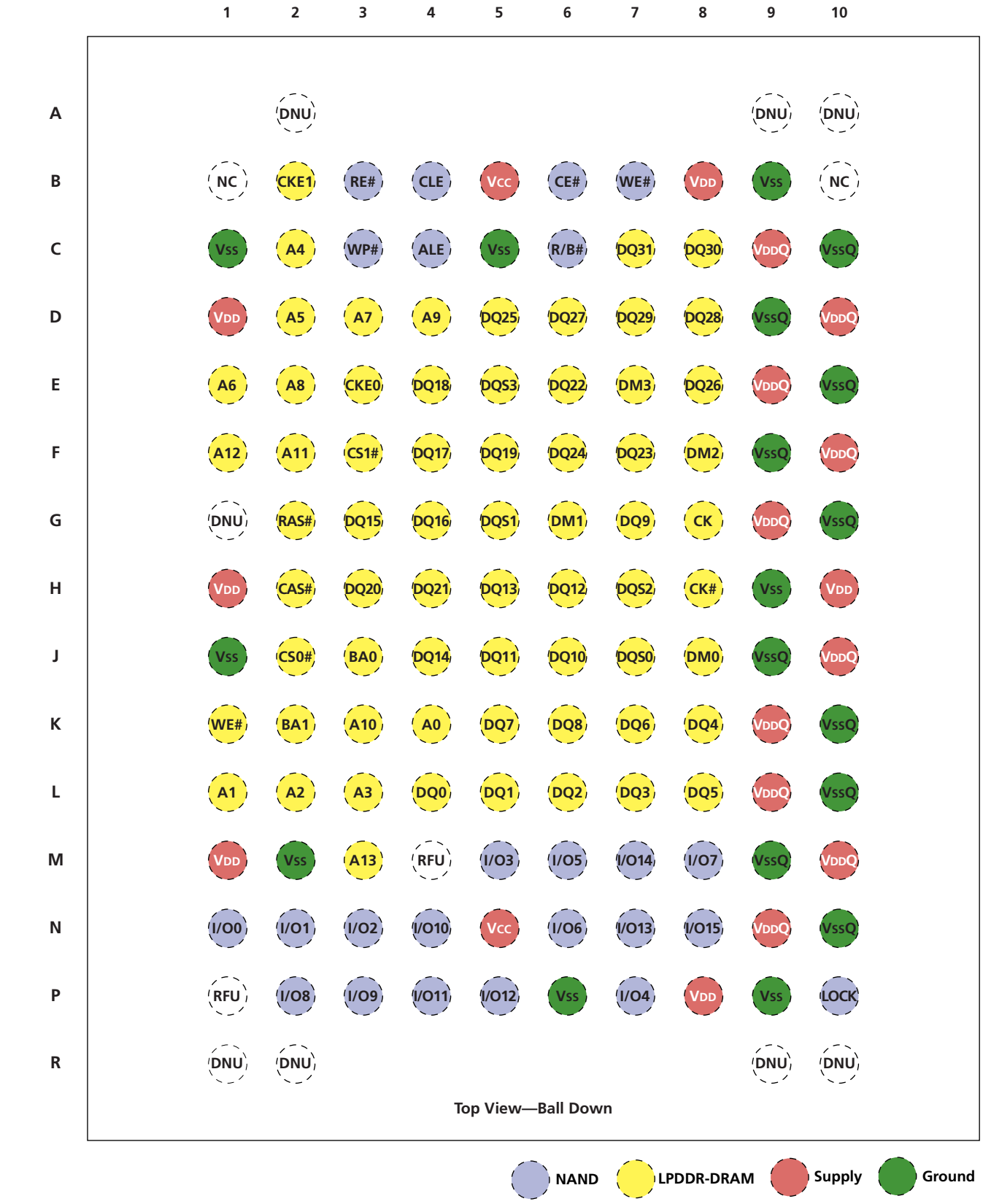


Figure 4: Ball Assignment: 137-Ball TFBGA (LP-SDRAM)

Ball Descriptions

Table 2: NAND Flash Ball Assignments

137-Ball MCP				
NAND Flash x8	**NAND Flash x16**	**Symbol**	**Type**	**Description**
C4	C4	ALE	Input	Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.
B6	B6	CE#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device.
B4	B4	CLE	Input	Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.
P10	P10	LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to VSS during power-up, or leave it unconnected (internal pull-down).
B3	B3	RE#	Input	Read enable: Gates information from the NAND Flash device to the host system.
B7	B7	WE#	Input	Write enable: Gates information from the host system to the NAND Flash device.
C3	C3	WP#	Input	Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.
M8, N6, M6, P7, M5, N3, N2, N1	N8, M7, N7, P5, P4, N4, P3, P2, M8, N6, M6, P7, M5, N3, N2, N1	I/O[7:0] (x8) I/O[15:0] (x16)	Input/ output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs. I/O[15:8] are RFU[1] for NAND x8 devices.
C6	C6	R/B#	Output	Ready/busy: Open drain, active LOW output that indicates when an internal operation is in progress.
B5, N5	B5, N5	VCC	Supply	VCC: NAND Flash power supply.

Notes: 1. Balls marked "RFU" may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 3: LP-DRAM Ball Assignments for LPDDR-SDRAM

137-Ball MCP				
LPDDR-SDRAM x16	**LPDDR-SDRAM x32**	**Symbol**	**Type**	**Description**
M3, F1, F2, K3, D4, E2, D3, E1, D2, C2, L3, L2, L1, K4	F1, F2, K3, D4, E2, D3, E1, D2, C2, L3, L2, L1, K4	A[13:0] (x16) A[12:0] (x32]	Input	Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR-SDRAM address is determined by density and configuration. Consult the LPDDR-SDRAM product datasheet for the maximum address for a given density and configuration. Unused address pins become "RFU.[1]"
J3, K2	J3, K2	BA0, BA1	Input	Bank address inputs: Specifies one of the four banks.
H2	H2	CAS#	Input	Column select: Specifies which command to execute.

Table 3: LP-DRAM Ball Assignments for LPDDR-SDRAM (continued)

137-Ball MCP (continued)				
LPDDR-SDRAM x16	**LPDDR-SDRAM x32**	**Symbol**	**Type**	**Description**
G8, H8	G8, H8	CK, CK#	Input	CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
E3, B2	E3, B2	CKE0, CKE1	Input	Clock enable. CKE0 is used for a single LPDDR-SDRAM product. CKE1 is used for dual LPDDR-SDRAM products, and is considered RFU for single LPDDR-SDRAM MCPs.
J2, F3	J2, F3	CS0#, CS1#	Input	Chip select: CS0# is used for a single LPDDR-SDRAM product. CS1# is used for dual LPDDR-SDRAM products, and is considered RFU for single LPDDR-SDRAM MCPs.
J8, G6	E7, F8, G6, J8	LDM, UDM (x16) DM[3:0] (x32)	Input	Data mask: Determines which bytes are written during WRITE operations. For x16 LPDDR-SDRAM, unused DM balls become RFU.
G2	G2	RAS#	Input	Row select: Specifies the command to execute.
K1	K1	WE#	Input	Write enable: Specifies the command to execute.
G3, J4, H5, H6, J5, J6, G7, K6, K5, K7, L8, K8, L7, L6, L5, L4	C7, C8, D7, D8, D6, E8, D5, F6, F7, E6, H4, H3, F5, E4, F4, G4, G3, J4, H5, H6, J5, J6, G7, K6, K5, K7, L8, K8, L7, L6, L5, L4	DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data bus: Data inputs/outputs. DQ[31:16] are RFU for x16 LPDDR-SDRAM devices.
J7, G5	E5, H7, G5, J7	LDQS, UDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Coordinates read/write transfers of data; one DQS per DQ byte. For x16 LPDDR-SDRAM, unused DQS balls become RFU.
B8, D1, H1, H10, M1, P8	B8, D1, H1, H10, M1, P8	V_{DD}	Supply	V_{DD}: LPDDR-SDRAM power supply.
C9, D10, E9, F10, G9, J10, K9, L9, M10, N9	C9, D10, E9, F10, G9, J10, K9, L9, M10, N9	$V_{DD}Q$	Supply	$V_{DD}Q$: LPDDR-SDRAM I/O power supply.
C10, D9, E10, F9, G10, J9, K10, L10, M9, N10	C10, D9, E10, F9, G10, J9, K10, L10, M9, N10	$V_{SS}Q$	Supply	$V_{SS}Q$: LPDDR-SDRAM I/O ground.
	M3	RFU[1]	–	Reserved for future use.

Note: Balls marked “RFU” may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 4: LP-DRAM Ball Assignments for LP-SDRAM

137-Ball Device				
LP-SDRAM x16	**LP-SDRAM x32**	**Symbol**	**Type**	**Description**
F1, F2, K3, D4, E2, D3, E1, D2, C2, L3, L2, L1, K4	F2, K3, D4, E2, D3, E1, D2, C2, L3, L2, L1, K4	A[12:0] (x16) A[11:0] (x32)	Input	Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LP-SDRAM address is determined by density and configuration. Consult the LP-SDRAM product datasheet for the maximum address for a given density and configuration. Unused address pins become "RFU.[1]"
J3, K2	J3, K2	BA0, BA1	Input	Bank address inputs: Specifies one of the four banks.
H2	H2	CAS#	Input	Column select: Specifies which command to execute.
E3, B2	E3, B2	CKE0, CKE1	Input	Clock enable. CKE0 is used for a single LP-SDRAM product. CKE1 is used for dual LP-SDRAM products, and is considered RFU for single LP-SDRAM MCPs.
G8	G8	CLK	Input	CLK is the system clock. All address and control signals are sampled on the rising edge of CLK.
J2, F3	J2, F3	CS0#, CS1#	Input	Chip select: CS0# is used for a single LP-SDRAM product. CS1# is used for dual LP-SDRAM products, and is considered RFU for single LP-SDRAM MCPs
J8, G6	E7, F8, G6, J8	LDQM, UDQM (x16) DQM[3:0] (x32)	Input	Input/output mask: DQM is sampled HIGH and is an input mask signal for WRITE accesses and an output enable signal for READ accesses. For x16 LP-SDRAM, unused DQM balls become RFU.
G2	G2	RAS#	Input	Row select: Specifies the command to execute.
K1	K1	WE#	Input	Write enable: Specifies the command to execute.
G3, J4, H5, H6, J5, J6, G7, K6, K5, K7, L8, K8, L7, L6, L5, L4	C7, C8, D7, D8, D6, E8, D5, F6, F7, E6, H4, H3, F5, E4, F4, G4, G3, J4, H5, H6, J5, J6, G7, K6, K5, K7, L8, K8, L7, L6, L5, L4	DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data bus: Data inputs/outputs. DQ[31:16] are RFU for x16 LP-SDRAM devices.
B8, D1, H1, H10, M1, P8	B8, D1, H1, H10, M1, P8	V_{DD}	Supply	V_{DD}: LP-SDRAM power supply.
C9, D10, E9, F10, G9, J10, K9, L9, M10, N9	C9, D10, E9, F10, G9, J10, K9, L9, M10, N9	$V_{DD}Q$	Supply	$V_{DD}Q$: LP-SDRAM I/O power supply.
C10, D9, E10, F9, G10, J9, K10, L10, M9, N10	C10, D9, E10, F9, G10, J9, K10, L10, M9, N10	$V_{SS}Q$	Supply	$V_{SS}Q$: LP-SDRAM I/O ground.
H8,	H8	NC	–	No connect: Not internally connected.
C7, C8, D5, D6, D7, D8, E4, E5, E6, E7, E8, F1, F4, F5, F6, F7, F8, G4, G5, H3, H4, H7, J7, M3	E5, F1, G5, H7, J7, M3	RFU[1]	–	Reserved for future use.

Notes: 1. Balls marked "RFU" may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 5: Non-Device-Specific Ball Assignments

137-Ball MCP				
Shared		**Symbol**	**Type**	**Description**
B9, C1, C5, H9, J1, M2, P6, P9		V_{SS}	Supply	V_{SS}: Shared ground.
Miscellaneous		**Symbol**	**Type**	**Description**
B1, B10		NC	–	No connect: Not internally connected.
A2, A9, A10, G1, R1, R2, R9, R10		DNU	–	Do not use: Must be grounded or left floating.
M4, P1		RFU[1]	–	Reserved for future use.

Notes: 1. Balls marked "RFU" may or may not be connected internally. These balls should not be used. Contact factory for details.

Electrical Specifications

Table 6: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
V_{CC}, V_{DD}, V_{DDQ} supply voltage relative to V_{SS}	V_{CC}, V_{DD}, V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature range		–55	+150	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, V_{DD}	1.70	1.80	1.95	V
I/O supply voltage	V_{DDQ}	1.70	1.80	1.95	V
Operating temperature range	–	–40	–	+85	°C

Device Diagrams

Figure 5: Functional Block Diagram: 137-Ball TFBGA (LPDDR-SDRAM) Example

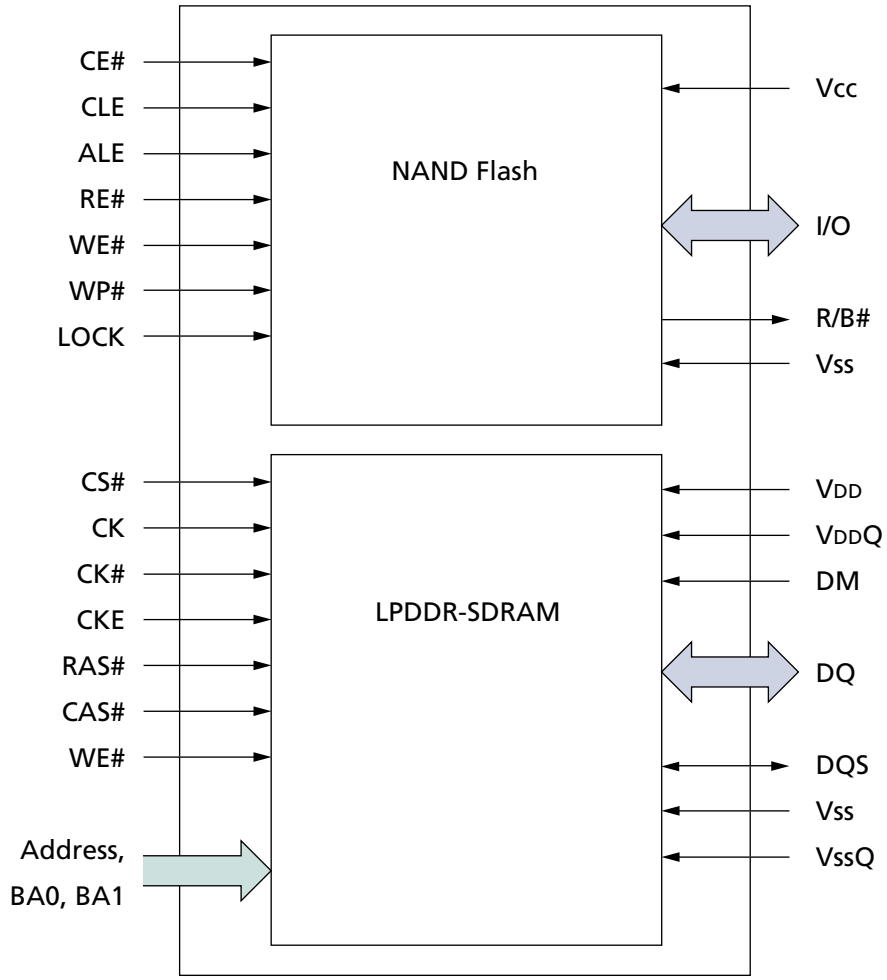
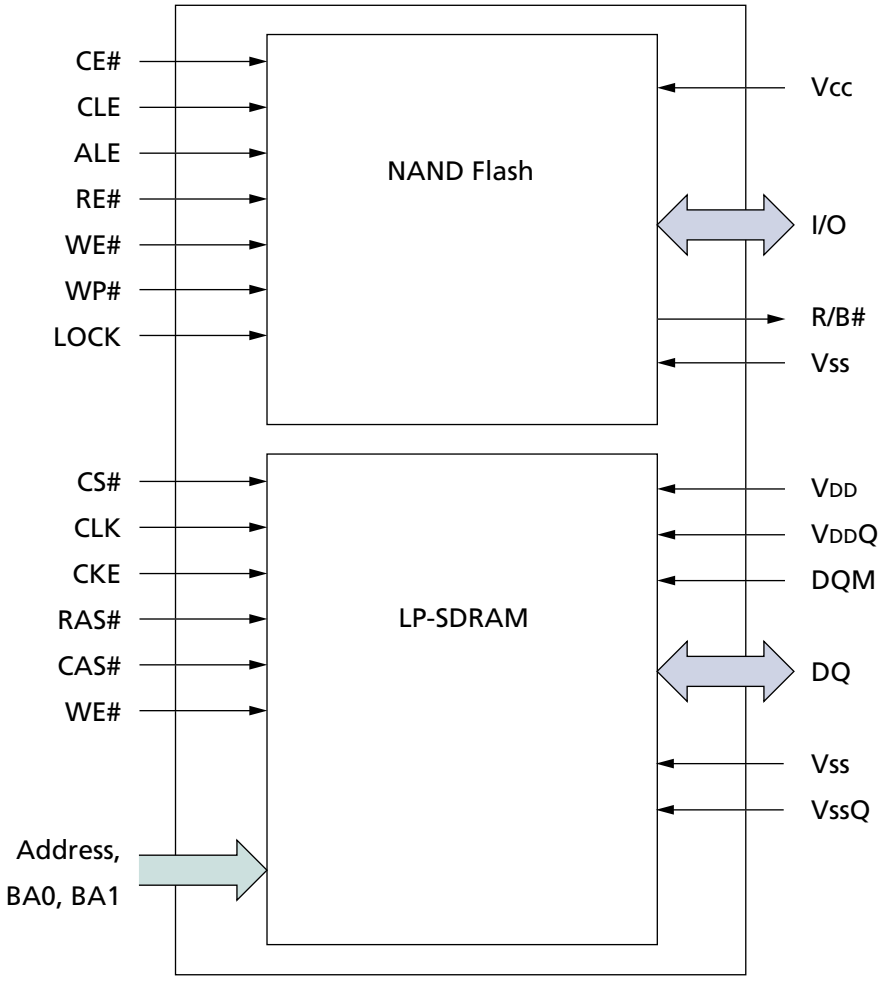


Table 8: Chip Select Signal Assignments per Chip Count Configuration

Chip Count	1st DRAM	2nd DRAM	Notes
1 NAND, 1 LP-DRAM	CS0#, CKE0	N/A	
1 NAND, 2 LP-DRAM	CS0#, CKE0	CS1#, CKE1	1
2 NAND, 2 LP-DRAM	CS0#, CKE0	CS1#, CKE1	1, 2

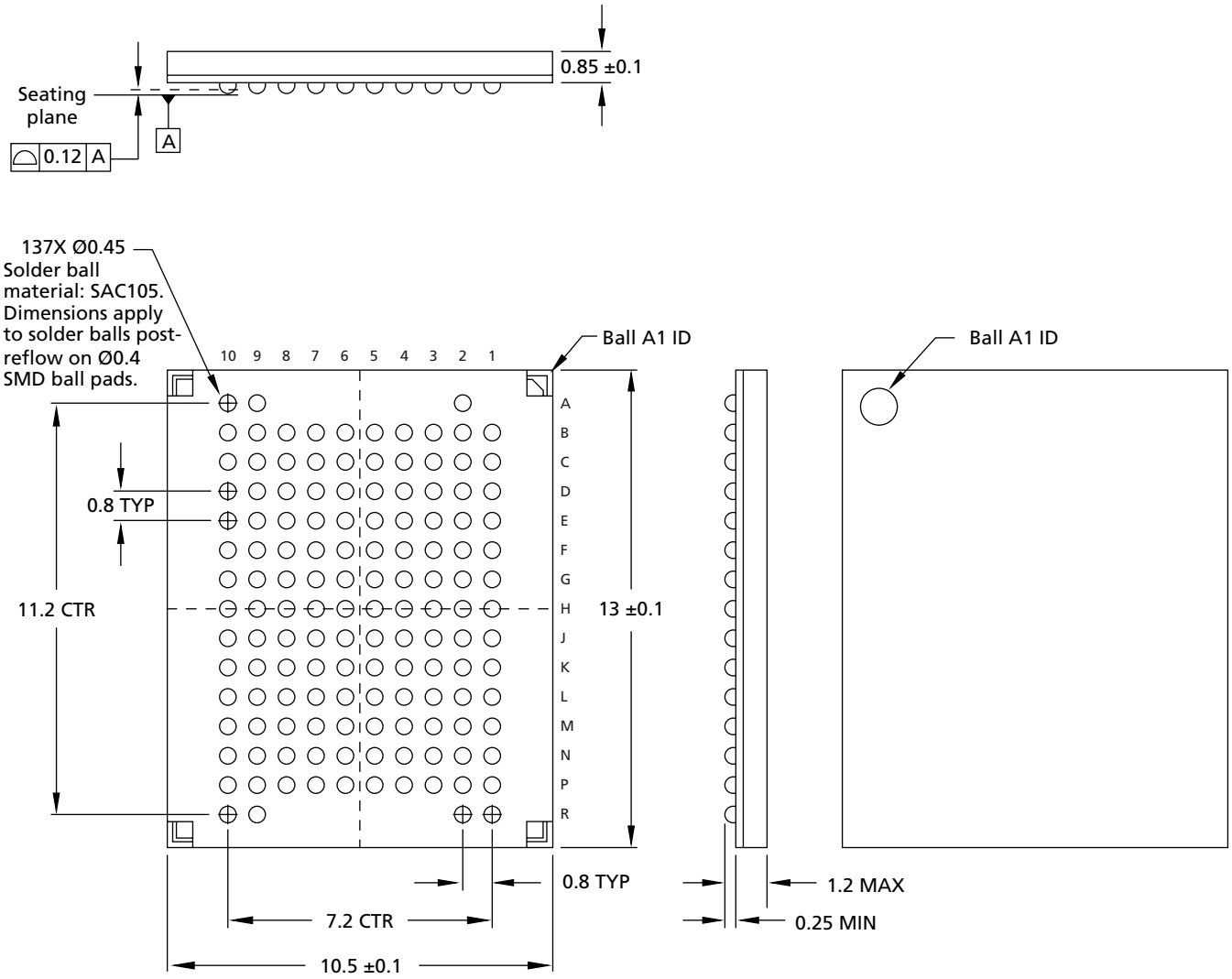
Notes: 1. All other signals are shared between both DRAM devices.
2. When multiple NAND chips are included, they share a single CE signal.

Figure 6: Functional Block Diagram: 137-Ball TFBGA (LP-SDRAM) Example



Package Dimensions

Figure 7: 137-Ball TFBGA



Note: All dimensions are in millimeters.

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Revision History

Rev. L, Preliminary 12/08

- "Options" on page 1: Added 200 MHz option.
- Figure 2: 137-Ball Marketing Part Number Example on page 2: Added 200 MHZ LP-DRAM Access Time.

Rev. K, Preliminary 11/08

- Figure 2: 137-Ball Marketing Part Number Example on page 2: Updated chip-count options.
- Table 1, Production Part Numbers for 137-Ball MCP Package, on page 2: Added JW257 and JW 258 details.

Rev. J, Preliminary 9/08

- Figure 2, 137-Ball Marketing Part Number Example, on page 2: Removed low power option.

Rev. I, Preliminary 8/08

- "NAND Flash-Specific Features" on page 1 added 8Gb NAND option.
- Figure 2, 137-Ball Marketing Part Number Example, on page 2 added 8Gb NAND option and 2 NAND, 2 DRAM chip count option, corrected typographical error on NAND Flash Configuration.
- Figure 3, Ball Assignment: 137-Ball TFBGA (LPDDR-SDRAM), on page 4: changed pin P1 from NC to RFU.
- Figure 4, Ball Assignment: 137-Ball TFBGA (LP-SDRAM), on page 5: changed pins E5, G5, H7, H8, J7, P1 from NC to RFU.
- Table 2, NAND Flash Ball Assignments, on page 6 and Table 3, LP-DRAM Ball Assignments for LPDDR-SDRAM, on page 6 and Table 4, LP-DRAM Ball Assignments for LP-SDRAM, on page 8: changed unused (based on configuration) DQ, I/O, command pins and P1 from NC to RFU.
- Figure 7, 137-Ball TFBGA, on page 13: Updated package diagram to reflect 0.10 tolerances.

Rev. H, Preliminary 5/08

- Figure 2: 137-Ball Marketing Part Number Example on page 2: Updated diagram.
- Table 1, Production Part Numbers for 137-Ball MCP Package, on page 2: Added new production part numbers.

Rev. G, Preliminary 5/08

- Table 1, Production Part Numbers for 137-Ball MCP Package, on page 2: Added new production part numbers.
- Capacitance tables deleted.

Rev. F, Preliminary 4/08

- Table 1, Production Part Numbers for 137-Ball MCP Package, on page 2: Added new production part numbers.

- Table 3, LP-DRAM Ball Assignments for LPDDR-SDRAM, on page 6, and Table 4, LP-DRAM Ball Assignments for LP-SDRAM, on page 8: Corrected CKE1 ball.
- Table 5, Non-Device-Specific Ball Assignments, on page 9: Updated NC ball listing.

Rev. E, Preliminary 2/08

- Figure 2: 137-Ball Marketing Part Number Example on page 2: Updated diagram.
- Table 1, Production Part Numbers for 137-Ball MCP Package, on page 2: Added table (and current production part number on page 1).
- Figure 3: Ball Assignment: 137-Ball TFBGA (LPDDR-SDRAM) on page 4 and Figure 4: Ball Assignment: 137-Ball TFBGA (LP-SDRAM) on page 5: Updated titles and ball assignments.
- Table 3, LP-DRAM Ball Assignments for LPDDR-SDRAM, on page 6: Updated table title, headings, and LDM, UDM, LDQS, UDQS assignments; updated CKE and CS descriptions; added RFU content and note.
- Table 4, LP-DRAM Ball Assignments for LP-SDRAM, on page 8: Added table and note.
- Table 5, Non-Device-Specific Ball Assignments, on page 9: Added note.
- Figure 5: Functional Block Diagram: 137-Ball TFBGA (LPDDR-SDRAM) Example on page 11 and Figure 6: Functional Block Diagram: 137-Ball TFBGA (LP-SDRAM) Example on page 12: Updated titles.

Rev. D, Preliminary 2/08

- Figure 7: 137-Ball TFBGA on page 13: Updated package diagram.

Rev. C, Preliminary 1/08

- Table 3, LP-DRAM Ball Assignments for LPDDR-SDRAM, on page 6: Removed M3 from DQ row, x16 LPDDR-DRAM column.
- Table 5, Non-Device-Specific Ball Assignments, on page 9: Removed P10 from both NC columns.
- Figure 4: Ball Assignment: 137-Ball TFBGA (LP-SDRAM) on page 5: Corrected color of ball B5.
- Figure 5: Functional Block Diagram: 137-Ball TFBGA (LPDDR-SDRAM) Example on page 11: Added LOCK input to NAND Flash.

Rev B, Preliminary 12/07

- “NAND Flash with LP-DRAM 137-Ball Multiple-Chip Package (MCP)” on page 1: Removed “Mobile” from title.
- “LP-DRAM-Specific Features” on page 1: Added SRR feature.
- Table 2, NAND Flash Ball Assignments, on page 6: Revised table.
- Separated original single ball-assignment table into individual tables: Table 2, NAND Flash Ball Assignments, on page 6, Table 3, LP-DRAM Ball Assignments for LPDDR-SDRAM, on page 6, and Table 5, Non-Device-Specific Ball Assignments, on page 9.
- Removed “Mobile” from LP-DRAM references and changed LP-DRAM to LPDDR-DRAM as applicable.

Rev. A, Preliminary 11/07

- Initial release.