

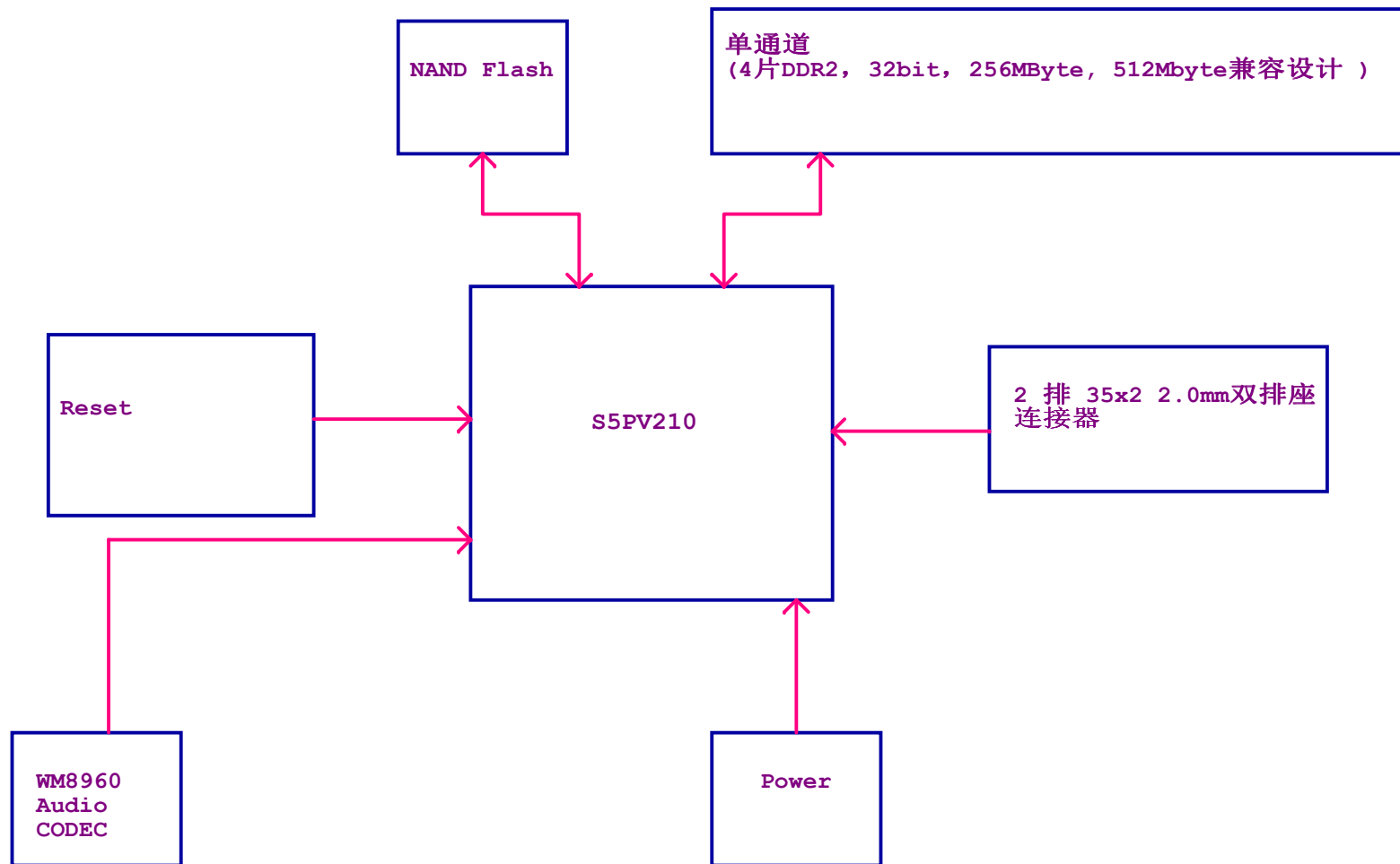
Revision History

Revision	Date	Comments
1.0	2010-12-9	初次版本

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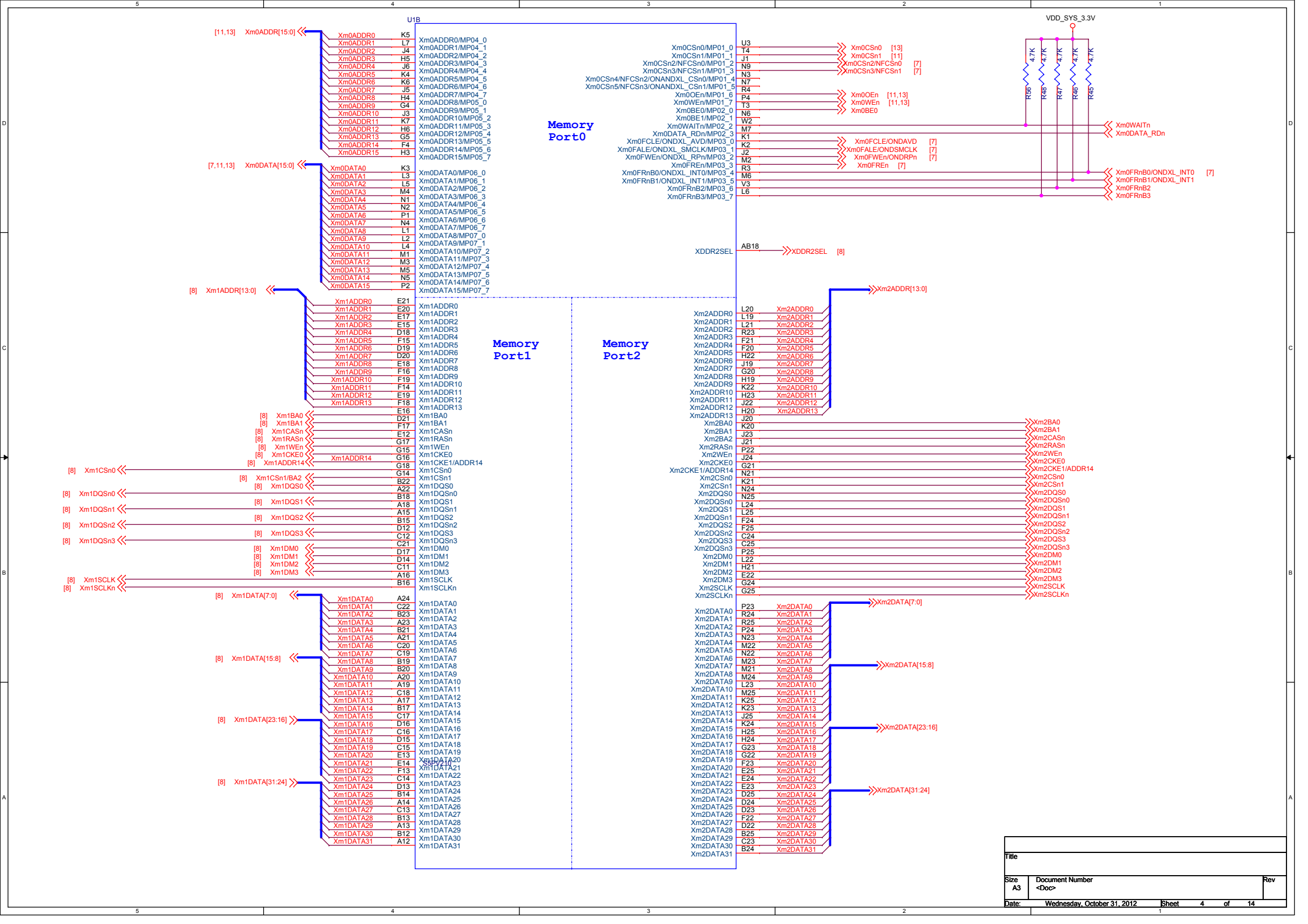
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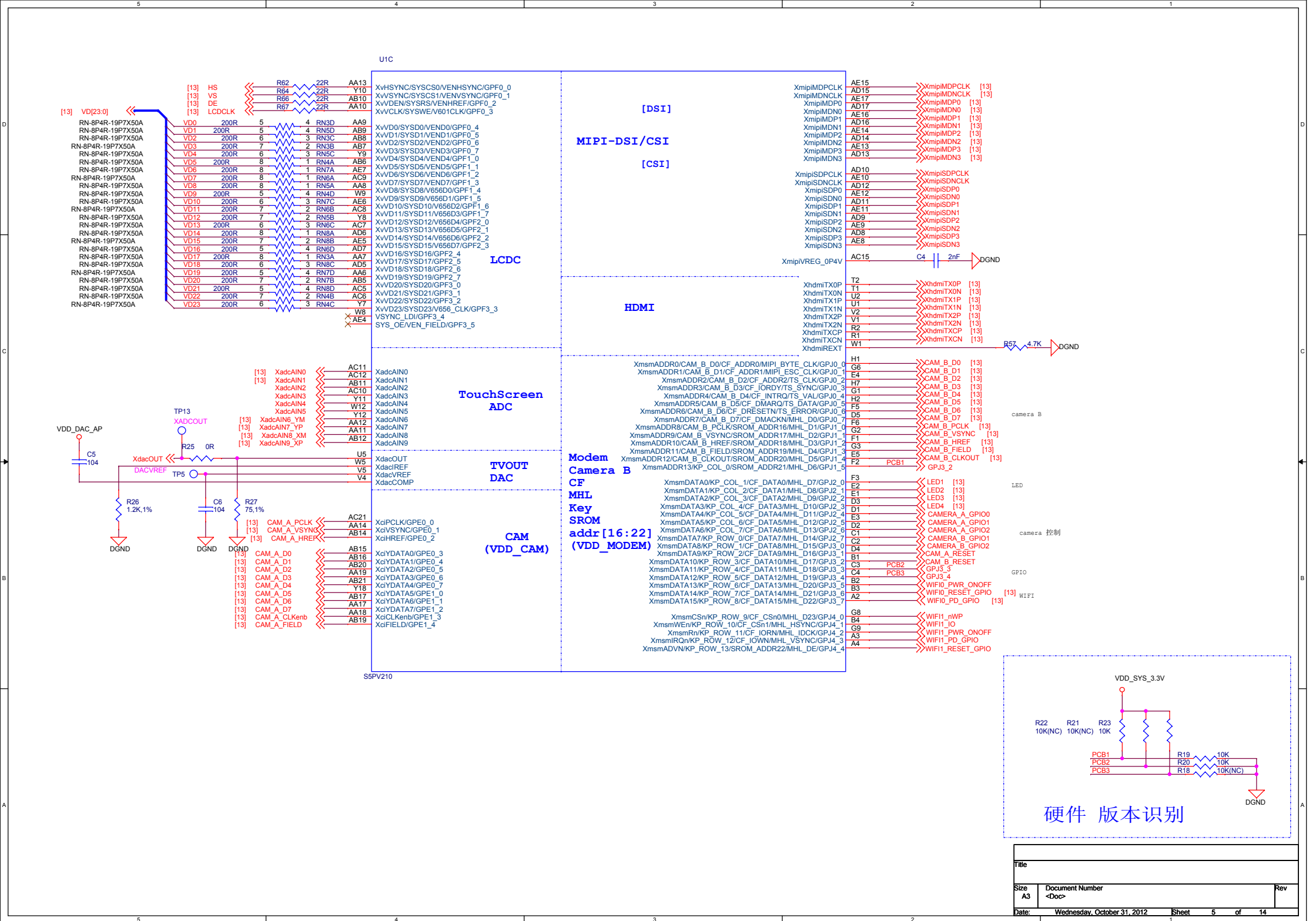
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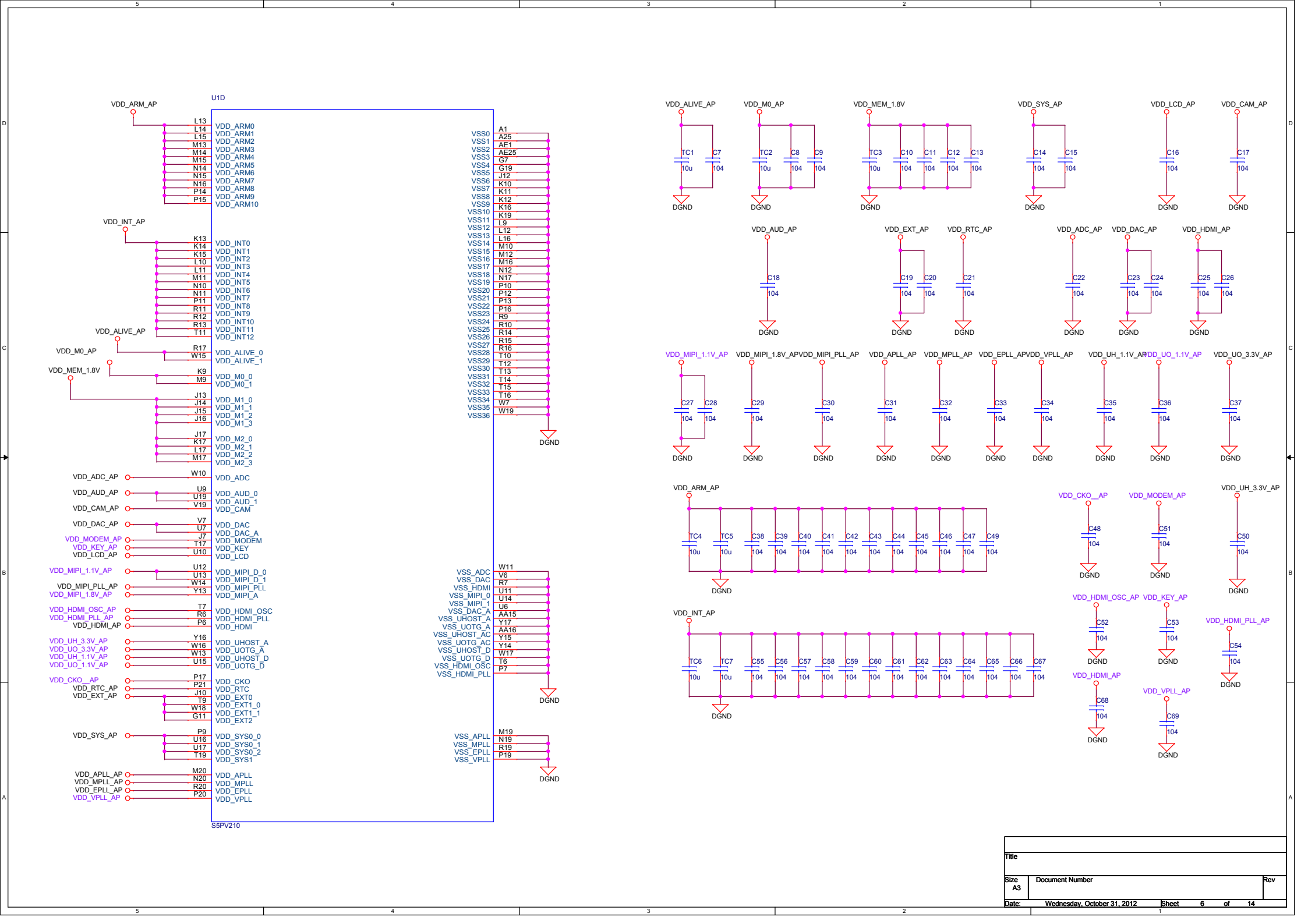


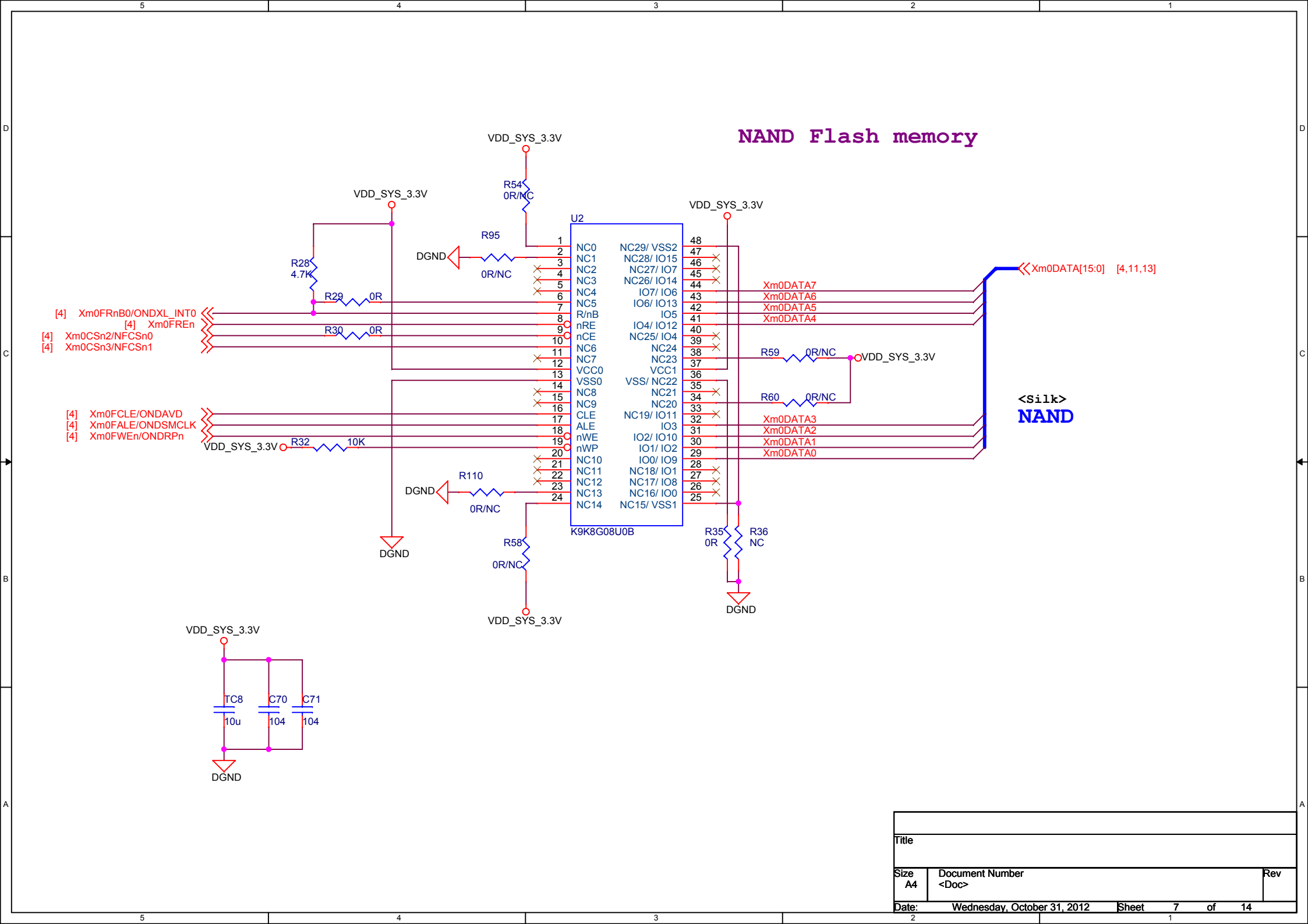
核心板面积大约75mm×75mm
周边4 排 50×2 2.0mm双排座连接器

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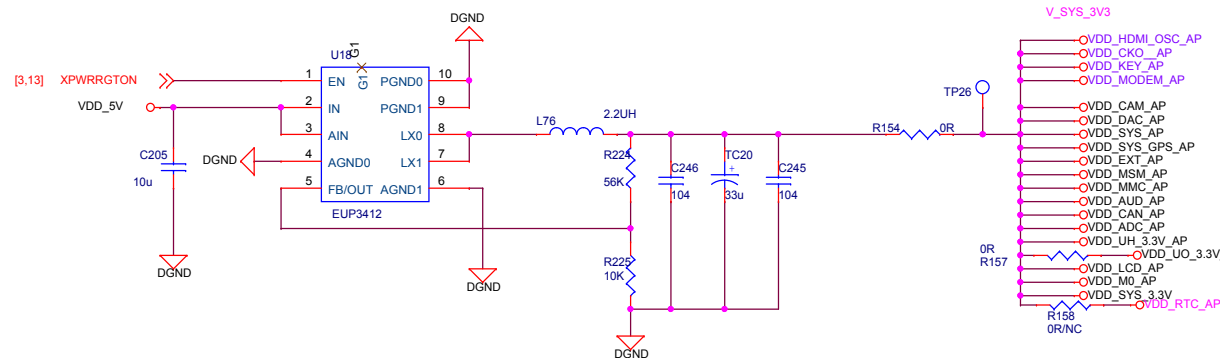
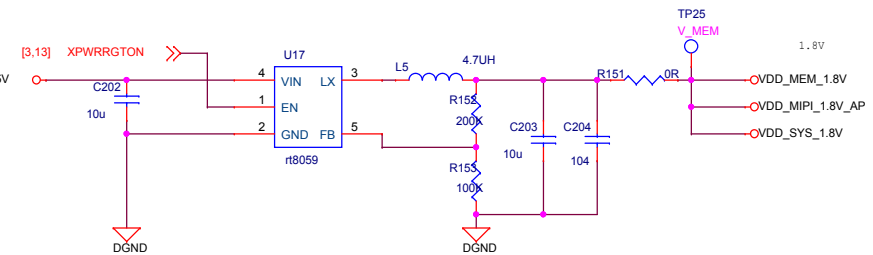
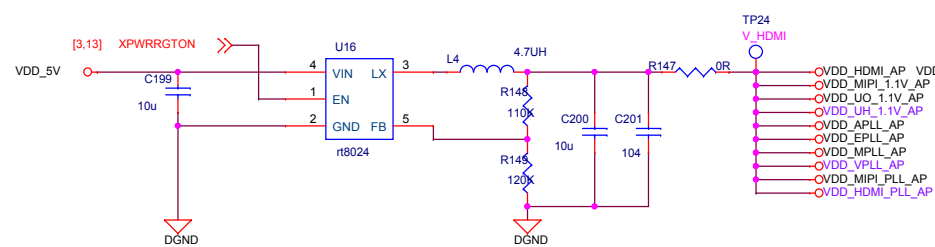
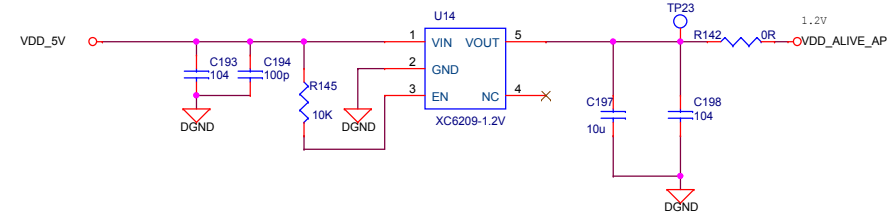
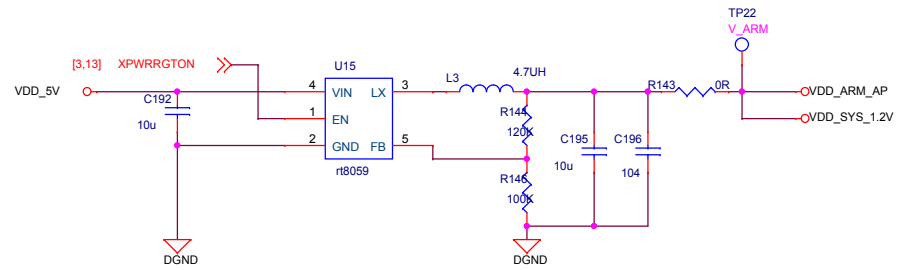
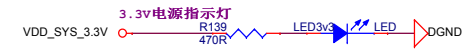
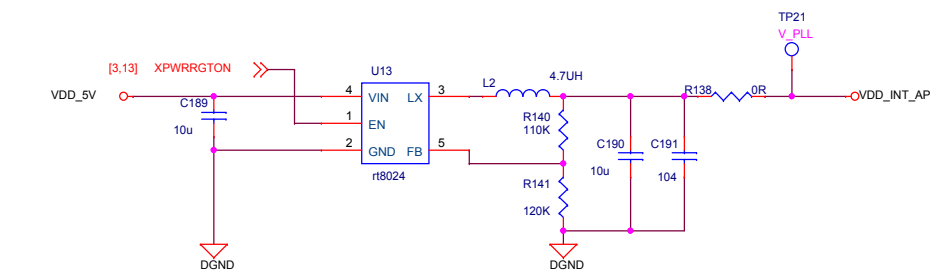


The diagram illustrates the TAG circuit connections. On the left, a vertical stack of components is shown: a 3.3V supply (VDD_SYS 3.3V) at the top, followed by resistors R80 (10K), R81 (10K), R83 (10K), and R84 (10K). Below these is a 10K resistor (R85) connected to GND. To the right of this stack are four input pins: XjTRSTn, XjTDI, XjTMS, and XjTCK, each with a blue circle symbol. Below these is a 470R resistor (R94) connected to GND. The output pin XjTDO is connected to a 470R resistor (R94) which is then connected to the array. The array is represented by a dashed box labeled 'Place array'. The circuit is labeled 'TAG电路' at the bottom left.

The image displays four circuit diagrams for different modules, each featuring a crystal oscillator and associated passive components.

- For PLL:** A 24MHz-M crystal (X1) is connected to a 5.1M resistor (R77) and a 15pF capacitor (C137) to ground (DGND). The other end of the crystal is connected to a 15pF capacitor (C138) to ground. The output signals are XT1 and XTO.
- For USB HOST:** A 24MHz-H crystal (X2) is connected to a 5.1M resistor (R79) and a 15pF capacitor (C139) to ground (DGND). The other end of the crystal is connected to a 15pF capacitor (C143) to ground. The output signals are XusbXT1 and XusbXTO.
- For VEDIO:** A 27MHz crystal (X3) is connected to a 5.1M resistor (R78) and a 15pF capacitor (C140) to ground (DGND). The other end of the crystal is connected to a 15pF capacitor (C142) to ground. The output signals are XhdmixT1 and XhdmixTO.
- For RTC:** A 32.768K crystal (X4) is connected to a 10M resistor (R82) to ground (DGND). The crystal is also connected to a 13pF capacitor (C141) to ground. The output signals are XrtcXT1 and XrtcXTO.

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