AN2569
Application note

STM32F10xxx GPIO application examples

Introduction

This application note is intended to provide practical application examples of the STM32F10xxx GPIO peripheral use.

This document, its associated firmware, and other such application notes are written to accompany the STM32F10xxx firmware library. These are available for download from the STMicroelectronics website: *www.st.com.*

1 STM32F10xxx I/O toggling

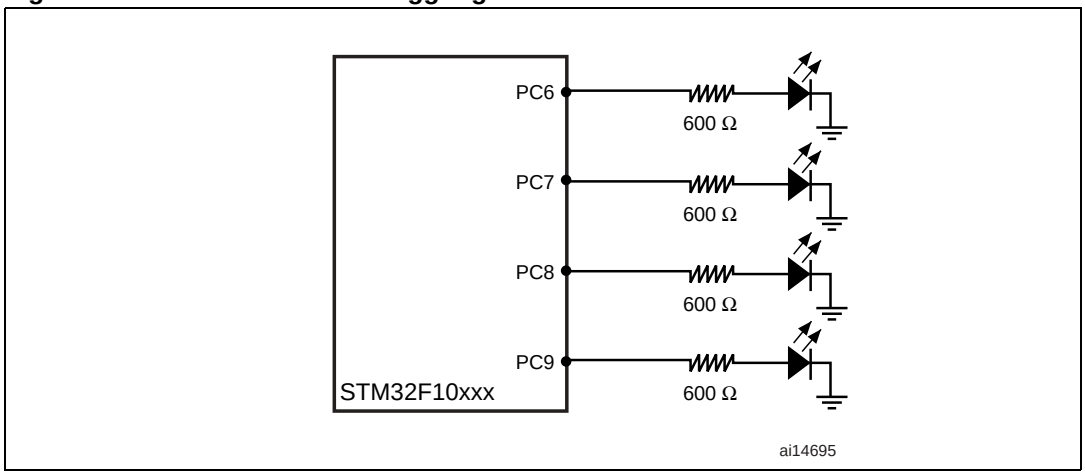
1.1 Overview

This example describes how to use the Port Bit Set/Reset register (GPIO BSRR) and the Port Bit Reset register (BRR) for I/O toggling.

1.2 Hardware description

Figure 1 shows the example hardware connection used. The hardware consists of 4 LEDs connected to the PC6, PC7, PC8 and PC9 pins.

Figure 1. STM32F10xxx I/O toggling



1.3 Firmware description

The provided firmware includes the GPIO driver that supports all GPIO features through a set of functions. An example of use for most of these functions is provided.

In this example GPIO, BSRR (Port Bit Set/Reset register) and BRR (Port Bit Reset register) are used for I/O toggling. With these registers, one or more GPIO pins can be modified in a single atomic write access.

This firmware is provided as GPIO example1 in the STM32F10xxx firmware library, available from the STMicroelectronics microcontroller website.

2 Using the STM32F10xxx SWJ pins as standard I/Os

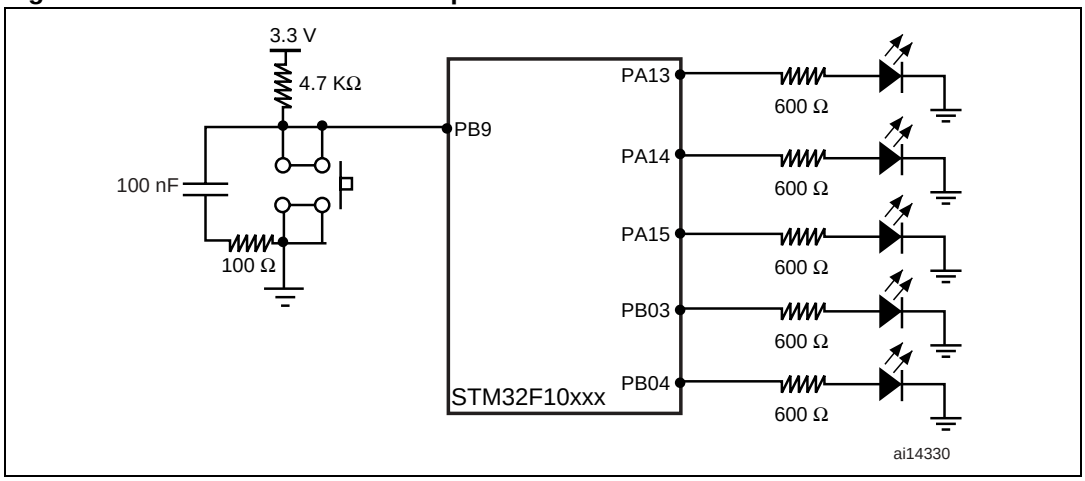
2.1 Overview

This section describes how to use the GPIO firmware library to release the SWJ-DP (Serial Wire JTAG- Debug Port) pins and reuse them as standard I/Os.

2.2 Hardware description

Figure 2 shows how to connect the five LEDs to the SWJ-DP pins.

Figure 2. STM32F10xxx SWJ-DP pins used as Standard I/Os



2.3 Firmware description

The provided firmware includes the GPIO driver that supports all GPIO features through a set of functions. An example of use for most of these functions is provided.

First, the SWJ-DP is disabled. The SWJ-DP pins are configured as output push-pull. Five LEDs connected to the PA13(JTMS/SWDAT), PA14(JTCK/SWCLK), PA15(JTDI), PB03(JTDO) and PB04(JTRST) pins are toggled in an infinite loop.

Note that once the JTAG IOs are disabled, the connection with the host debugger is lost and cannot be re-established as long as the JTAG IOs remain disabled. To avoid this situation, the PB09 pin is connected to a push-button that is used to disable or not the JTAG IOs:

- push-button pressed at reset: JTAG IOs disabled
- push-button not pressed at reset: JTAG IOs unchanged

This firmware is provided as *GPIO example2* in the STM32F10xxx firmware library, available from the STMicroelectronics microcontrollers website.

2.4 Conclusion

The SWJ-DP IOs can be used as standard IOs to reach 80% of the IO ratio.

3 Revision history

Table 1. Document revision history

Date	Revision	Changes
14-Jun-2007	1	Initial release.
11-Oct-2007	2	*Section 1: STM32F10xxx I/O toggling* added.

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