1/4-INCH VGA CMOS ACTIVE-PIXEL DIGITAL IMAGE SENSOR DIE

MT9V111

Features

- DigitalClarity™ CMOS Imaging Technology
- Ultra low-power, low-cost CMOS image sensor
- Superior low-light performance
- Up to 30 fps progressive scan at 27 MHz for high-quality video at VGA resolution
- On-chip Image Flow Processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, 2X fixed zoom
- Image decimation to arbitrary size with smooth, continuous zoom and pan
- Automatic exposure, white balance and black compensation, flicker avoidance, color saturation, and defect identification and correction, auto frame rate, black light compensation
- Xenon and LED-type flash support
- Two-wire serial programming interface
- ITU-R BT.656 (YCbCr), YUV, 565RGB, 555RGB, or 444RGB output data formats

General Physical Specifications

- Wafer thickness: 305µm ±12µm (12.0 mil ±0.5 mil) *(Consult factory for die thickness other than 305µm)*
- Backside wafer surface of polished bare silicon
- Typical metal 1 thickness: 3.1KÅ
- Typical metal 2 thickness: 3.1KÅ
- Typical metal 3 thickness: 6.1KÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over titanium
- Typical topside passivation: 2.2KÅ nitride over 6.0KÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm (2.95 mil x 3.54 mil)

Option

- Form

Die	D
Wafer – 200mm (8")	W

- Testing

Standard (Level 1) Probe	C1

NOTE: Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database K82A
Die Outline
(see page 8)

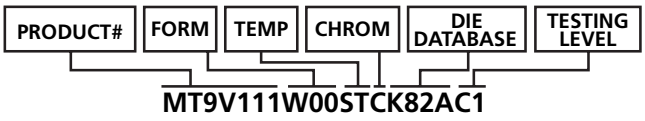
Die Size: 6,267.00µm x 6,267.00µm
246.732 mil x 246.732 mil

See Tables 1 and 2, "K82A Bond Pad Location and Identfications," on pages 4–7

Order Information

2.8V Power Supply:

MT9V111W00STCK82AC1
MT9V111D00STCK82AC1



Key Performance Parameters

- Optical Format: 1/4-inch (4:3)
- Active Imager Size: 3.584mm(H) x 2.688mm(V)
- Active Pixels: 640H x 480V (VGA)
- Pixel Size: 5.6µm x 5.6µm
- Color Filter Array: RGB Bayer Pattern
- Shutter Type: Electronic Rolling Shutter (ERS)
- Data Rate/Master Clock:
  12 MPS/12 MHz (default)
  27 MPS/27 MHz (MAX)
- Frame Rate:
  VGA (640H x 480V) 15 fps @ 12 MHz (default), programmable up to 30 fps @ 27 MHz
  CIF (352H x 288V) programmable up to 60 fps
  QVGA (320H x 240V) programmable up to 90 fps
- ADC Resolution: 10 bit, on chip
- Responsivity: 1.9V/lux-sec (550nm)
- Dynamic range: 60 dB
- SNR_{MAX}: 45dB
- Supply Voltage: 2.8V ±0.25V
- Power Comsumption: <80mW at 2.8V, 12MHz, 15 fps and VGA resolution
- Operating Temperature: -20°C to +60°C

General Description

The MT9V111 is a one-fourth inch VGA-format CMOS active-pixel digital image sensor, the result of combining the MT9V011 image sensor core with Micron® Imaging's third-generation digital image flow processor technology. The MT9V111 has an active imaging pixel array of 649 x 489, capturing high-quality color images at VGA resolution. The sensor is a complete camera-on-a-chip solution and is designed specifically to meet the demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9V111 is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed via a parallel eight-bit DOUT port as shown in Figure 1. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. The die can be put in an ultra-low power sleep mode by asserting the STANBY pin. Output pads can also be tri-stated by de-asserting the OE_BAR pad. The MT9V111 internal registers can be configured using a two-wire serial interface.

The MT9V111 can be programmed to output progressive scan images up to 30 fps in an 8-bit ITU_R BT.656 (YCbCr) formerly CCIR656, YUV, 565RGB, 555RGB, or 444RGB formats. The FRAME_ and LINE_VALID signals are output on dedicated pads, along with a pixel clock that is synchronous with valid data.

Die Testing Procedures

Micron® Imager die products are tested with a Standard Probe (C1) test. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-chip A/D converter, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

Please refer to the packaged product data sheets found on Micron's Web site (www.micron.com) for functional and parametric specifications. The specifications are provided for reference only.

Bonding Instructions

The K82A Imager die has 44 bond pads. Refer to Tables 1 and 2 for a complete list of bond pads and coordinates.

The K82A Imager die does not require the user to determine bond option features.

The K82A Imager die also has several pads defined as "Do Not Use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 3 shows the MT9V111 typical die connections. For low-noise operation the MT9V111 die requires separate supplies for analog and digital power.

Wafer Saw

A standard wafer saw cuts the die 100 percent through. Micron holds die dimensions to a maximum tolerance of +0/-25µm (+0/-1 mil) of each cut, as measured from the vertical cut. For clarification purposes, the die size provided is measured from center of the die street to center of the die street. A finished die is approximately 38µm (1.5 mil) smaller on each side due to the sawing operation. For example, a 5,080µm x 7,620µm (200 mil x 311 mil) die is approximately 5,042µm x 7,582µm (198.5 mil x 309.5 mil) after sawing.

Wafer-Level Processing

Customers should choose the wafer form when post-processing of die is required. This includes adding extra passivation or metal layers or bumping of the bond pads. For these customers, the street widths are provided in the die outline. Also, a reference from the center of bond pad 1 to the center of the intersection of two streets is provided as an easy alignment reference.

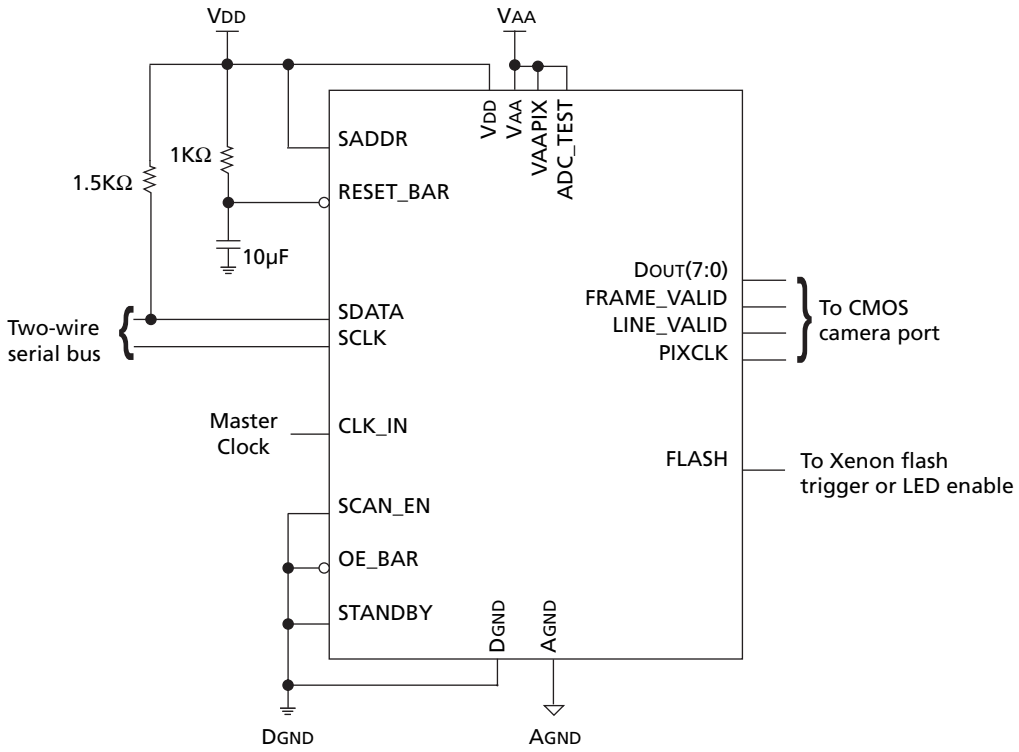
Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Micron recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Figure 1: Typical Configuration (Connection)



NOTE:

Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.

Table 1: K82A Bond Pad Location and Identification

PAD	MT9V111	FROM CENTER OF PAD 1			
		"X"[1] MICRONS	"Y"[1] MICRONS	"X"[1] INCHES	"Y"[1] INCHES
1	DGND3	0.00	0.00	0.0000000	0.0000000
2	DOUT2	466.56	0.00	0.0183685	0.0000000
3	DOUT3	933.12	0.00	0.0367370	0.0000000
4	DOUT4	1399.68	0.00	0.0551055	0.0000000
5	DOUT5	1866.24	0.00	0.0734740	0.0000000
6	DGND4	2332.80	0.00	0.0918425	0.0000000
7	VDD3	2799.36	0.00	0.1102110	0.0000000
8	DOUT6	3686.72	0.00	0.1451465	0.0000000
9	DOUT7	4153.28	0.00	0.1635150	0.0000000
10	VDD4	4619.84	0.00	0.1818835	0.0000000
11	DGND5	5086.40	0.00	0.2002520	0.0000000
12	VDD5	5502.95	-416.55	0.2166514	-0.0163994
13	VDD6	5502.95	-883.11	0.2166514	-0.0347679
14	DGND	5502.95	-1349.67	0.2166514	-0.0531364
15	DGND6	5502.95	-1816.23	0.2166514	-0.0715049
16	VDD7	5502.95	-2282.79	0.2166514	-0.0898734
17	DGND7	5502.95	-2749.35	0.2166514	-0.1082419
18	OE_BAR	5502.95	-3215.91	0.2166514	-0.1266104
19	STANDBY	5502.95	-3682.47	0.2166514	-0.1449789
20	RESET_BAR	5502.95	-4149.03	0.2166514	-0.1633474
21	VAAPIX	5502.95	-4655.91	0.2166514	-0.1833033
22	ADC_TEST	5502.95	-5142.63	0.2166514	-0.2024656
23	AGND1	5086.40	-5798.21	0.2002520	-0.2282760
24	VAA1	4619.84	-5798.21	0.1818835	-0.2282760
25	AGND0	4153.28	-5798.21	0.1635150	-0.2282760
26	VAA0	3686.72	-5798.21	0.1451465	-0.2282760
27	VDD0	2799.36	-5798.21	0.1102110	-0.2282760
28	DGND0	2332.80	-5798.21	0.0918425	-0.2282760
29	SADDR	1866.24	-5798.21	0.0734740	-0.2282760
30	SDATA	1399.68	-5798.21	0.0551055	-0.2282760
31	SCLK	933.12	-5798.21	0.0367370	-0.2282760
32	CLK_IN	466.56	-5798.21	0.0183685	-0.2282760
33	DGND1	0.00	-5798.21	0.0000000	-0.2282760
34	VDD1	-295.27	-5142.63	-0.0116246	-0.2024656
35	FRAME_VALID	-295.27	-4655.91	-0.0116246	-0.1833033

Table 1: K82A Bond Pad Location and Identification (continued)

PAD	MT9V111	FROM CENTER OF PAD 1			
		"X"[1] MICRONS	"Y"[1] MICRONS	"X"[1] INCHES	"Y"[1] INCHES
36	LINE_VALID	-295.27	-4149.03	-0.0116246	-0.1633474
37	PIXCLK	-295.27	-3682.47	-0.0116246	-0.1449789
38	FLASH	-295.27	-3215.91	-0.0116246	-0.1266104
39	DGND2	-295.27	-2749.35	-0.0116246	-0.1082419
40	DNU[2]	-295.27	-2282.79	-0.0116246	-0.0898734
41	DNU	-295.27	-1816.23	-0.0116246	-0.0715049
42	DOUT0	-295.27	-1349.67	-0.0116246	-0.0531364
43	DOUT1	-295.27	-883.11	-0.0116246	-0.0347679
44	VDD2	-295.27	-416.55	-0.0116246	-0.0163994

NOTE:
1. Reference to center of each bond pad from center of bond pad number 1.
2. DNU = "Do Not Use."

Table 2: K82A Bond Pad Location and Identification

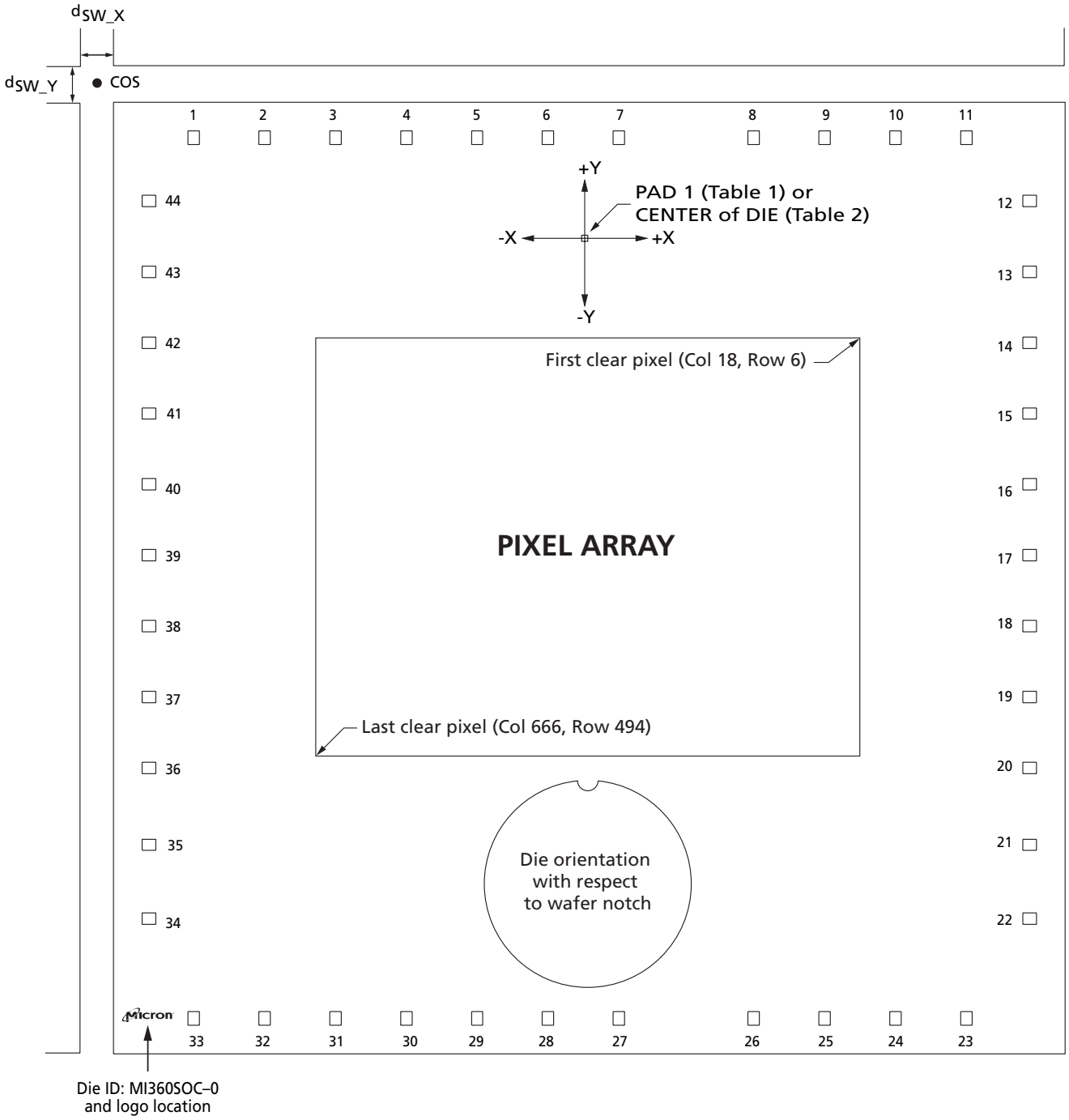
PAD	MT9V111	FROM CENTER OF DIE (0, 0)			
		"X"[1] MICRONS	"Y"[1] MICRONS	"X"[1] INCHES	"Y"[1] INCHES
1	DGND3	-2603.84	2899.11	-0.1025134	0.1141380
2	DOUT2	-2137.28	2899.11	-0.0841449	0.1141380
3	DOUT3	-1670.72	2899.11	-0.0657764	0.1141380
4	DOUT4	-1204.16	2899.11	-0.0474079	0.1141380
5	DOUT5	-737.60	2899.11	-0.0290394	0.1141380
6	DGND4	-271.04	2899.11	-0.0106709	0.1141380
7	VDD3	195.52	2899.11	0.0076976	0.1141380
8	DOUT6	1082.88	2899.11	0.0426331	0.1141380
9	DOUT7	1549.44	2899.11	0.0610016	0.1141380
10	VDD4	2016.00	2899.11	0.0793701	0.1141380
11	DGND5	2482.56	2899.11	0.0977386	0.1141380
12	VDD5	2899.11	2482.56	0.1141380	0.0977386
13	VDD6	2899.11	2016.00	0.1141380	0.0793701
14	DGND	2899.11	1549.44	0.1141380	0.0610016
15	DGND6	2899.11	1082.88	0.1141380	0.0426331
16	VDD7	2899.11	616.32	0.1141380	0.0242646
17	DGND7	2899.11	149.76	0.1141380	0.0058961
18	OE_BAR	2899.11	-316.80	0.1141380	-0.0124724
19	STANDBY	2899.11	-783.36	0.1141380	-0.0308409
20	RESET_BAR	2899.11	-1249.92	0.1141380	-0.0492094
21	VAAPIX	2899.11	-1756.80	0.1141380	-0.0691654
22	ADC_TEST	2899.11	-2243.52	0.1141380	-0.0883276
23	AGND1	2482.56	-2899.11	0.0977386	-0.1141380
24	VAA1	2016.00	-2899.11	0.0793701	-0.1141380
25	AGND0	1549.44	-2899.11	0.0610016	-0.1141380
26	VAA0	1082.88	-2899.11	0.0426331	-0.1141380
27	VDD0	195.52	-2899.11	0.0076976	-0.1141380
28	DGND0	-271.04	-2899.11	-0.0106709	-0.1141380
29	SADDR	-737.60	-2899.11	-0.0290394	-0.1141380
30	SDATA	-1204.16	-2899.11	-0.0474079	-0.1141380
31	SCLK	-1670.72	-2899.11	-0.0657764	-0.1141380
32	CLK_IN	-2137.28	-2899.11	-0.0841449	-0.1141380
33	DGND1	-2603.84	-2899.11	-0.1025134	-0.1141380
34	VDD1	-2899.11	-2243.52	-0.1141380	-0.0883276
35	FRAME_VALID	-2899.11	-1756.80	-0.1141380	-0.0691654

Table 2: K82A Bond Pad Location and Identification (continued)

PAD	MT9V111	FROM CENTER OF DIE (0, 0)			
		"X"[1] MICRONS	"Y"[1] MICRONS	"X"[1] INCHES	"Y"[1] INCHES
36	LINE_VALID	-2899.11	-1249.92	-0.1141380	-0.0492094
37	PIXCLK	-2899.11	-783.36	-0.1141380	-0.0308409
38	FLASH	-2899.11	-316.80	-0.1141380	-0.0124724
39	DGND2	-2899.11	149.76	-0.1141380	0.0058961
40	DNU[2]	-2899.11	616.32	-0.1141380	0.0242646
41	DNU	-2899.11	1082.88	-0.1141380	0.0426331
42	DOUT0	-2899.11	1549.44	-0.1141380	0.0610016
43	DOUT1	-2899.11	2016.00	-0.1141380	0.0793701
44	VDD2	-2899.11	2482.56	-0.1141380	0.0977386

NOTE:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = "Do Not Use."

Figure 2: Die Outline (Top View)



NOTE:

1. Die street widths are not drawn to scale.
2. In die orientation as shown, the image is inverted reverted.

Wafer Diameter: 200mm (8")

Wafer Thickness: 305µm ± 12µm (12.0 mil ± 0.5 mil)

Die Size (stepping interval):
6,267.0µm x 6,267.0µm
(246.732 mil x 246.732 mil)

Street Width
Along X-Axis (dsw_X): 127.0µm (5.00 mil)

Street Width
Along Y-Axis (dsw_Y): 127.0µm (5.00 mil)

Center of Streets (COS)
(Relative to Bond Pad 1):
X = -529.66µm, Y = 234.395µm
(X = -20.853 mil, Y = 9.228 mil)

Bond Pad Size (MIN): 85.0µm x 100µm
(3.35 mil x 3.94 mil)

Passivation Openings (MIN): 75.0µm x 90.0µm
(2.95 mil x 3.54 mil)

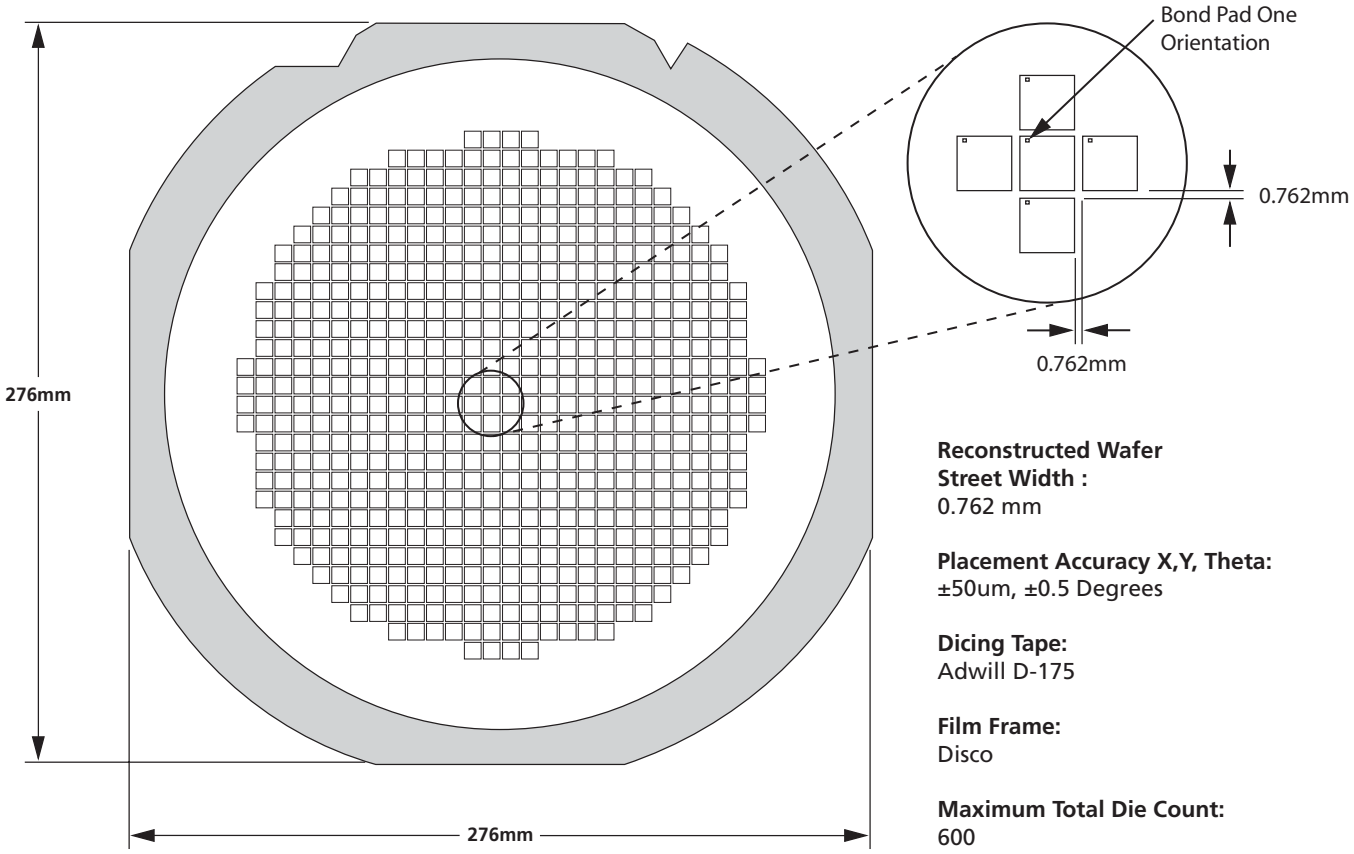
Minimum Bond Pad Pitch: 466.56µm (18.369 mil)

Optical Array (Orientation Inverted Reverted):
Optical Center from Chip Center
X = 11µm, Y = 91.3µm

First Clear Pixel (Col 18, Row 6)
From Chip Center:
X = 1803.41µm, Y = 1457.47µm
From Center of Pad 1:
X = 4407.34µm, Y = -1441.61µm

Last Clear Pixel (Col 666, Row 494)
From Chip Center:
X = -1825.39µm, Y = -1275.32µm
From Center of Pad 1:
X = 778.44µm, Y = -4174.41µm

Figure 3: K82A Die Orientation in Reconstructed Wafer



Reconstructed Wafer Street Width :
0.762 mm

Placement Accuracy X,Y, Theta:
±50um, ±0.5 Degrees

Dicing Tape:
Adwill D-175

Film Frame:
Disco

Maximum Total Die Count:
600

Data Sheet Designation

No Mark: Although considered final, these specifications are subject to change.

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Revision History

Rev F, Pub. 04/04, No Mark 4/04
- Added **Figure 3**

Rev E, Pub. 03/04, No Mark 3/04
- Added information to the **Features** and **Key Performance Parameters** paragraphs in page 1
- Changed second paragraph under **General Despcription**
- Modified **Figure 1** to show how to connect bond pad 22 (ADC_TEST)
- Changed bond pad 22 name to better describe its function (ADC_TEST)

Rev D, Pub. 02/04, No Mark 2/04
- Changed YCrCb to YCbCr
- Changed Supply Voltage: 2.8V ±0.3V to Supply Voltage: 2.8V ±0.25V

Rev C, Pub. 02/04, No Mark 2/04
- Added **Key Performance Parameters**
- Added **Figure 1**
- Modified **Features** and **Bonding Instructions**
- Changed data sheet designation to No Mark

Rev B, Pub. 11/03, Preliminary 11/03
- Updated part numbers

Rev A, Pub. 11/03, Preliminary 11/03