

MSP430 Isolated FET Interface

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MSP430

ABSTRACT

This application report describes how to build an isolated FET interface for the MSP430 Flash Emulation Tool (FET). When developing and debugging line-powered MSP430 applications such as motor control, electricity energy meters, power monitoring systems etc. it is important to have electrical isolation for the development tool such that the personnel involved and the connected electronic equipment, like the host PC, is protected.

The simple interface solution presented in this report uses two dual ISO150 isolated bi-directional digital couplers to achieve the required isolation. This solution not only provides electrical isolation for protection but also eliminates ground loops, which is a requirement while debugging high-performance analog applications.

This document includes the schematics, layout, and bill of materials for building this interface. The Gerber files for the PCB are provided in the zip file associated with this application report.

Introduction

The FET interface box MSP-FETP430IF is widely used for developing and debugging MSP430Fxxx microcontroller applications [1]. The function of this FET interface box is to provide level shifting of the JTAG signals between the host PC and the MSP430 target. However, it does not provide electrical isolation rendering it unusable for line-powered MSP430 applications such as motor control, electricity energy meters, power monitoring systems etc. due to safety issues to the person using the tool and the potential to permanently damage the equipment used including the host PC.

The isolated FET interface described in this application report offers both level shifting of the JTAG signals and electrical isolation. It is designed to be a drop-in replacement board for the MSP-FETP430IF interface box.

Circuit Description

The isolated FET interface design supports the following functional requirements:

- JTAG signals level shifting between the PC printer port and the MSP430 target
- Electrical isolation with a minimum isolation voltage of 1.5-kV
- Low current operation such that it can be powered directly from the PC printer port and the MSP430 target power supply

The key component for this application is the isolated coupler. There are many types of isolated couplers available today. The most common types are optical couplers. High-speed optical couplers have typical propagation delays in the range of 1- μ s and do not meet the speed requirement of MSP430 JTAG signals. Faster optical isolators need high current drive and operate at 5-V. Optical couplers also have the disadvantage of drawing high pulse currents when the integrated LED is active.

The ISO150 dual isolated bi-directional digital coupler [2] selected for this design eliminates all the previously mentioned disadvantages. In this device the digital signal is transmitted across an isolation barrier by coupling pulses through high-voltage capacitors. The device has the following features that make it suitable for this application:

- Very short propagation delay, 27 ns typical
- Operating supply voltage range from 3-V to 5.5-V
- Input and output voltage levels are dependent on the supply voltages (level-shifter capability)
- Low operating current
- Minimum isolation voltage of 1500-V at 60 Hz

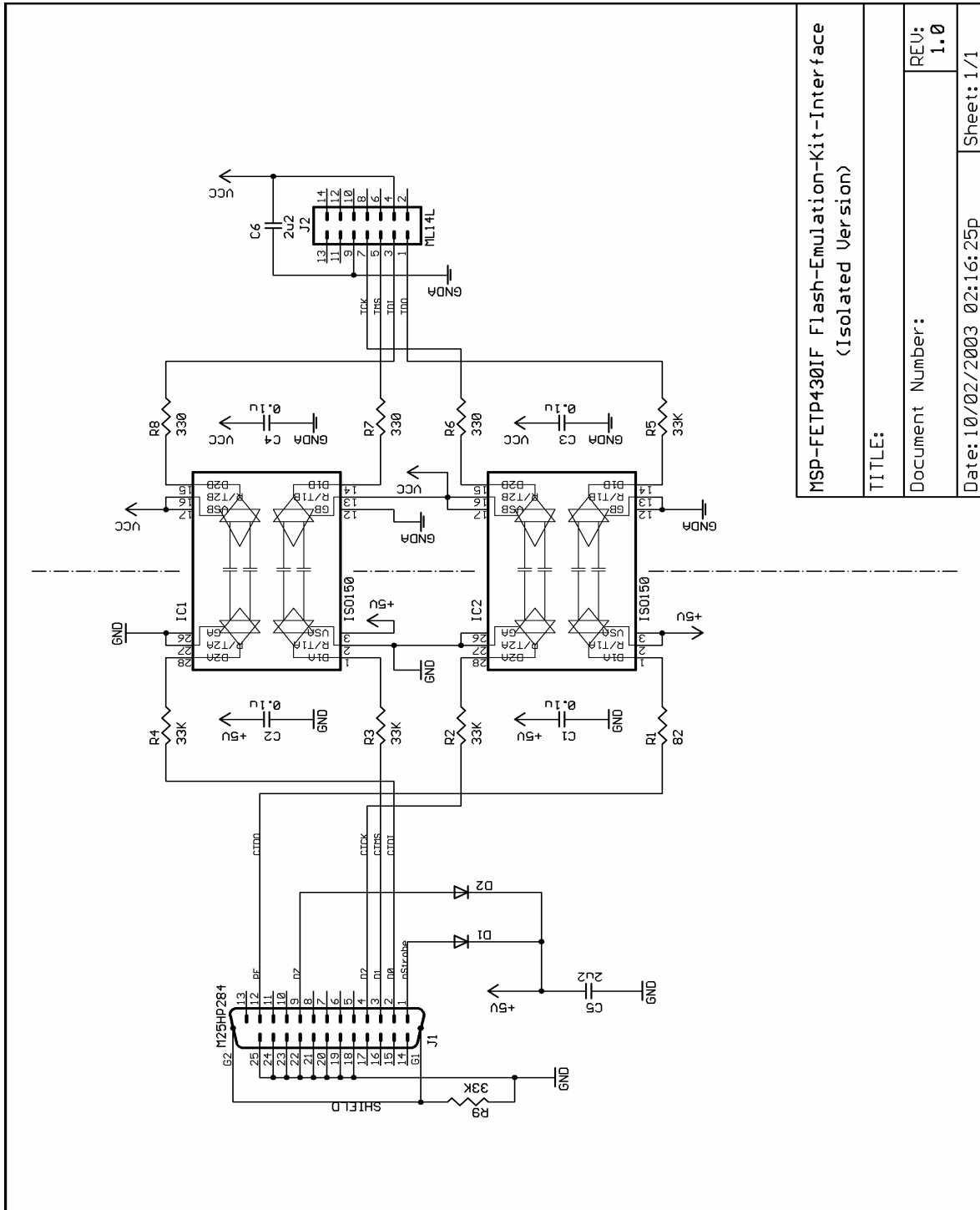
MSP430 derivatives that have dedicated JTAG pins require a minimum of four signals TCK, TMS, TDI and TDO for JTAG communication. In the FET interface TCK, TMS and TDI are directed from the PC to the MSP430, and TDO is directed from the MSP430 back to the host PC. To isolate these four signals two ISO150 devices are required as each device has two independent channels. To program and debug MSP430 derivatives with shared JTAG pins, the interface design needs to be extended to additionally support the JTAG TEST signal from the PC to the MSP430. Either one more ISO150 coupler or a single channel optical coupler could be used for supporting this function.

During operation, the PC side of the interface operates three channels in transmit mode and one channel in receive mode. This results in approximately 2-mA current consumption, which can be easily supported by the PC parallel port. The MSP430 side operates three channels in receive mode and one channel in transmit mode. This results in approximately 6-mA current consumption from the MSP430 application. This current is drawn from the MSP430 application circuit via pin four of the JTAG connector.

The decoupling capacitors on both sides provide the required power supply decoupling and high frequency noise rejection when the CMOS ICs are switched. The series resistors in the data lines are used both for circuit protection and line impedance matching, based on the original FET interface design [1].

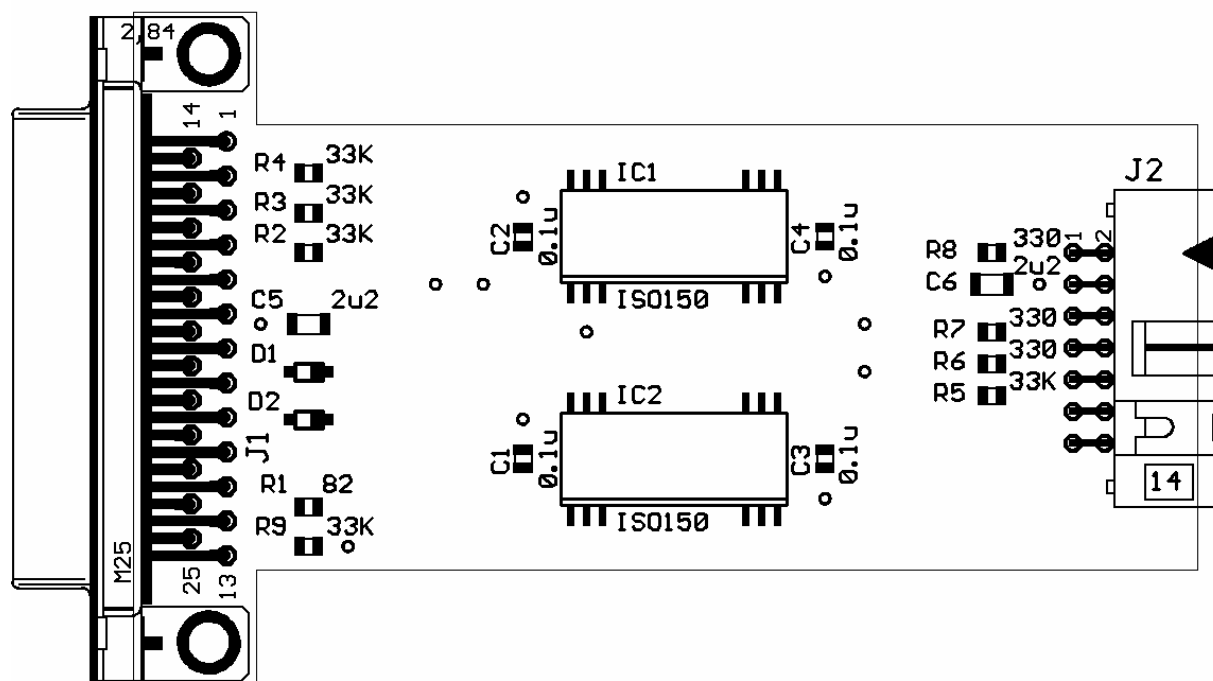
The D-Sub connector for interfacing with the PC parallel port as well as the 14-pin JTAG header uses the same pin out as the standard MSP-FETP430IF interface.

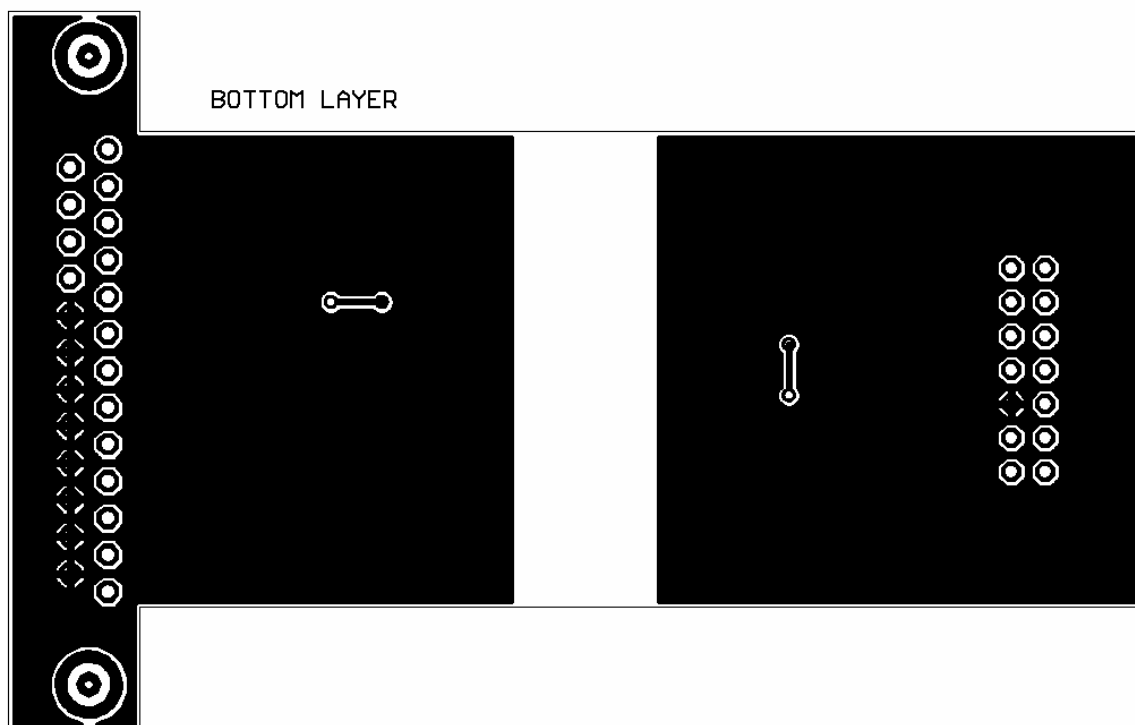
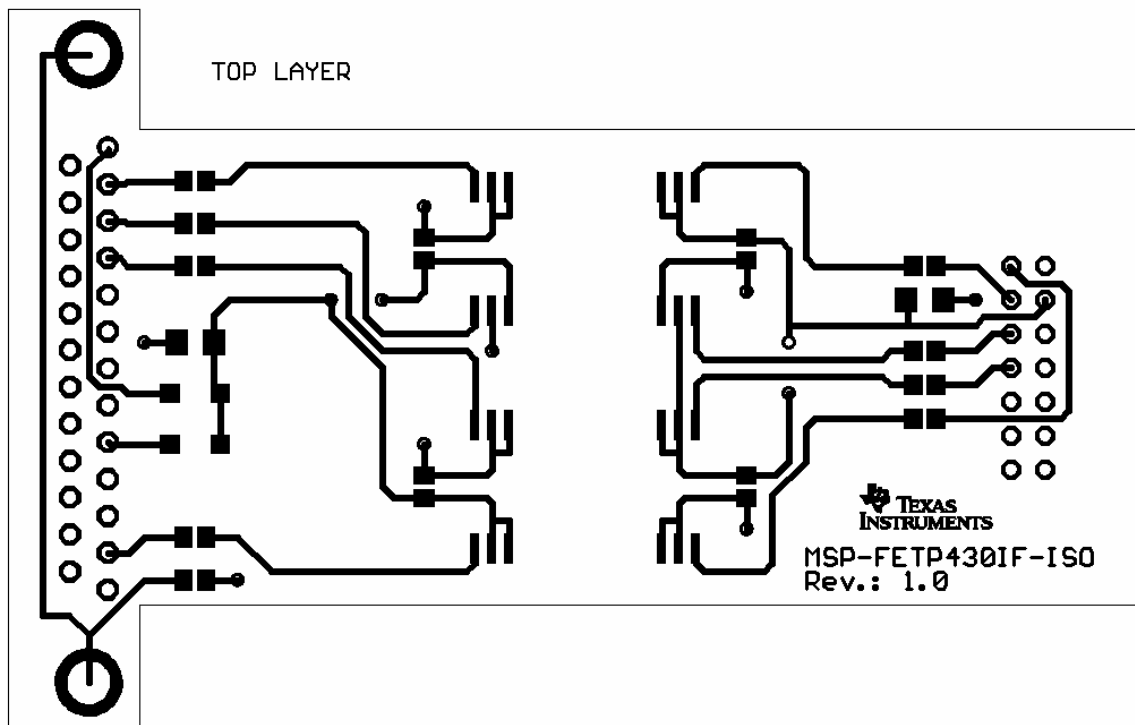
Schematic



Board Layout

The PCB designed for this application is a two-layer board. The layout information is provided as a zip file along with this application report and is in the extended Gerber file (274x) format. The following three images show component placement, top layer and the bottom layer. Please note that the images are not to scale.





Bill of Materials

Table 1 shows the BOM for the Isolated FET interface. The parts can be ordered retail from Digi-Key (<http://www.digikey.com>).

Table 1. Bill of materials

Qty	Digi-Key#	Value	Package	Parts
2	B0520LWDICT-ND	Diode Schottky, 20V	SOD-123	D1, D2
4	311-1142-1-ND	0.1u	SMT-0805	C1, C2, C3, C4
2	PCC2312CT-ND	2u2	SMT-1206	C5, C6
5	311-33.0KCCT-ND	33k	SMT-0805	R2, R3, R4, R5, R9
1	311-82.0CCT-ND	82R	SMT-0805	R1
3	311-330CCT-ND	330R	SMT-0805	R6, R7, R8
2	ISO150AU-ND	ISO150AU	SO-28	IC1, IC2
1	A23283-ND	Connector D-Sub, 25 Pin, Right Angle, Male		J1
1	A26287-ND	Header, 14 Pin, Right Angle, Male		J2

The board is designed to fit into the same enclosure used for the standard MSP-FETP430IF interface. The enclosure can be purchased directly from PacTec (<http://www.pactecenclosures.com>), the model number is CNL-0006.

Using the isolated FET interface

The MSP430 target application must be powered by its own power supply. Pin four of the JTAG header must be connected to the V_{CC} of the target MSP430. The MSP430 application power supply must be capable of providing the additional 6-mA current drawn by the isolated FET interface. The minimum operating voltage must be at least 3V, which is the minimum operating voltage for the ISO150 couplers used in this isolated FET interface.

This interface can be used only with MSP430 devices that have dedicated JTAG pins such as MSP430F13x, MSP430F14x, MSP430F15x, MSP430F16x, MSP430F4xx and MSP430FE4xx (Electricity Meter) derivatives. For use with MSP430 devices with shared JTAG pins the isolated FET interface must be modified as described in the circuit description section.

References

1. *MSP430-FET FLASH Emulation Tool (FET) User's Guide*
2. *ISO150 Dual, Isolated, Bidirectional Digital Coupler Data sheet (SBOS032)*

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