C1L5-06

LTPS TFT LCD Driver 132xRGBx160 with 262K Color

MD Electronic System Design Dept.

TPO Displays Corp.

Revision History

Ver. No	Date	Section	Description
0.01	2006/05/18		New release
0.02	2006/08/25	13	Tearing Effect Output
		19	Application Circuit

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Section **page**

1. GENERAL SPECIFICATION

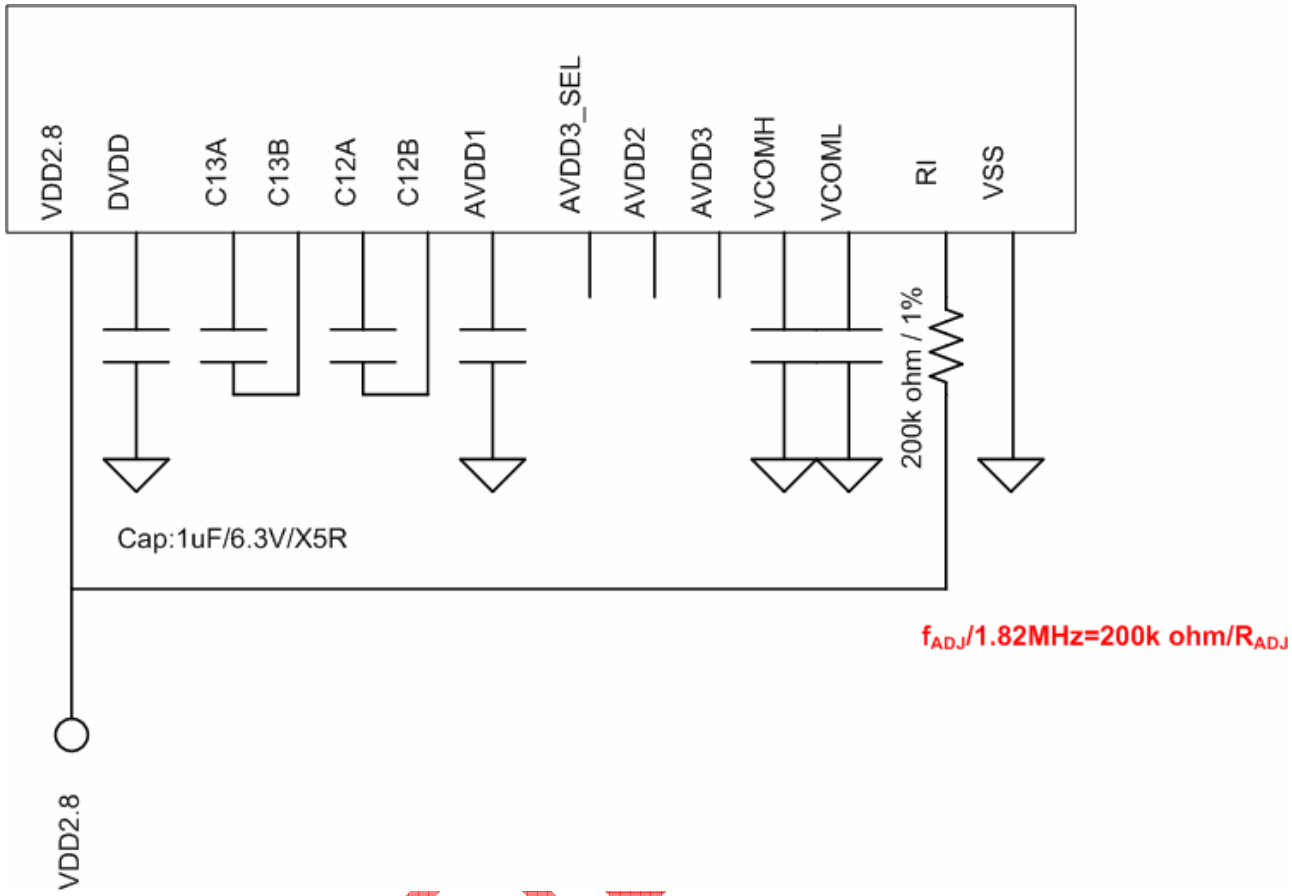
Item	Description
Process	0.18um CMOS process embedded SRAM
Package	**COG**
Function	1. Timing controller (Embedded SRAM = 132 x RGB x 160 x 6 bit) 2. Digital to Analog Driver 3. Level shifter 4. DC to DC inverter

2. FEATURES

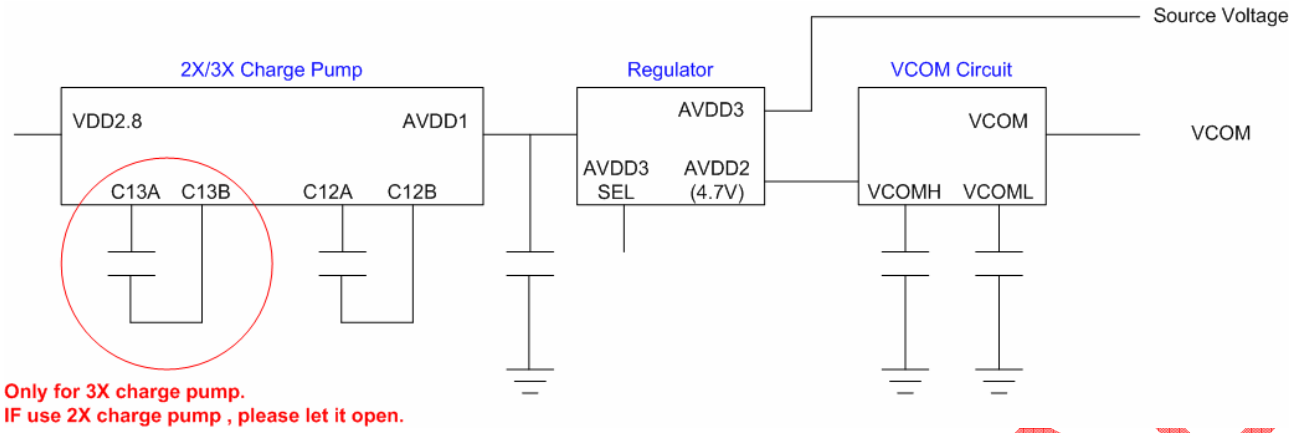
- ✧ 132 channels source driver output for LTPS LCD panel.
- ✧ Embedded single 380.16K bits (132 × 160 × 6 bits × RGB) SRAM to support single panel display
- ✧ Built-in LCD timing controller
- ✧ Built-in level shifter
- ✧ Built-in clock generator (VCO) function.
- ✧ DC/DC Charge pump
- ✧ Support 4 resolution types: 132x160, 128x160, 128x128, 96x 96,
- ✧ Supply Power Voltage Range VDD2.8=2.5V to 3.3V
- ✧ Supply I/O Voltage Range VDDIO=1.6V to 3.3V
- ✧ Support i80/M68 CPU interface with 8 / 9 / 16 / 18 bits
- ✧ Support 16/18 bits parallel RGB interface DE / HS +VS Modes
- ✧ Support 3-wire serial peripheral Interface (SPI)
- ✧ Support 5 display modes for CPU interface: normal / partial / 8 color / 8 color dithering / sleep mode / deep sleep mode
- ✧ Support 6 display modes for parallel RGB interface: moving / still / partial / 8 color / 8 color dithering / sleep mode / deep sleep mode
- ✧ Built-in gamma correction function and adjustable by registers.
- ✧ Line / frame inversion supported.
- ✧ HBM ESD (Handling body mode) > ±2KV , MM (machinery mode) > ±200V and Latch up > ±200mA

3. BLOCK DIAGRAM

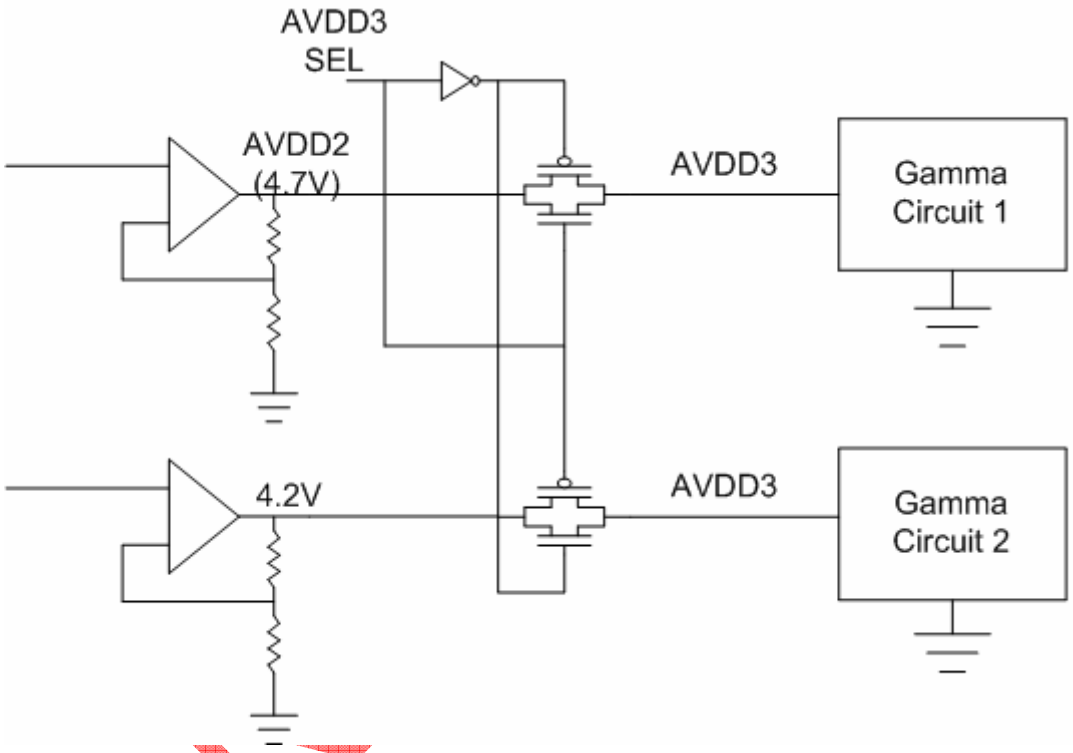
DC/DC Block



f_{ADJ}/1.82MHz=200k ohm/R_{ADJ}



Only for 3X charge pump.
IF use 2X charge pump , please let it open.



4. PIN DESCRIPTIONS

Pin Name	Type	Description
Power Supply Pins		
VDD2.8	P	Power supply voltage for DC/DC converter and analog system
VDDIO	P	Power supply voltage for interface system
VSS	P	System ground
Interface Pins		
nReset	I	Device reset signal. It's active low.
HOST[1:0]	I	Interface type select HOST1 / HOST0 / Designation 0 / 0 / 8080-series system 1 / 0 / 6800-series system 0 / 1 / Parallel RGB with 3-wires SPI 1 / 1 / 3-wires SPI
nCS (DE)	I	Chip Select or Data Enable 8080-series/6800-series: H: Chip de-select L: Chip select Parallel RGB: H: DATA valid L: DATA invalid (If no used, please connect to VDDIO or VSS)
RS	I	Command/DATA select H: DATA L: Command (If no used, please connect to VDDIO or VSS)
nWR (R/W、HS)	I	8080-series: write enable 6800-series: read and write select H: read L: write Parallel RGB: horizontal sync input (If no used, please connect to VDDIO or VSS)
nRD (E、VS)	I	8080-series: read enable 6800-series: read/write enable Parallel RGB: vertical sync input (If no used, please connect to VDDIO or VSS)
D[17:0]	I/O	18 bit bi-directional display data bus for parallel interface 8 bit bus use D[7:0] 9 bit bus use D[8:0] 16 bit bus use D[15:0](Parallel RGB Mode R:G:B=5:6:5) 18 bit bus use D[17:0](Parallel RGB Mode R:G:B=6:6:6) (If no used, please connect to VDDIO or VSS)
MCLK	I	Pixel clock (If no used, please connect to VDDIO or VSS)
SPI_nCS	I	Serial- peripheral interface enable (If no used, please connect to VDDIO or VSS)
SCK	I	Serial-peripheral interface DATA transfer clock (If no used, please connect to VDDIO or VSS)
SDI	I	Serial- peripheral interface DATA input (If no used, please connect to VDDIO or VSS)
SDO	O	Serial- peripheral interface DATA output (If no used, please connect to VDDIO or VSS)
Panel Control Signal Pins		
CKH1	O	RGB switch control signal
CKH2	O	RGB switch control signal
CKH3	O	RGB switch control signal
CKH4	O	RGB switch control signal
CKH5	O	RGB switch control signal

CKH6	O	RGB switch control signal
STV	O	Vertical driver shift register start pulse for panel 1
CKV	O	Vertical driver shift register clock pulse
ENBV	O	Gate enable pulse
CSV	O	Vertical scan direction control (Controlled by MODE_SEL2[7]) H: normal scan L: reverse scan
VC1	O	
VC2	O	
GAS	O	Gate all select
DO[65:0]	O	Pixel electrode driving output
VCOM	O	VCOM voltage for LCD panel display
VCOMH	O	VCOM high voltage output
VCOML	O	VCOM low voltage output
RI	I	VCO frequency adjust pin
DC to DC Converter Pins		
nPWDN	I	DC/DC converter control pin H: enable L: disable If no used, please open this pin
DVDD	O	Regulator output for logical system power
AVDD1	O	Regulator output for analog circuit and panel control timing output
AVDD2	O	Regulator output for VCOM output
AVDD3	O	Regulator output for Gamma circuit output
AVDD3_SEL	I	Select AVDD3 voltage 4.7V/4.2V H(AVDD1): AVDD3=4.7V L(VSS):AVDD3=4.2V
XVDD	O	Regulator output for SOP power supply(AVDD1)
C12A		Capacitor connection for 2X charge pump
C12B		Capacitor connection for 2X charge pump
C13A		Capacitor connection for 3X charge pump (If no used, please open this pin)
C13B		Capacitor connection for 3X charge pump (If no used, please open this pin)
CPCLK10	O	Clock output for SOP 2x charge pump
CPCLK55	O	Clock output for SOP -1x charge pump
Other Pins		
VDDIOOUT	O	If no used, please open this pin
VSSOUT	O	If no used, please open this pin
TEST		Please open this pin
DUMMY		Please open this pin
NC		Please open this pin

5. PADS LAYOUT, COORDINATION

5.1 PAD LAYOUT (Bump View)

-Chip size(excluding scribe lane): 6770 um x 870 um

-Chip thickness: 400 +/- 25.4 um

-PAD coordinate: PAD center

-Coordinate origin: Chip center

-Au bump size

Input side: 25 um x 100 um

Output side: 45 um x 63 um

Corner Bump: 90um x 90um

-Au bump height: 15 +/- 3um

-Au bump hardness: 65 +/- 15 HV

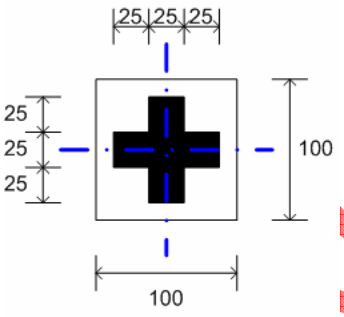
-Au bump co-planarity: < 1 um within chip

-Alignment Mark coordinate

M1(-3150，200)

M2(3150，200)

-Alignment Mark size



-Dummy bump coordinate

M3(-3300，175)

M4(-3300，235)

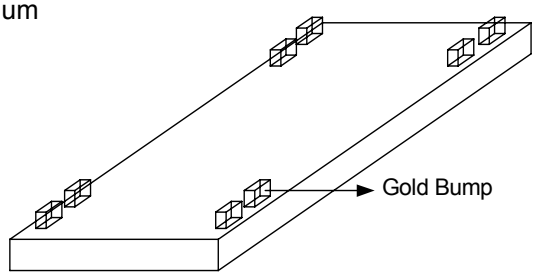
M5(3300，175)

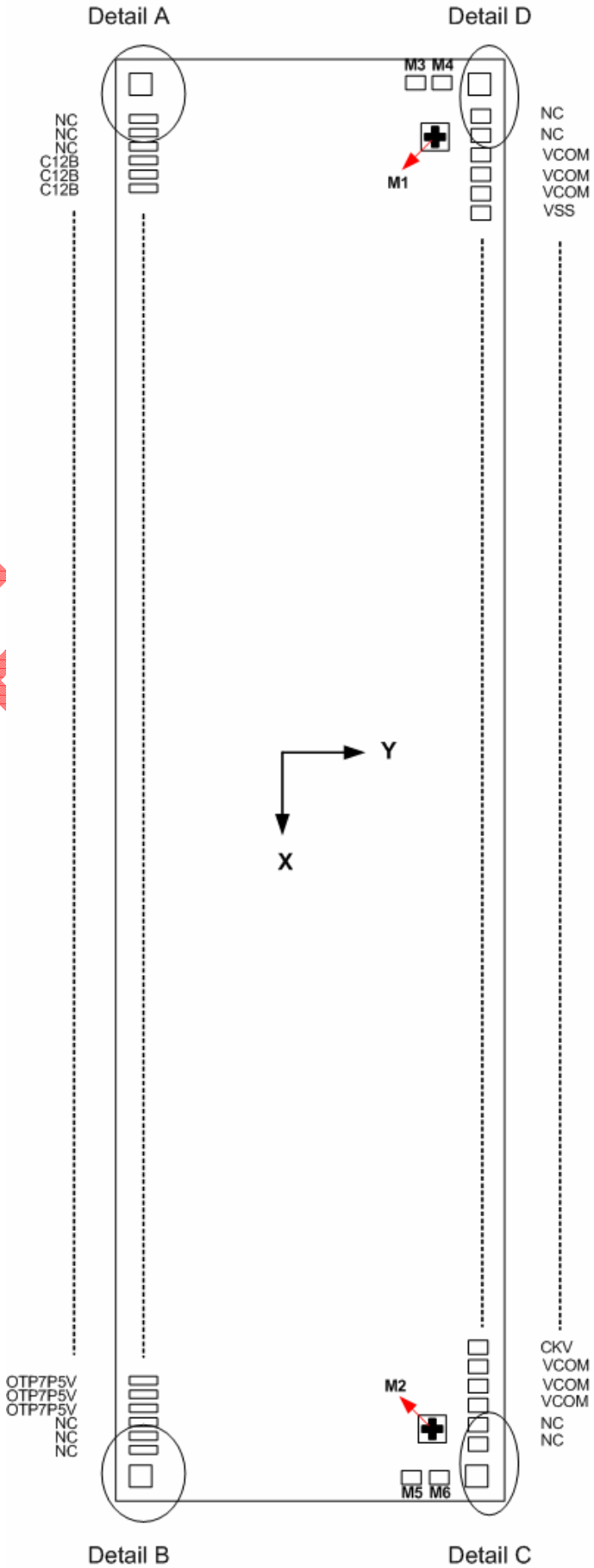
M6(3300，235)

-Dummy bump size

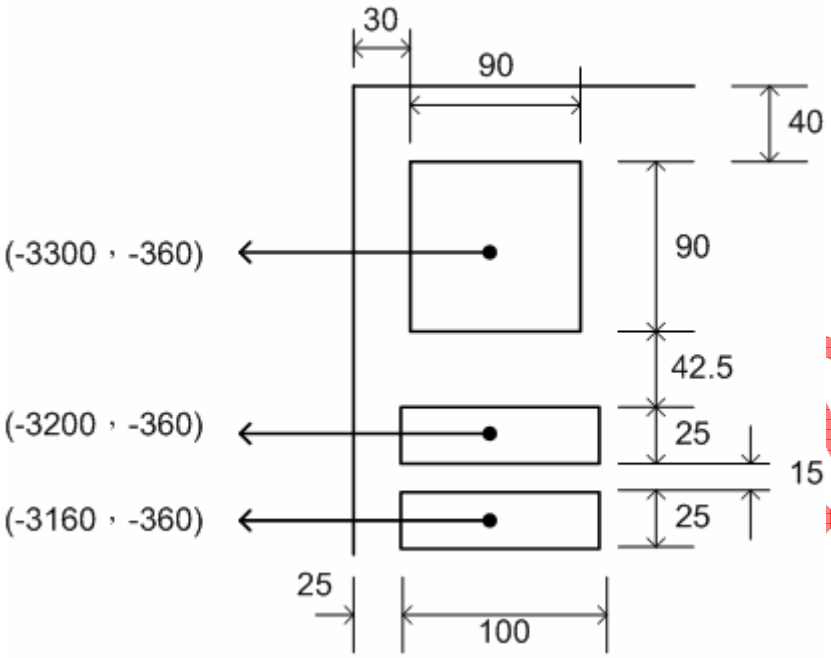
45 um x 63 um

Bump View

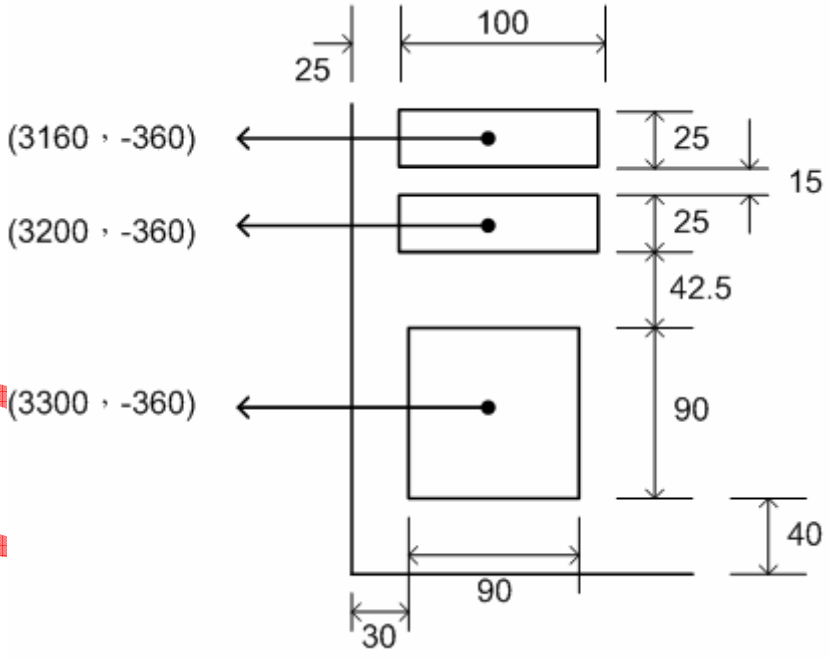




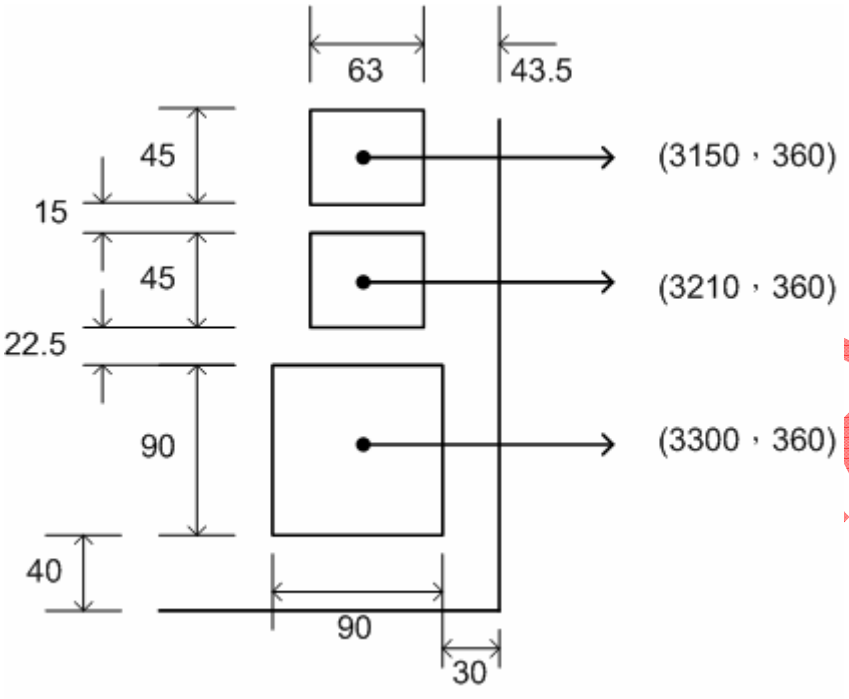
Detail A



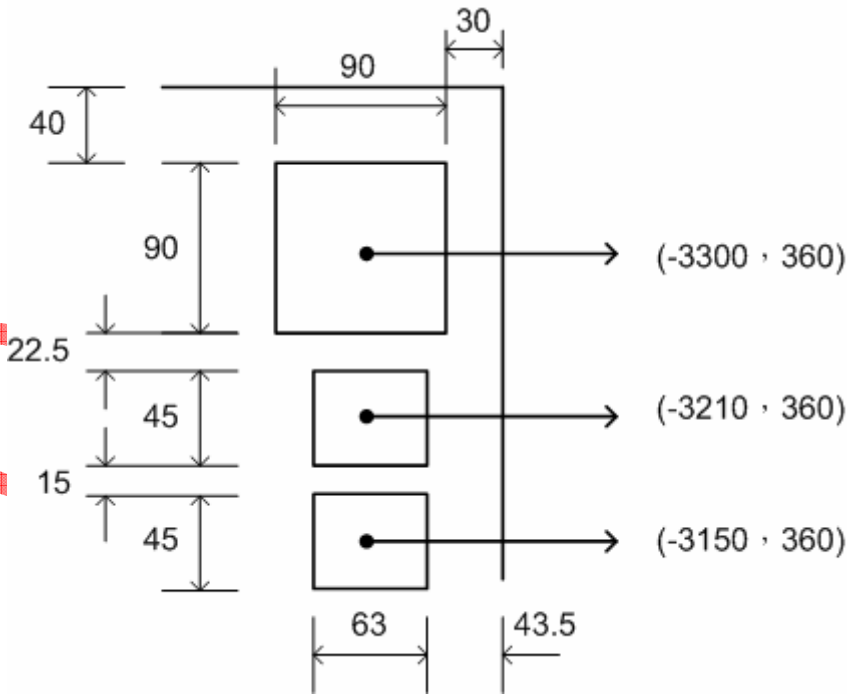
Detail B

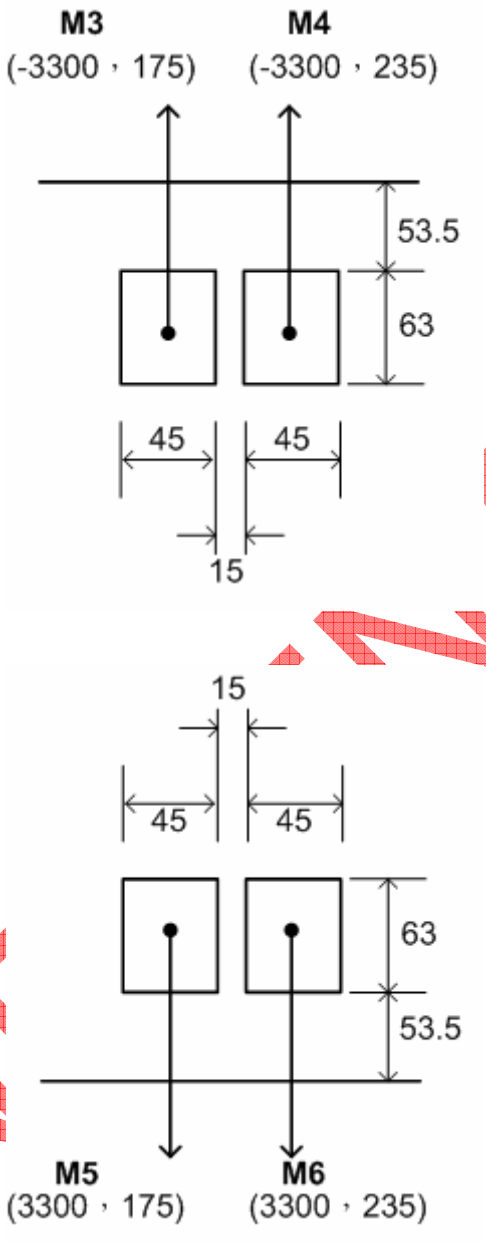


Detail C



Detail D





5.2 PAD COORDINATION

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	NC	-3200	-360	82	VSSOUT	40	-360
2	NC	-3160	-360	83	HOST1	80	-360
3	NC	-3120	-360	84	VDDIOOUT	120	-360
4	C12B	-3080	-360	85	HOST0	160	-360
5	C12B	-3040	-360	86	VSSOUT	200	-360
6	C12B	-3000	-360	87	AVDD3_SEL	240	-360
7	C12B	-2960	-360	88	VDDIO	280	-360
8	C12A	-2920	-360	89	SPI_nCS	320	-360
9	C12A	-2880	-360	90	SCK	360	-360
10	C12A	-2840	-360	91	SDI	400	-360
11	C12A	-2800	-360	92	SDO	440	-360
12	C13B	-2760	-360	93	VDDIO	480	-360
13	C13B	-2720	-360	94	VSS	520	-360
14	C13B	-2680	-360	95	MCLK	560	-360
15	C13A	-2640	-360	96	MCLK	600	-360
16	C13A	-2600	-360	97	nCS(DE)	640	-360
17	C13A	-2560	-360	98	nCS(DE)	680	-360
18	DUMMY	-2520	-360	99	nWR(R/W HS)	720	-360
19	DUMMY	-2480	-360	100	nWR(R/W HS)	760	-360
20	DUMMY	-2440	-360	101	nRD(E VS)	800	-360
21	AVDD1	-2400	-360	102	nRD(E VS)	840	-360
22	AVDD1	-2360	-360	103	RS	880	-360
23	AVDD1	-2320	-360	104	RS	920	-360
24	AVDD1	-2280	-360	105	TEST1	960	-360
25	VCOMH	-2240	-360	106	TEST2	1000	-360
26	VCOMH	-2200	-360	107	TEST3	1040	-360
27	VCOMH	-2160	-360	108	TEST4	1080	-360
28	VCOML	-2120	-360	109	TEST5	1120	-360
29	VCOML	-2080	-360	110	TEST6	1160	-360
30	VCOML	-2040	-360	111	VDDIO	1200	-360
31	AVDD2	-2000	-360	112	VDDIO	1240	-360
32	AVDD2	-1960	-360	113	RIN5[D17]	1280	-360
33	AVDD2	-1920	-360	114	RIN5[D17]	1320	-360
34	AVDD2	-1880	-360	115	RIN4[D16]	1360	-360
35	AVDD3	-1840	-360	116	RIN4[D16]	1400	-360
36	AVDD3	-1800	-360	117	RIN3[D15]	1440	-360
37	AVDD3	-1760	-360	118	RIN3[D15]	1480	-360
38	DVDD	-1720	-360	119	RIN2[D14]	1520	-360
39	DVDD	-1680	-360	120	RIN2[D14]	1560	-360
40	DVDD	-1640	-360	121	RIN1[D13]	1600	-360
41	DVDD	-1600	-360	122	RIN1[D13]	1640	-360
42	DUMMY	-1560	-360	123	RIN0[D12]	1680	-360
43	VDD2.8	-1520	-360	124	RIN0[D12]	1720	-360
44	VDD2.8	-1480	-360	125	GIN5[D11]	1760	-360
45	VDD2.8	-1440	-360	126	GIN5[D11]	1800	-360
46	DUMMY	-1400	-360	127	GIN4[D10]	1840	-360
47	VSS	-1360	-360	128	GIN4[D10]	1880	-360
48	VSS	-1320	-360	129	GIN3[D9]	1920	-360
49	VSS	-1280	-360	130	GIN3[D9]	1960	-360
50	VSS	-1240	-360	131	GIN2[D8]	2000	-360
51	VSS	-1200	-360	132	GIN2[D8]	2040	-360
52	VSS	-1160	-360	133	GIN1[D7]	2080	-360
53	VSS	-1120	-360	134	GIN1[D7]	2120	-360
54	VSS	-1080	-360	135	GIN0[D6]	2160	-360
55	VSS	-1040	-360	136	GIN0[D6]	2200	-360
56	VSS	-1000	-360	137	BIN5[D5]	2240	-360
57	VSS	-960	-360	138	BIN5[D5]	2280	-360

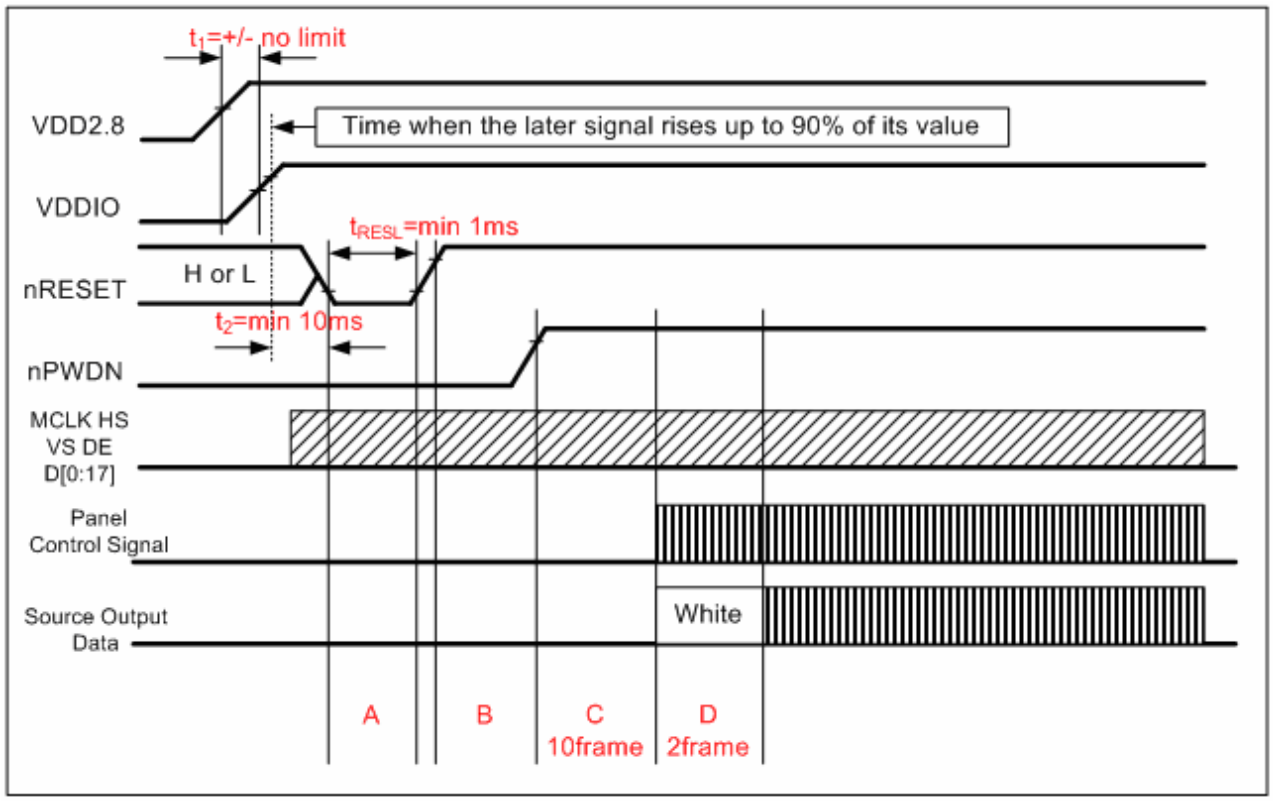
58	VSS	-920	-360	139	BIN4[D4]	2320	-360
59	DUMMY	-880	-360	140	BIN4[D4]	2360	-360
60	VDD2.8	-840	-360	141	BIN3[D3]	2400	-360
61	VDD2.8	-800	-360	142	BIN3[D3]	2440	-360
62	VDD2.8	-760	-360	143	BIN2[D2]	2480	-360
63	VDD2.8	-720	-360	144	BIN2[D2]	2520	-360
64	VDD2.8	-680	-360	145	BIN1[D1]	2560	-360
65	VDD2.8	-640	-360	146	BIN1[D1]	2600	-360
66	DUMMY	-600	-360	147	BIN0[D0]	2640	-360
67	DVDD	-560	-360	148	BIN0[D0]	2680	-360
68	DVDD	-520	-360	149	VDDIO	2720	-360
69	DVDD	-480	-360	150	VDDIO	2760	-360
70	VDDIO	-440	-360	151	VSS	2800	-360
71	VDDIO	-400	-360	152	VSS	2840	-360
72	VSS	-360	-360	153	VSS	2880	-360
73	VSS	-320	-360	154	RI	2920	-360
74	VSS	-280	-360	155	RI	2960	-360
75	nPWDN	-240	-360	156	OTP_7P5V	3000	-360
76	nPWDN	-200	-360	157	OTP_7P5V	3040	-360
77	nRESET	-160	-360	158	OTP_7P5V	3080	-360
78	nRESET	-120	-360	159	NC	3120	-360
79	VDDIO	-80	-360	160	NC	3160	-360
80	VDDIO	-40	-360	161	NC	3200	-360
81	VSSOUT	0	-360				

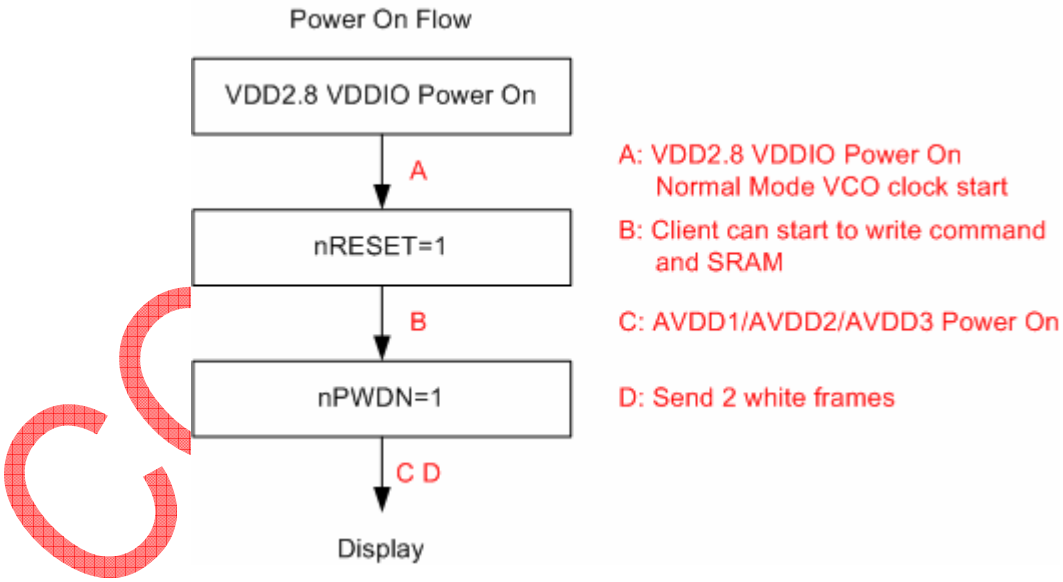
No.	Pin Name	X	Y	No.	Pin Name	X	Y
162	NC	3210	360	243	DO50	-1650	360
163	NC	3150	360	244	DO51	-1710	360
164	VCOM	3090	360	245	DO52	-1770	360
165	VCOM	3030	360	246	DO53	-1830	360
166	VCOM	2970	360	247	DO54	-1890	360
167	CKV	2910	360	248	DO55	-1950	360
168	STV1	2850	360	249	DO56	-2010	360
169	CSV	2790	360	250	DO57	-2070	360
170	ENBV	2730	360	251	DO58	-2130	360
171	CPCLK10	2670	360	252	DO59	-2190	360
172	CPCLK55	2610	360	253	DO60	-2250	360
173	XVDD	2550	360	254	DO61	-2310	360
174	XVDD	2490	360	255	DO62	-2370	360
175	VSS	2430	360	256	DO63	-2430	360
176	VSS	2370	360	257	DO64	-2490	360
177	CKH1	2310	360	258	DO65	-2550	360
178	CKH2	2250	360	259	Dummy	-2610	360
179	CKH3	2190	360	260	GAS	-2670	360
180	CKH4	2130	360	261	VC1	-2730	360
181	CKH5	2070	360	262	VC2	-2790	360
182	CKH6	2010	360	263	VSS	-2850	360
183	GAS	1950	360	264	VSS	-2910	360
184	DUMMY	1890	360	265	VCOM	-2970	360
185	DO00	1830	360	266	VCOM	-3030	360
186	DO01	1770	360	267	VCOM	-3090	360
187	DO02	1710	360	268	NC	-3150	360
188	DO03	1650	360	269	NC	-3210	360
189	DO04	1590	360				
190	DO05	1530	360				
191	DO06	1470	360				
192	DO07	1410	360				
193	DO08	1350	360				
194	DO09	1290	360				
195	DO10	1230	360				
196	DO11	1170	360				
197	DO12	1110	360				
198	DO13	1050	360				
199	DO14	990	360				
200	DO15	930	360				
201	DO16	870	360				
202	DO17	810	360				
203	DO18	750	360				
204	DO19	690	360				
205	DO20	630	360				
206	DO21	570	360				
207	DO22	510	360				
208	DO23	450	360				
209	DO24	390	360				
210	DO25	330	360				
211	DO26	270	360				
212	DO27	210	360				
213	DO28	150	360				
214	DO29	90	360				
215	DO30	30	360				
216	DO31	-30	360				
217	DO32	-90	360				
218	DUMMY	-150	360				
219	DUMMY	-210	360				

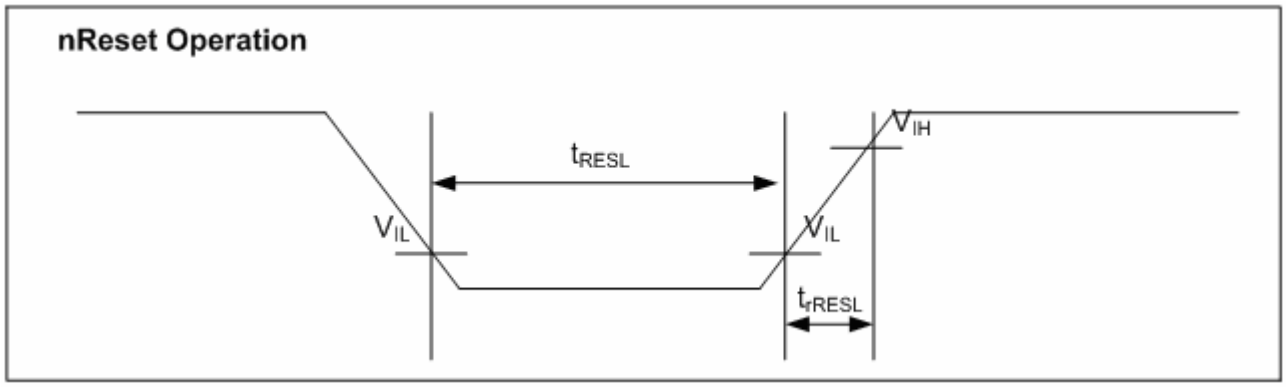
220	DUMMY	-270	360				
221	DUMMY	-330	360				
222	DUMMY	-390	360				
223	DUMMY	-450	360				
224	DUMMY	-510	360				
225	DUMMY	-570	360				
226	DO33	-630	360				
227	DO34	-690	360				
228	DO35	-750	360				
229	DO36	-810	360				
230	DO37	-870	360				
231	DO38	-930	360				
232	DO39	-990	360				
233	DO40	-1050	360				
234	DO41	-1110	360				
235	DO42	-1170	360				
236	DO43	-1230	360				
237	DO44	-1290	360				
238	DO45	-1350	360				
239	DO46	-1410	360				
240	DO47	-1470	360				
241	DO48	-1530	360				
242	DO49	-1590	360				

6. POWER ON/OFF SEQUENCE

6.1 POWER ON SEQUENCE



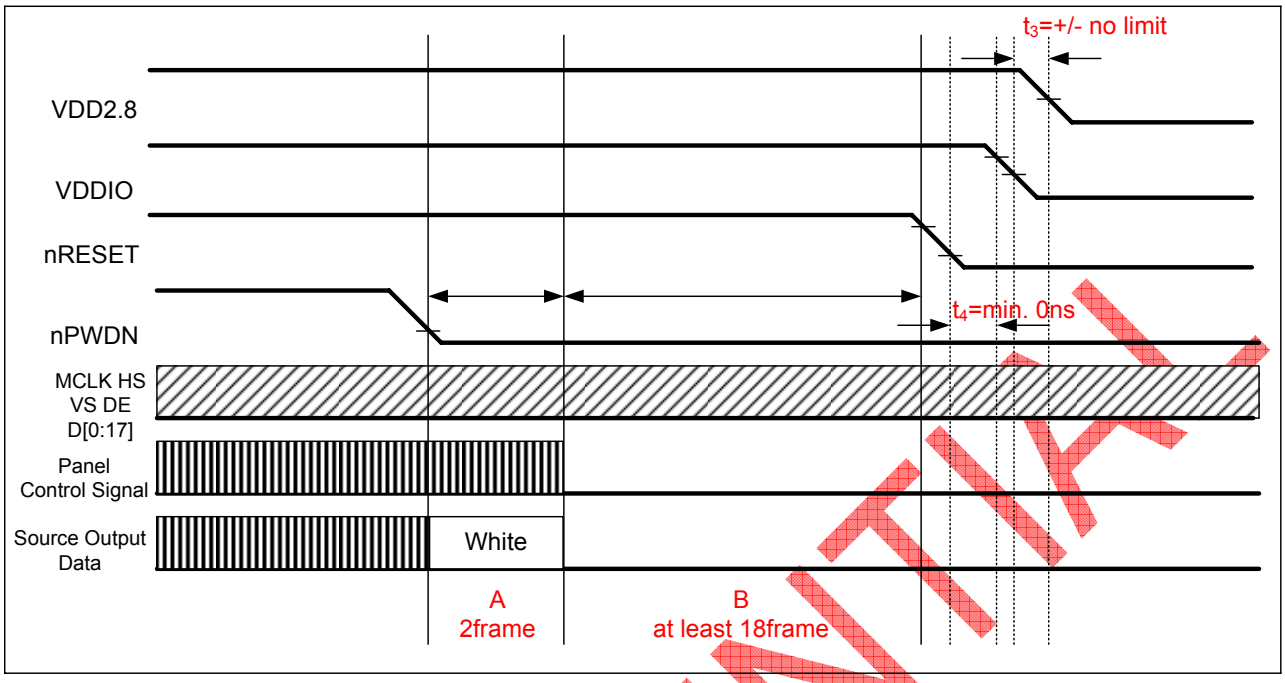


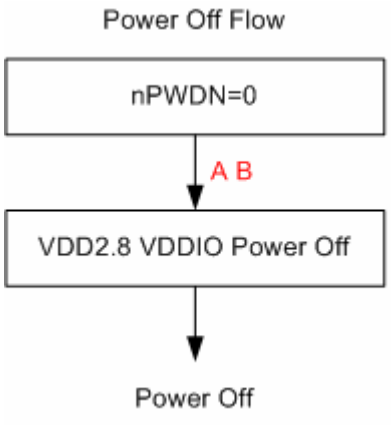


VDDIO=1.6 to 3.3 V

Item	Symbol	Min	Typ	Max	unit
nReset low width	t_{RESL}	1	–	–	ms
nReset rising time	t_{rRESL}	–	–	100	ns

6.2 POWER OFF SEQUENCE





A: Send 2 white frames

B: Control signal & source output stop
AVDD1/AVDD2/AVDD3 Power off
VDD2.8 VDDIO Power Off

7. GAMMA VOLTAGE MAPPING

The γ-adjustment is controlled by a group of registers to set an appropriate grayscale voltage for the γ-characteristics of a liquid crystal panel. The grayscale voltage is adjusted by the ladder resistors and user can use nine 4-bit registers to set the nine points of gamma curve.AVDD3_SEL is used to select Gamma Voltage Table.

Gamma Voltage Table1(3.8V Vlc)					
Gray Level	PV	NV	Gray Level	PV	NV
0	4.40	0.50	32	2.57	2.33
1	4.30	0.60	33	2.54	2.36
2	4.10	0.80	34	2.52	2.38
3	3.94	0.96	35	2.50	2.40
4	3.81	1.09	36	2.48	2.42
5	3.70	1.20	37	2.45	2.45
6	3.60	1.30	38	2.43	2.47
7	3.51	1.39	39	2.41	2.49
8	3.43	1.47	40	2.39	2.51
9	3.35	1.55	41	2.37	2.53
10	3.29	1.61	42	2.35	2.55
11	3.23	1.67	43	2.33	2.57
12	3.17	1.73	44	2.31	2.59
13	3.12	1.78	45	2.29	2.61
14	3.08	1.82	46	2.27	2.63
15	3.04	1.86	47	2.25	2.65
16	3.00	1.90	48	2.22	2.68
17	2.96	1.94	49	2.20	2.70
18	2.92	1.98	50	2.18	2.72
19	2.89	2.01	51	2.15	2.75
20	2.86	2.04	52	2.13	2.77
21	2.83	2.07	53	2.10	2.80
22	2.81	2.09	54	2.07	2.83
23	2.78	2.12	55	2.04	2.86
24	2.75	2.15	56	2.01	2.89
25	2.73	2.17	57	1.97	2.93
26	2.71	2.19	58	1.93	2.97
27	2.68	2.22	59	1.88	3.02
28	2.66	2.24	60	1.82	3.08
29	2.63	2.27	61	1.68	3.22
30	2.61	2.29	62	1.43	3.47
31	2.59	2.31	63	1.10	3.80

Gamma Voltage Table2(3.3V Vlc)					
Gary Level	PV	NV	Gary Level	PV	NV
0	3.912	1.118	32	2.384	2.646
1	3.881	1.149	33	2.366	2.664
2	3.781	1.249	34	2.347	2.683
3	3.661	1.369	35	2.329	2.701
4	3.525	1.505	36	2.310	2.720
5	3.410	1.620	37	2.293	2.737
6	3.311	1.719	38	2.274	2.756
7	3.224	1.806	39	2.256	2.774
8	3.150	1.880	40	2.238	2.792
9	3.084	1.946	41	2.220	2.810
10	3.026	2.004	42	2.201	2.829
11	2.973	2.057	43	2.182	2.848
12	2.927	2.103	44	2.163	2.867
13	2.885	2.145	45	2.144	2.886
14	2.846	2.184	46	2.125	2.905
15	2.811	2.219	47	2.106	2.924
16	2.777	2.253	48	2.086	2.944
17	2.745	2.285	49	2.066	2.964
18	2.714	2.316	50	2.045	2.985
19	2.685	2.345	51	2.025	3.005
20	2.657	2.373	52	2.003	3.027
21	2.630	2.400	53	1.980	3.050
22	2.603	2.427	54	1.956	3.074
23	2.578	2.452	55	1.929	3.101
24	2.554	2.476	56	1.899	3.131
25	2.530	2.500	57	1.867	3.163
26	2.507	2.523	58	1.830	3.200
27	2.486	2.544	59	1.787	3.243
28	2.464	2.566	60	1.733	3.297
29	2.443	2.587	61	1.623	3.407
30	2.423	2.607	62	1.374	3.656
31	2.403	2.627	63	1.112	3.918

9. INPUT INTERFACE SELECTION

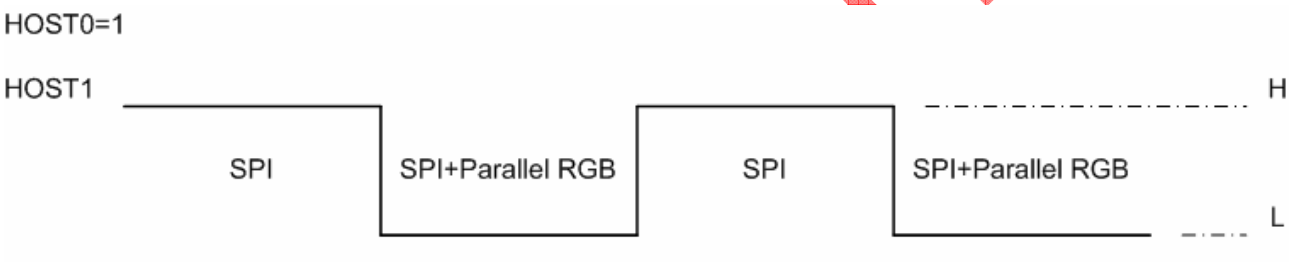
C1L5-06 provides plentiful input interfaces for the display memory and register access which include 8/16/9/18-bit CPU interface, parallel RGB interface and SPI interfaces. User can base on the available system architecture to select a suitable input interface to read/write the control registers and display memory. The input mode selection is determined by the HOST[1:0] pins.

HOST1	HOST0	Designation
0	0	8080-series system
1	0	6800-series system
0	1	Parallel RGB with 3-wires SPI
1	1	3-wires SPI

9.1 Interface switches between SPI and Parallel RGB

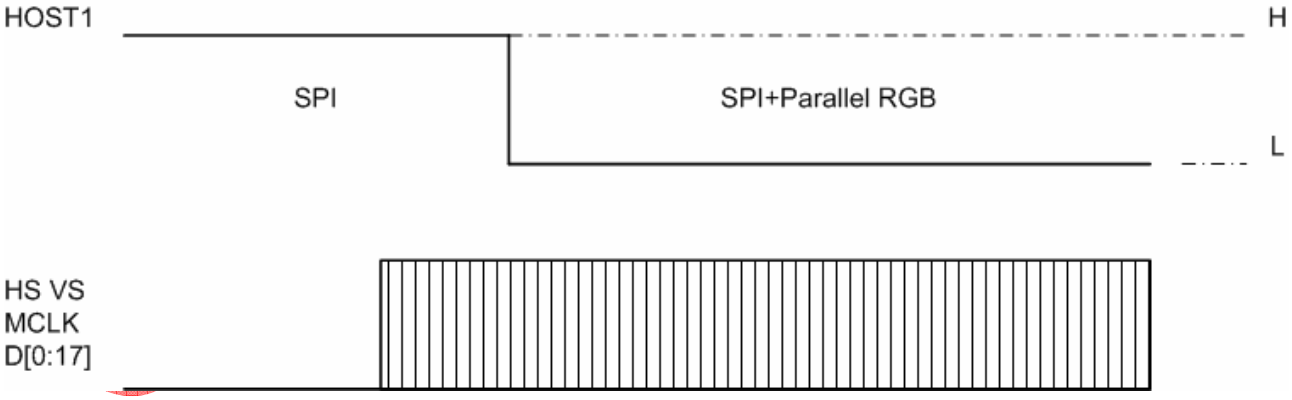
9.1.1.How to Switch

We use HOST1 to switch. HOST0 will be pulled high on FPC and HOST1 is controlled by HOST side.



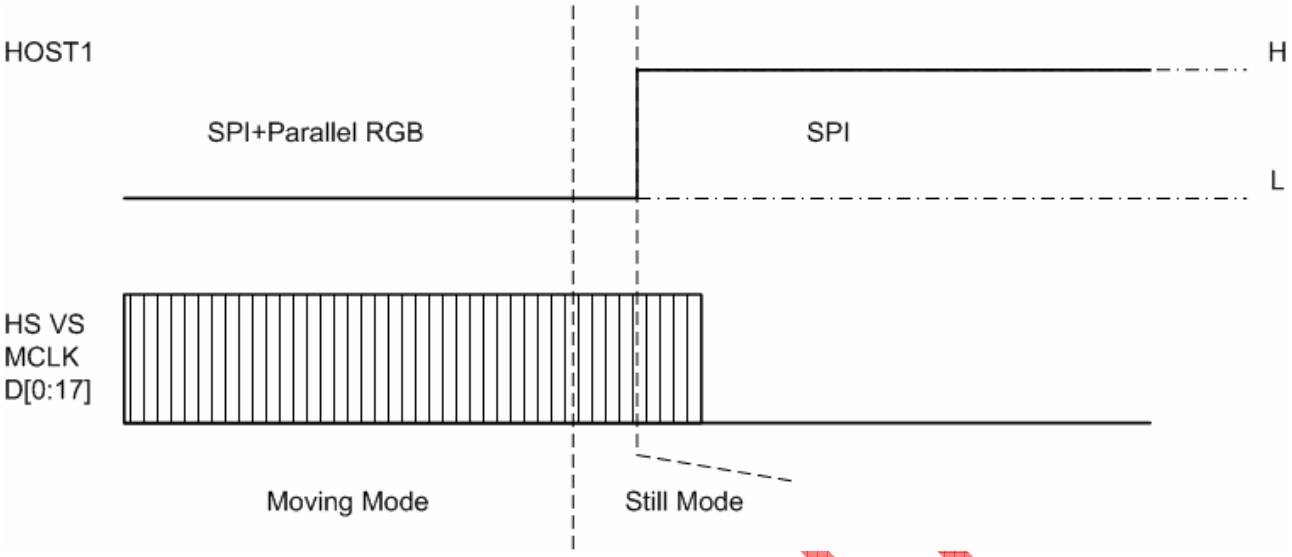
9.1.2 SPI switches to Parallel RGB

Parallel RGB transfer timing need to start to work before HOST1 goes to low state.



9.1.3 Parallel RGB switches to SPI

We must to change to still mode before HOST1 goes to high state.

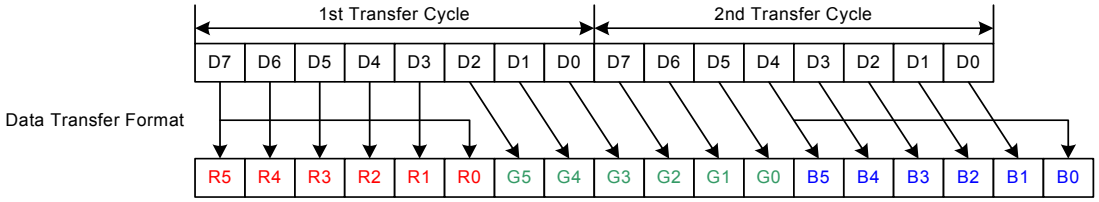


10. CPU INTERFACE

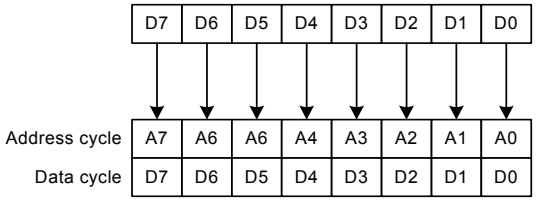
10.1 8-bit CPU INTERFACE MODE

8-Bit Bus Width CPU interface

Memory Access:

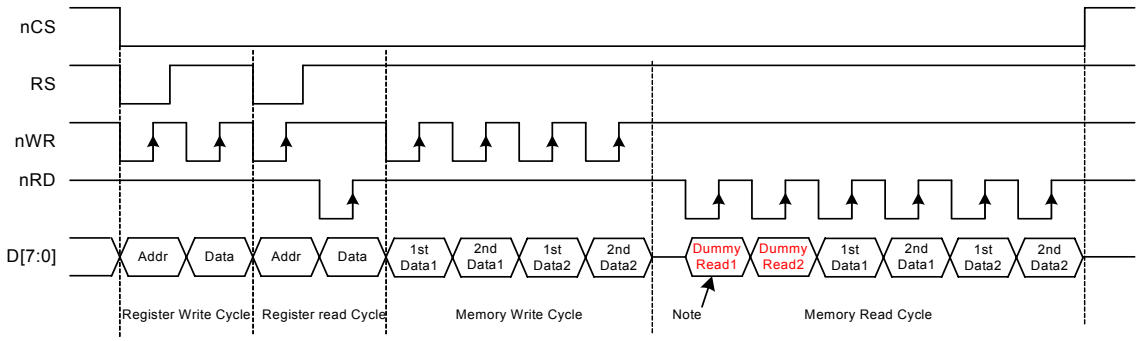


Register Access:

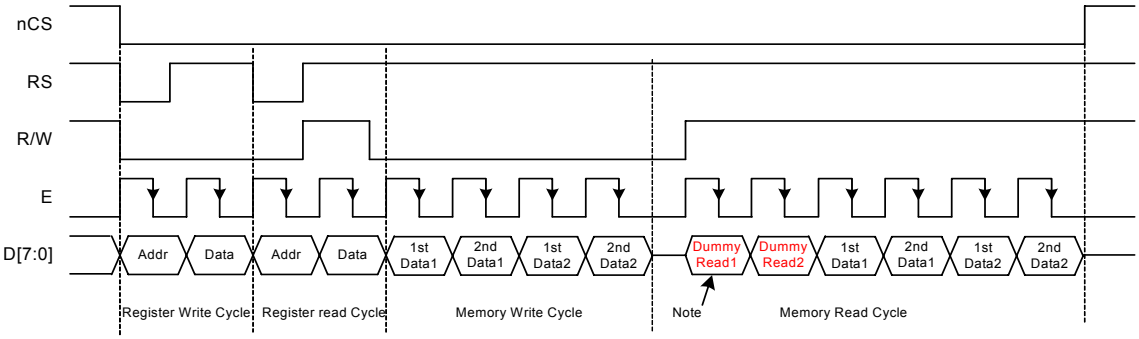


Timing Waveform

Example: i80 CPU



Example: M68 CPU

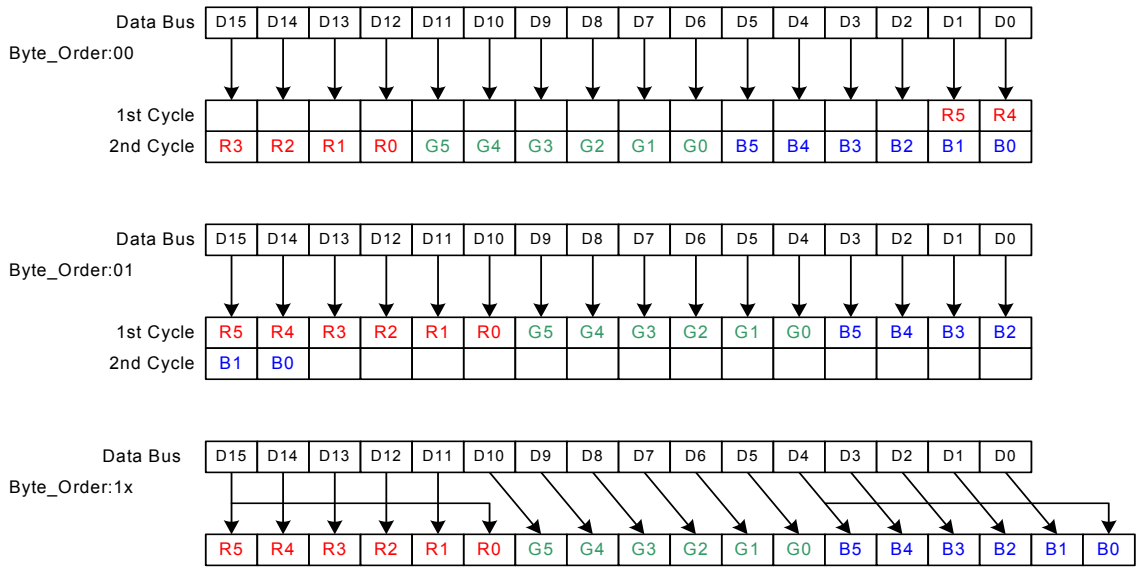


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

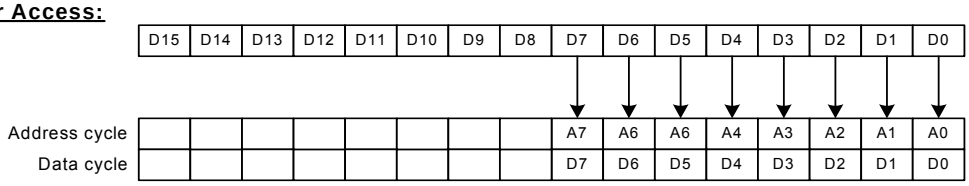
10.2 16-bit CPU INTERFACE MODE

16-Bit Bus Width CPU interface

Memory Access:

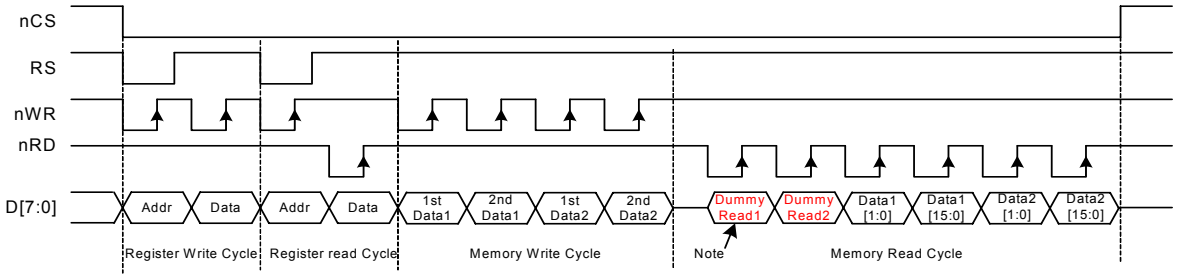


Register Access:

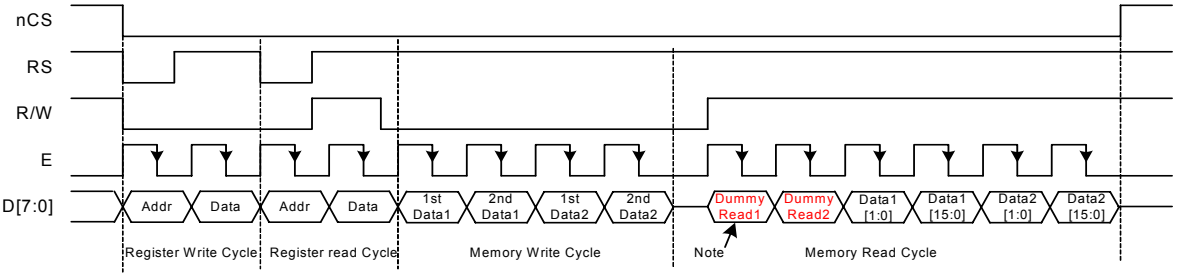


Timing Waveform

Example: i80 CPU, 16-bit, Byte Order=00

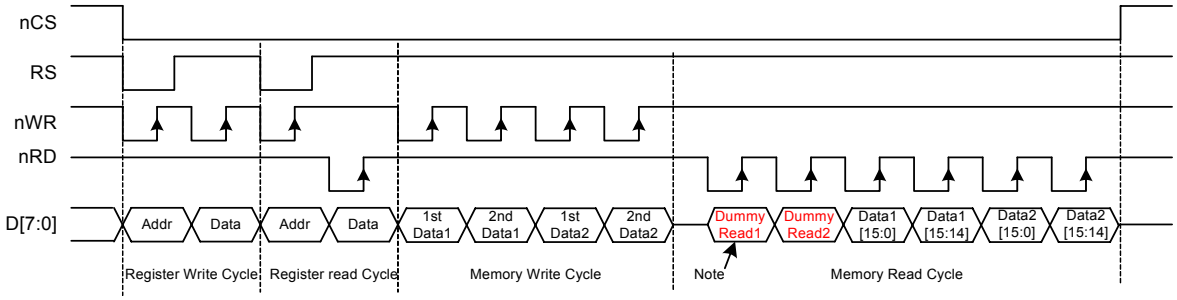


Example: M68 CPU, 16-bit, Byte Order=00

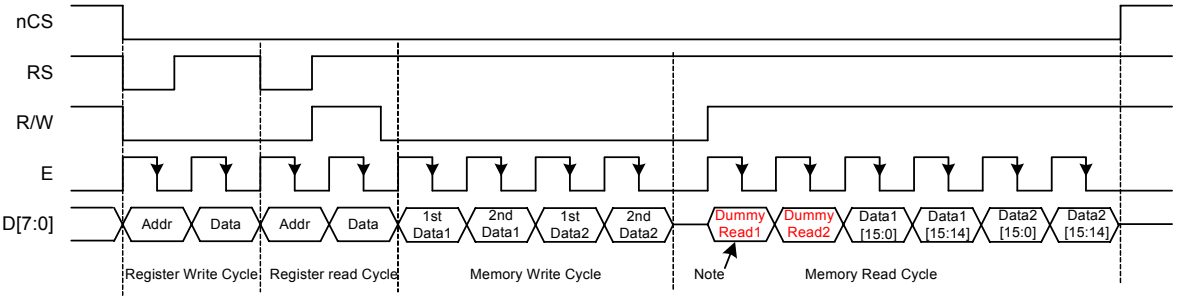


Timing Waveform

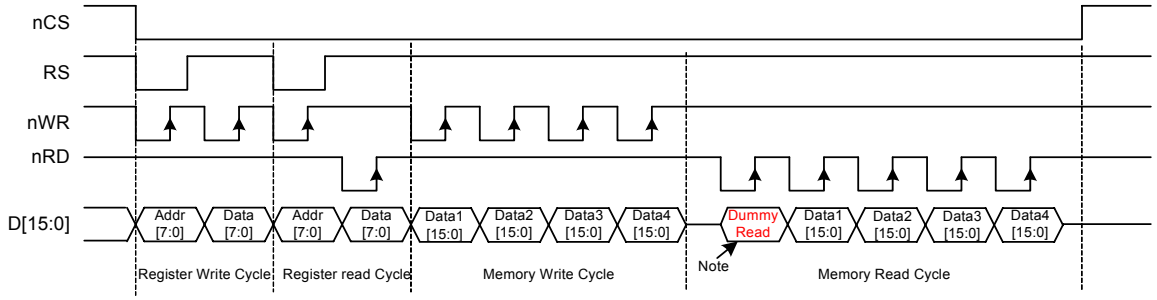
Example: i80 CPU, 16-bit, Byte_Order=01



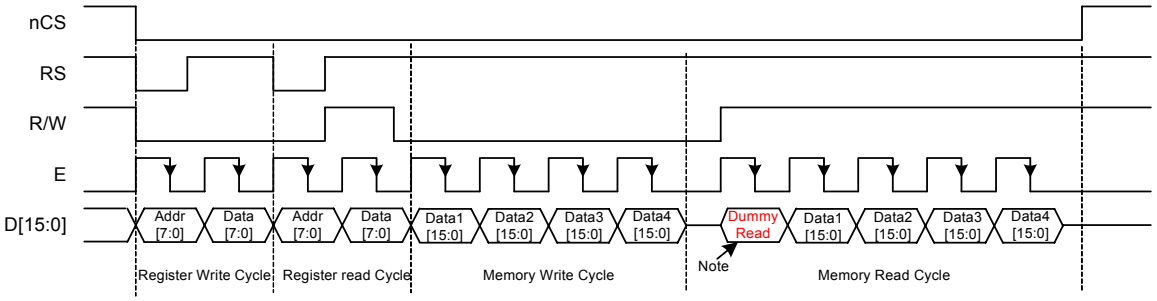
Example: M68 CPU, 16-bit, Byte_Order=01



Example: i80 CPU, 16bit, Byte_Order=1x



Example: M68 CPU, 16-bit, Byte_Order=1x

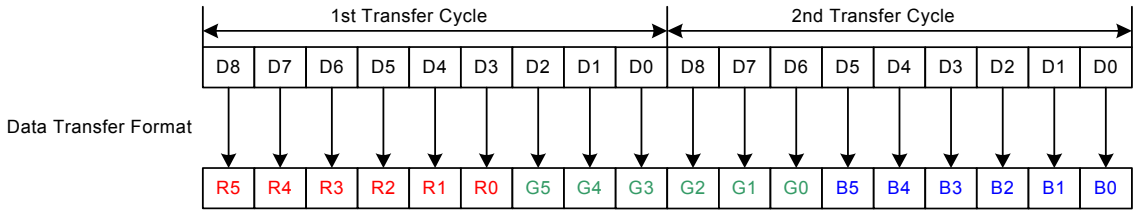


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

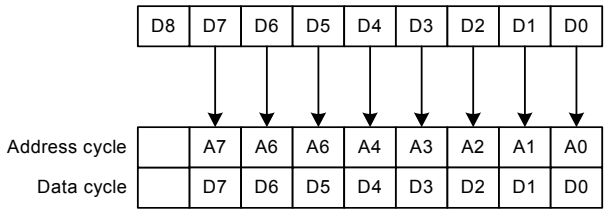
10.3 9-bit CPU INTERFACE MODE

9-Bit Bus Width CPU interface

Memory Access:

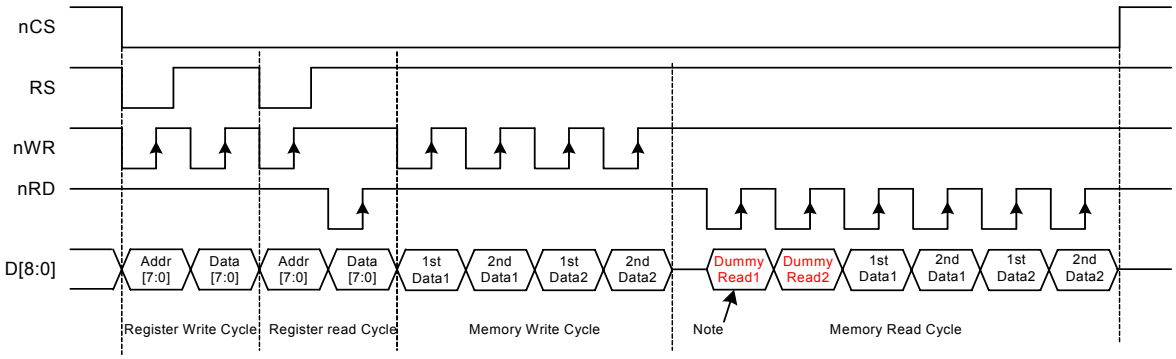


Register Access:

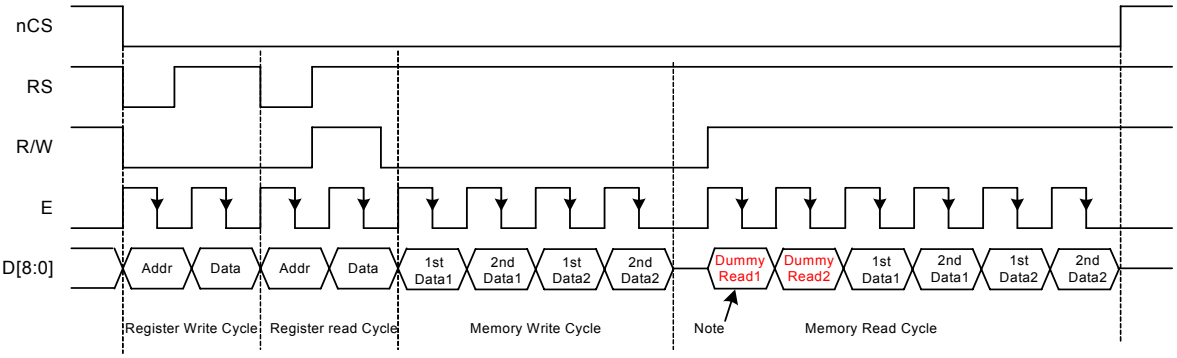


Timing Waveform

Example: i80 CPU



Example: M68 CPU

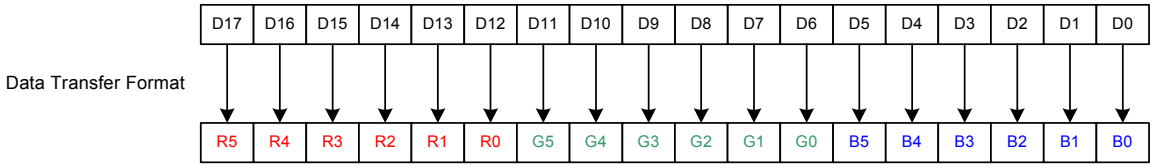


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

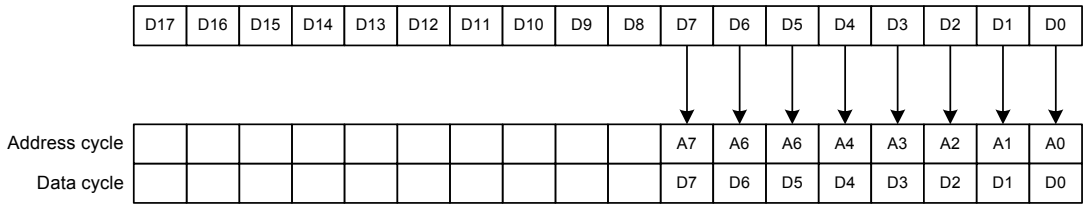
10.4 18-bit CPU INTERFACE MODE

18-Bit Bus Width CPU interface

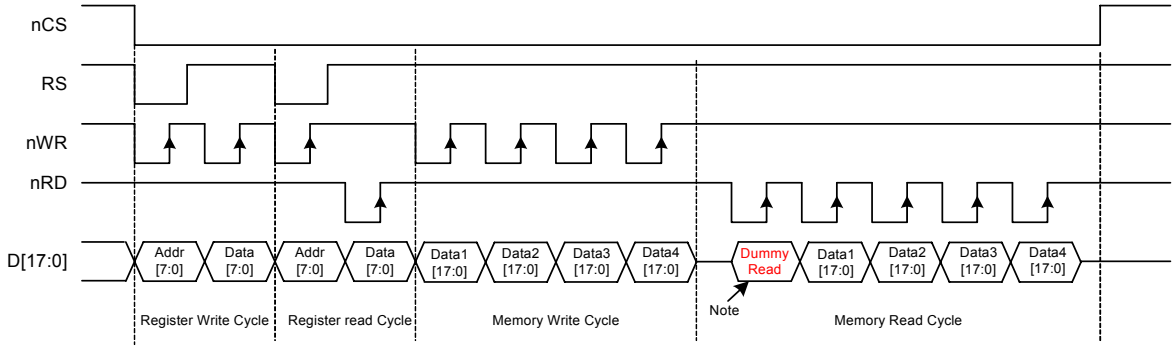
Memory Access:



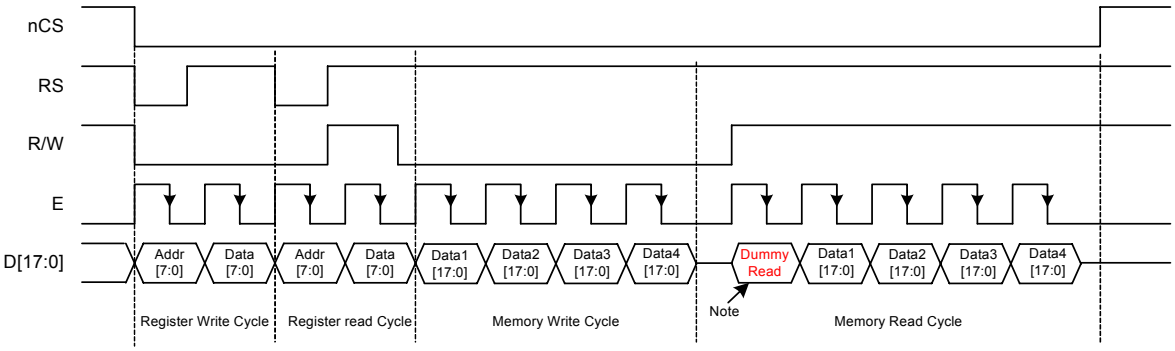
Register Access:



Example: i80 CPU

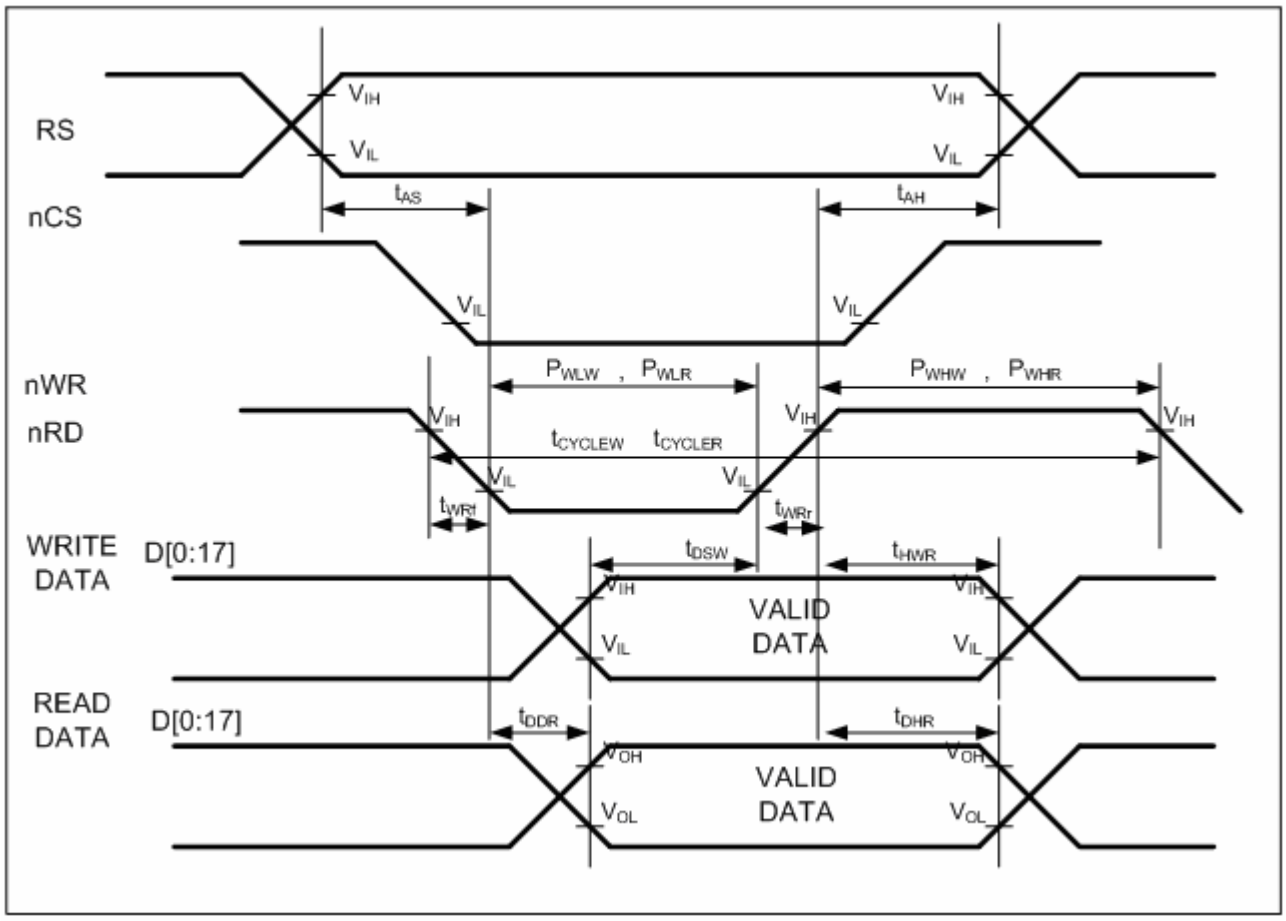


Example: M68 CPU



Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

10.5 i80 CPU INPUT TIMING



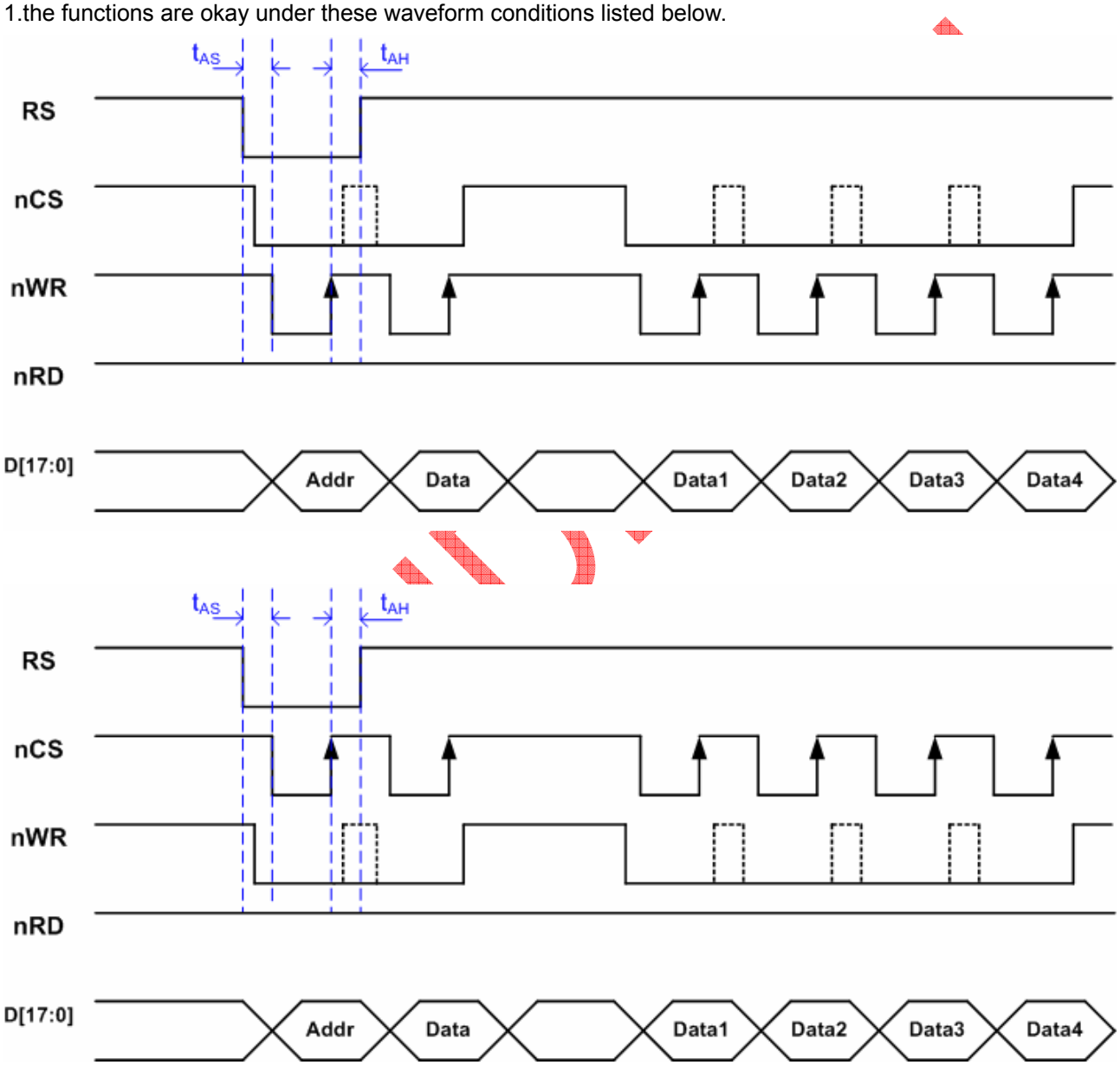
Normal Write Mode(18/16/9/8-Bit Interface): VDDIO=1.6 to 3.3 V

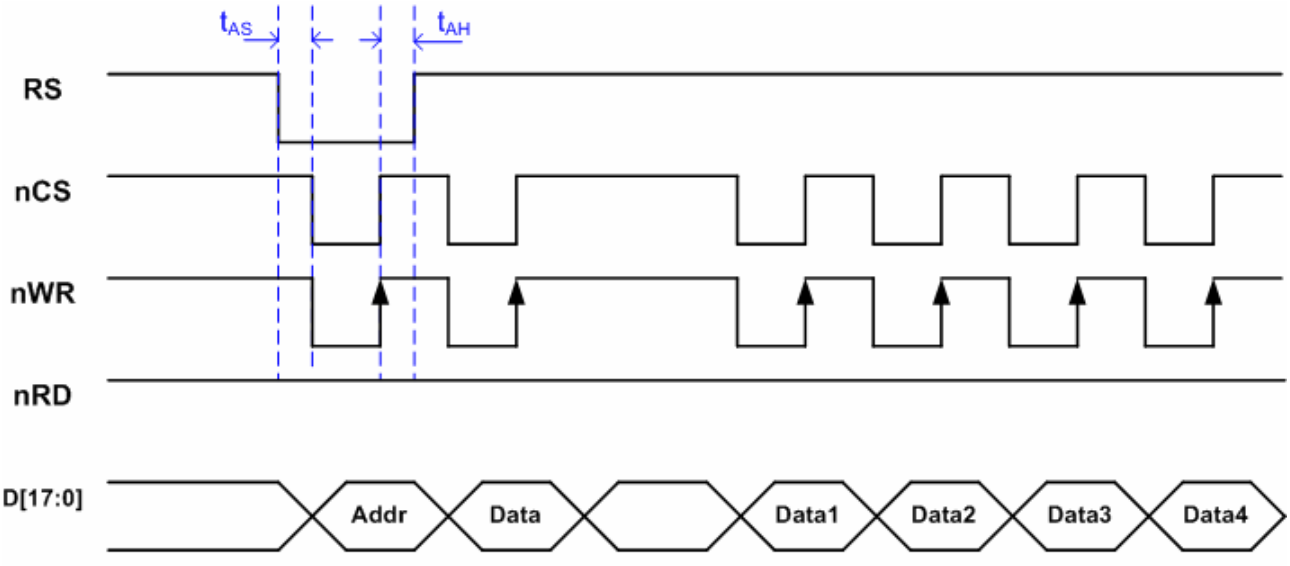
Item	Symbol	Min	Typ	Max	unit
Bus cycle time	t_{CYCLEW}	100	–	–	ns
	t_{CYCLER}	200	–	–	ns
nWR_nRD pulse width low	P_{WLW}	20	–	–	ns
	P_{WLR}	40	–	–	ns
nWR_nRD pulse width high	P_{WHW}	20	–	–	ns
	P_{WHR}	40			
Pulse rise/fall time	t_{WRr}, t_{WRf}	–	–	25	ns
Setup time(RS,nCS,nWR,nRD)	t_{AS}	0	–	–	ns
Hold time(RS,nCS,nWR,nRD)	t_{AH}	2	–	–	ns
Data setup time	t_{DSW}	25	–	–	ns
Data hold time	t_{HWR}	5	–	–	ns
Data output setup time	t_{DDR}	–	–	200	ns
Data output hold time	t_{DHR}	5	–	–	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input signal	V_{IH}		0.8*VDDIO	-	VDDIO	Volt
	V_{IL}		GND	-	VDDIO*0.2	Volt
Output signal	V_{OH}	I_{OH}=-0.1mA	VDDIO-0.5	-	VDDIO	Volt
	V_{OL}	I_{OL}=0.1mA	GND	-	0.5	Volt

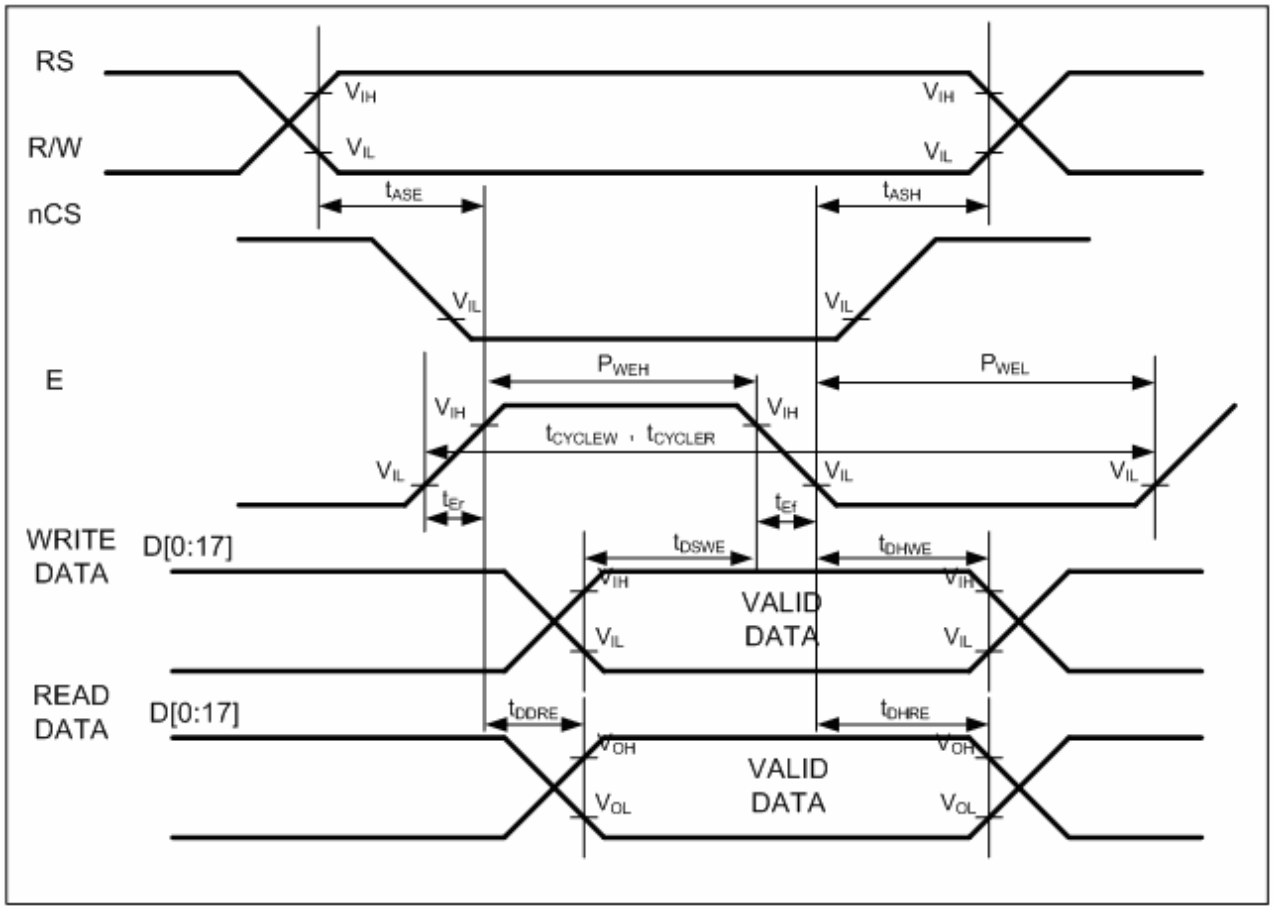
Note :

1.the functions are okay under these waveform conditions listed below.





10.6 M68 CPU Input Timing

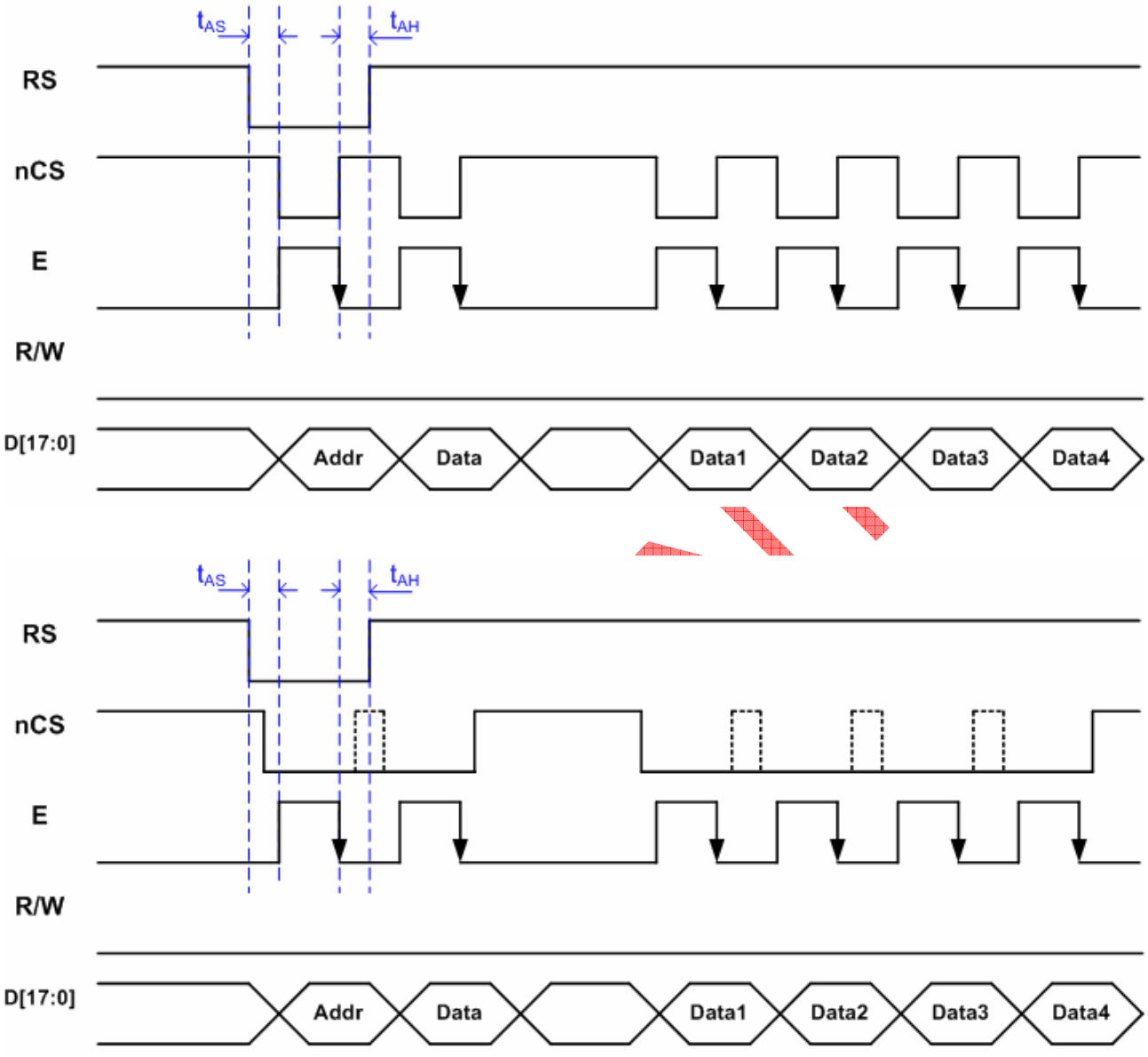


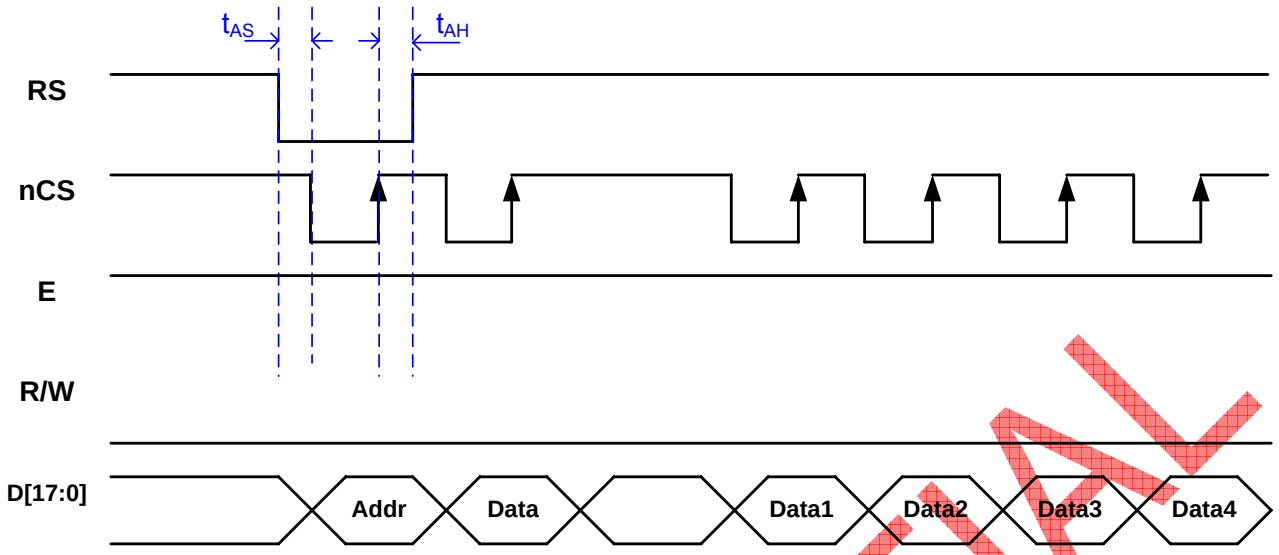
Normal Write Mode(18/16/9/8-Bit Interface): VDDIO=1.6 to 3.3 V

Item		Symbol	Min	Typ	Max	unit
Bus cycle time	write	t_{CYCLEW}	100	–	–	ns
	read	t_{CYCLER}	200	–	–	ns
E pulse width low	write	P_{WEL}	20	–	–	ns
	read		40	–	–	ns
E pulse width high	write	P_{WEH}	20	–	–	ns
	read		40			
E Pulse rise/fall time		t_{Er}, t_{Ef}	–	–	25	ns
Setup time(RS,nCS,E,R/W)		t_{ASE}	0	–	–	ns
Hold time(RS,nCS,E,R/W)		t_{ASH}	2	–	–	ns
Data setup time		t_{DSWE}	25	–	–	ns
Data hold time		t_{DHWE}	5	–	–	ns
Data output setup time		tDDR	–	–	200	ns
Data output hold time		tDHR	5	–	–	ns

Note :

1.the functions of E and R/W are okay under these waveform conditions list below.





10.7 SRAM ADDRESS for RGB DATABASE

The display data is written into TP0XX embedded display memory by the CPU or RGB interface. In the RGB interface mode, only the data of moving picture area is needed to be transmitted to update the display image and also reduce the power consumption. When writing the display memory, the memory address counter can increase/decrease automatically by setting SRAM _Control register. The relative registers of display memory access are listed in the following table.

The PWS_X and PWS_Y registers set the start address of memory access window, and PWE_X and PWE_Y registers set the end address of memory window. The SRAM_Position_X and SRAM_Position_Y registers are the address counters, which will increase automatically for each memory read or write. For example, if the panel resolution is set to 96 x 96, the SRAM_Position_X is reset to zero when it count to 95, and the SRAM_Position_Y increases one automatically.

Registers Table of Display Memory Access Setting	
PWS_X	X-axis start address of display window for memory access
PWS_Y	Y-axis start address of display window for memory access
PWE_X	X-axis end address of display window for memory access
PWE_Y	Y-axis end address of display window for memory access
SRAM_Position_X	X-axis addressing register for memory access.
SRAM_Position_Y	Y-axis addressing register for memory access.

10.7.1 132 × 160 Mode

Line No.	R0	G0	B0	R1	G1	B1	.....	R130	G130	B130	R131	G131	B131
	D17.....D0			D17.....D0				D17.....D0			D17.....D0		
L1	“0000”H			“0001”H			.....	“0082”H			“0083”H		
L2	“0100”H			“0101”H			.....	“0182”H			“0183”H		
L3	“0200”H			“0201”H			.....	“0282”H			“0283”H		
L4	“0300”H			“0301”H			.....	“0382”H			“0383”H		
L5	“0400”H			“0401”H			.....	“0482”H			“0483”H		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	.....	⋮	⋮	⋮	⋮	⋮	⋮
L155	“9A00”H			“9A01”H			.....	“9A82”H			“9A83”H		
L156	“9B00”H			“9B01”H			.....	“9B82”H			“9B83”H		
L157	“9C00”H			“9C01”H			.....	“9C82”H			“9C83”H		
L158	“9D00”H			“9D01”H			.....	“9D82”H			“9D83”H		
L159	“9E00”H			“9E01”H			.....	“9E82”H			“9E83”H		
L160	“9F00”H			“9F01”H			.....	“9F82”H			“9F83”H		

10.7.2 128 × 160 Mode

Line No.	R0	G0	B0	R1	G1	B1	.....	R126	G126	B126	R127	G127	B127
	D17.....D0			D17.....D0				D17.....D0			D17.....D0		
L1	"0000"H			"0001"H			.....	"007E"H			"007F"H		
L2	"0100"H			"0101"H			.....	"017E"H			"017F"H		
L3	"0200"H			"0201"H			.....	"027E"H			"027F"H		
L4	"0300"H			"0301"H			.....	"037E"H			"037F"H		
L5	"0400"H			"0401"H			.....	"047E"H			"047F"H		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	.....	⋮	⋮	⋮	⋮	⋮	⋮
L155	"9A00"H			"9A01"H			.....	"9A7E"H			"9A7F"H		
L156	"9B00"H			"9B01"H			.....	"9B7E"H			"9B7F"H		
L157	"9C00"H			"9C01"H			.....	"9C7E"H			"9C7F"H		
L158	"9D00"H			"9D01"H			.....	"9D7E"H			"9D7F"H		
L159	"9E00"H			"9E01"H			.....	"9E7E"H			"9E7F"H		
L160	"9F00"H			"9F01"H			.....	"9F7E"H			"9F7F"H		

10.7.3 128 × 128 Mode

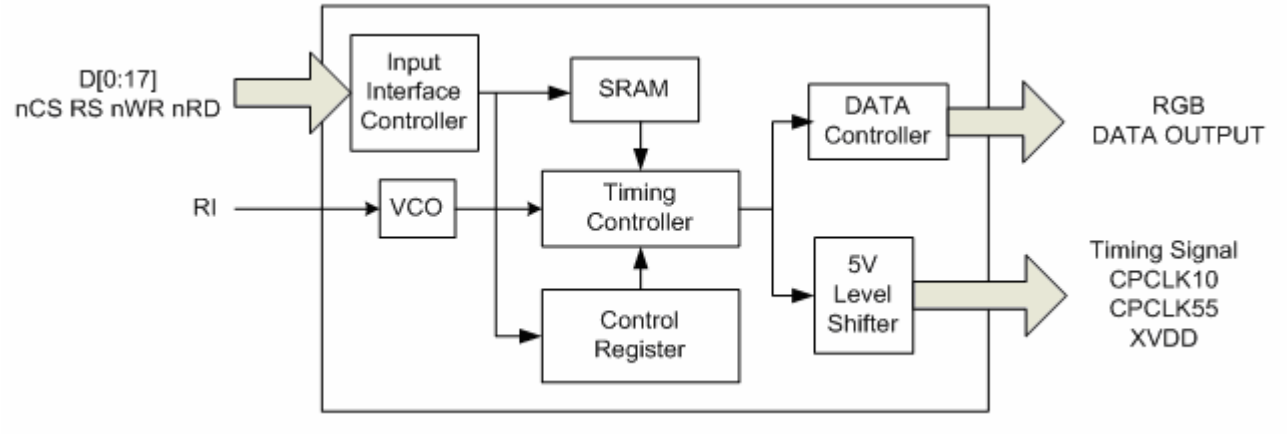
Line No.	R0	G0	B0	R1	G1	B1	.....	R126	G126	B126	R127	G127	B127
	D17.....D0			D17.....D0				D17.....D0			D17.....D0		
L1	"0000"H			"0001"H			.....	"007E"H			"007F"H		
L2	"0100"H			"0101"H			.....	"017E"H			"017F"H		
L3	"0200"H			"0201"H			.....	"027E"H			"027F"H		
L4	"0300"H			"0301"H			.....	"037E"H			"037F"H		
L5	"0400"H			"0401"H			.....	"047E"H			"047F"H		
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
L123	"7A00"H			"7A01"H			.....	"7A7E"H			"7A7F"H		
L124	"7B00"H			"7B01"H			.....	"7B7E"H			"7B7F"H		
L125	"7C00"H			"7C01"H			.....	"7C7E"H			"7C7F"H		
L126	"7D00"H			"7D01"H			.....	"7D7E"H			"7D7F"H		
L127	"7E00"H			"7E01"H			.....	"7E7E"H			"7E7F"H		
L128	"7F00"H			"7F01"H			.....	"7F7E"H			"7F7F"H		

10.7.4 96 × 96 Mode

Line No.	R0	G0	B0	R1	G1	B1	…….	R94	G94	B94	R95	G95	B95
	D17……D0			D17……D0				D17……D0			D17……D0		
L1	“0000”H			“0001”H			…….	“005E”H			“005F”H		
L2	“0100”H			“0101”H			…….	“015E”H			“015F”H		
L3	“0200”H			“0201”H			…….	“025E”H			“025F”H		
L4	“0300”H			“0301”H			…….	“035E”H			“035F”H		
L5	“0400”H			“0401”H			…….	“045E”H			“045F”H		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
L91	“5A00”H			“5A01”H			…….	“5A5E”H			“5A5F”H		
L92	“5B00”H			“5B01”H			…….	“5B5E”H			“5B5F”H		
L93	“5C00”H			“5C01”H			…….	“5C5E”H			“5C5F”H		
L94	“5D00”H			“5D01”H			…….	“5D5E”H			“5D5F”H		
L95	“5E00”H			“5E01”H			…….	“5E5E”H			“5E5F”H		
L96	“5F00”H			“5F01”H			…….	“5F5E”H			“5F5F”H		

10.8 DISPLAY MODE FUNCTION BLOCK DIAGRAM

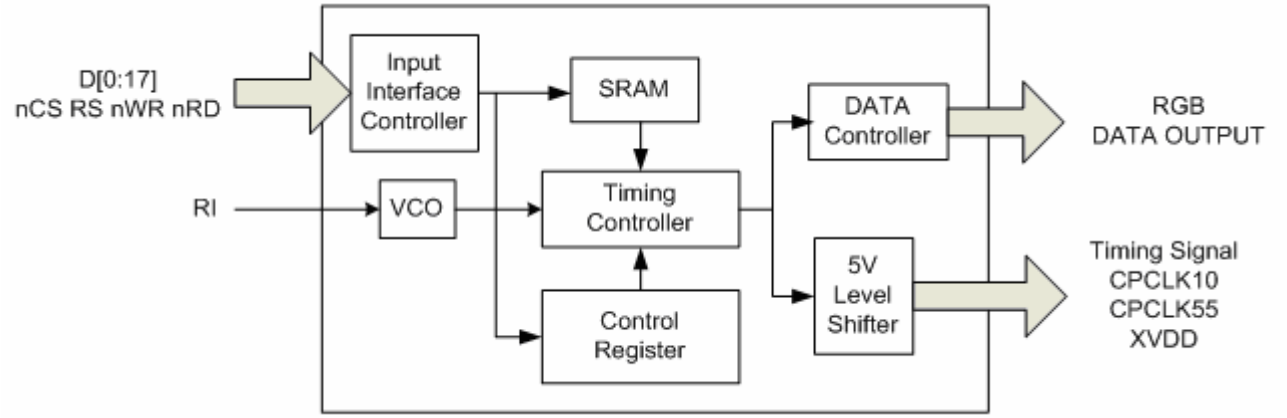
10.8.1 Normal Mode



Note:

1. CPCLK10、PCLK55、XVDD output

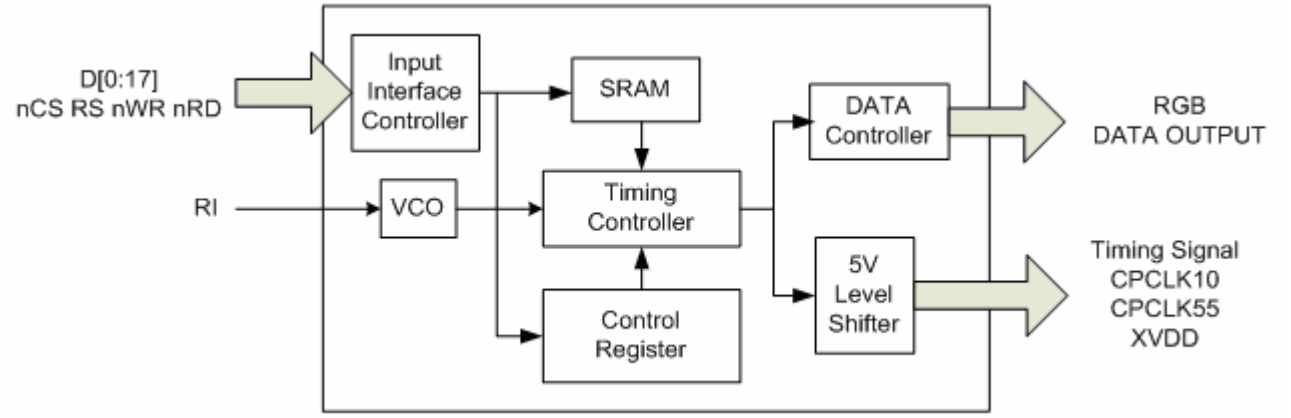
10.8.2 8Color(Dithering) Mode



Note:

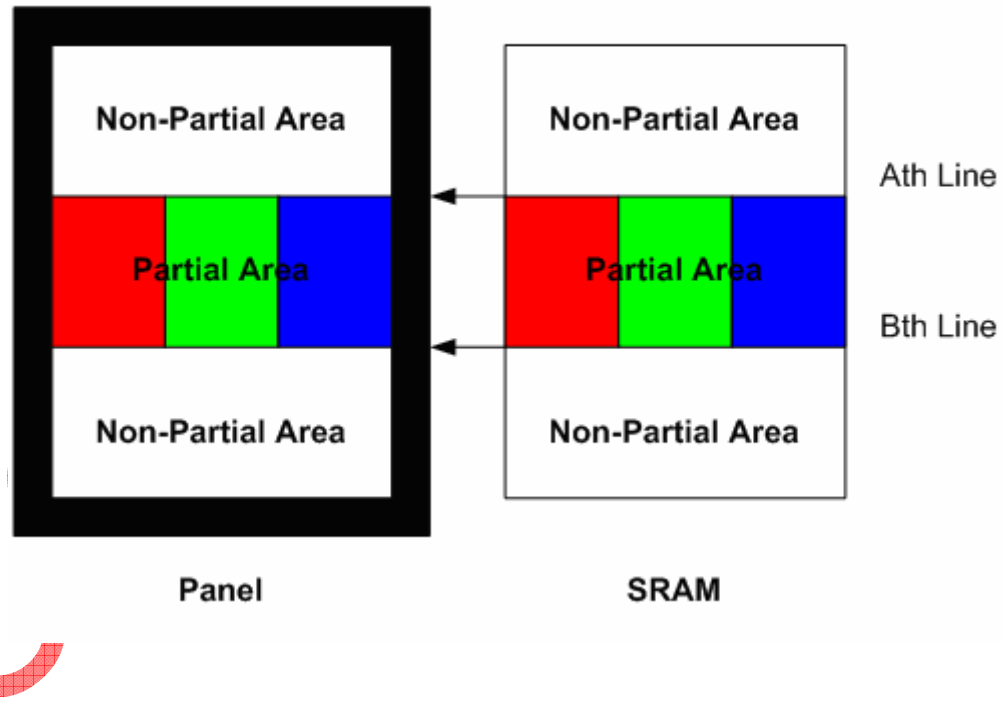
1. CPCLK10、PCLK55、XVDD output

10.8.3 Partial Mode

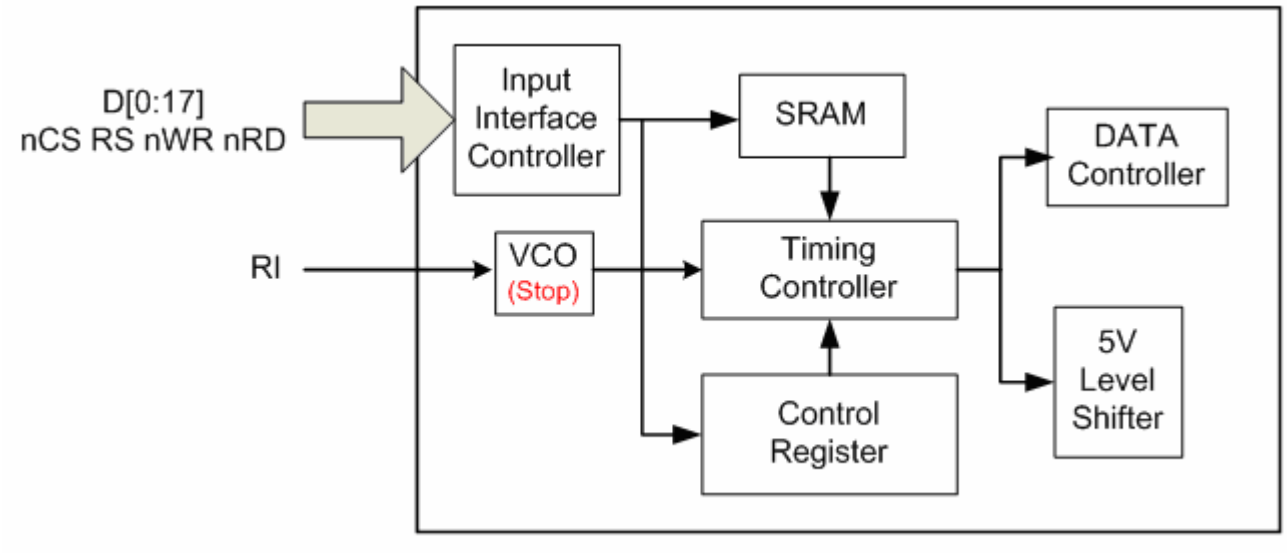


Note:

1. Only display area, other area no signal and no display
2. When full panel display mode change to partial display mode, ASIC must scan two frame white data at non-partial(no display) area.
3. CPCLK10、PCLK55、XVDD output
4.PDS-Y(0x14h)=Ath Line, PDE-Y(0x16h)=Bth Line

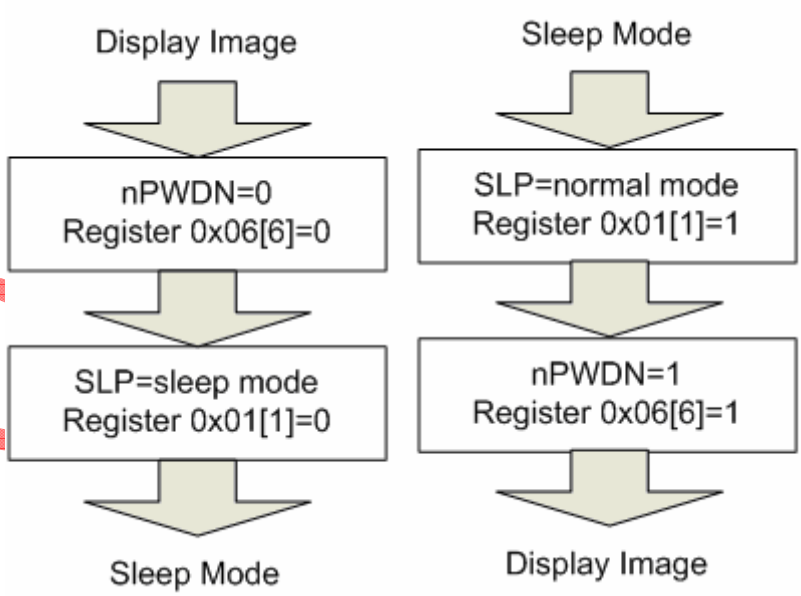


10.8.4 Sleep Mode

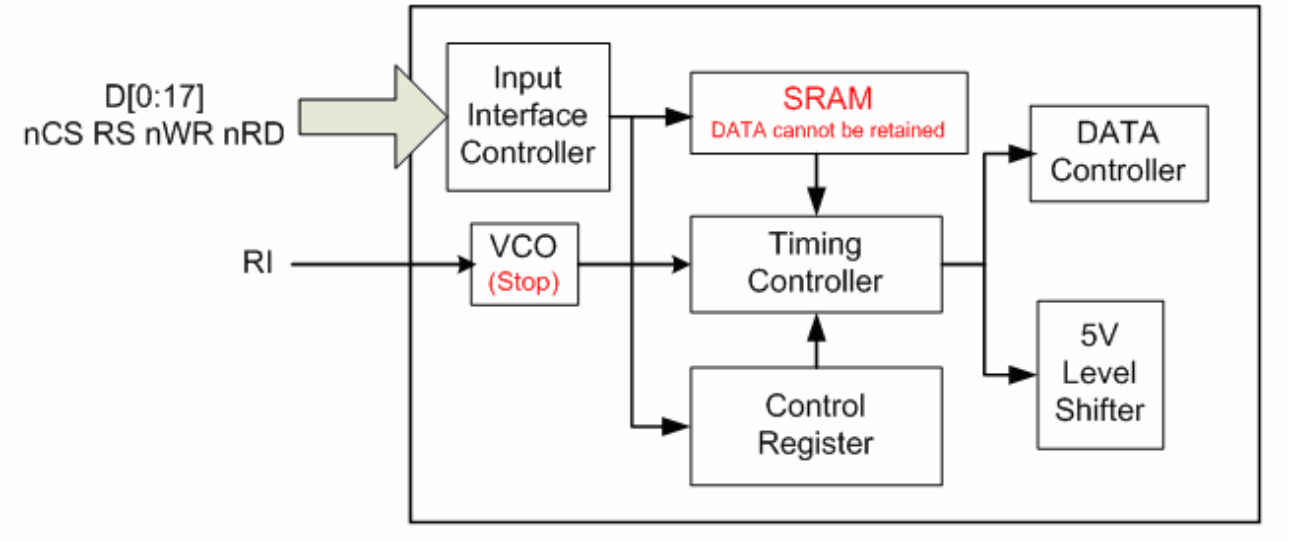


Note:

1. SRAM data can be retained.
2. The VCO is stopped in sleep mode.
3. The power DVDD is not off in sleep mode.
4. CPCLK10、PCLK55、XVDD off

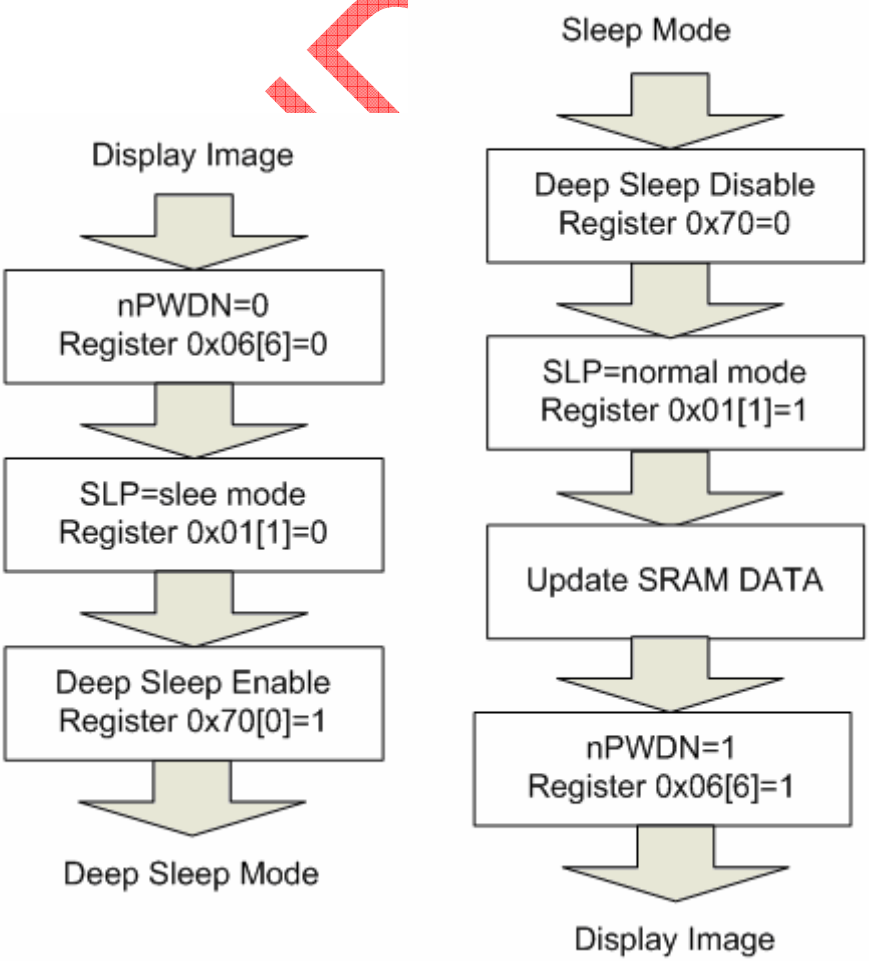


10.8.5 Deep Sleep Mode



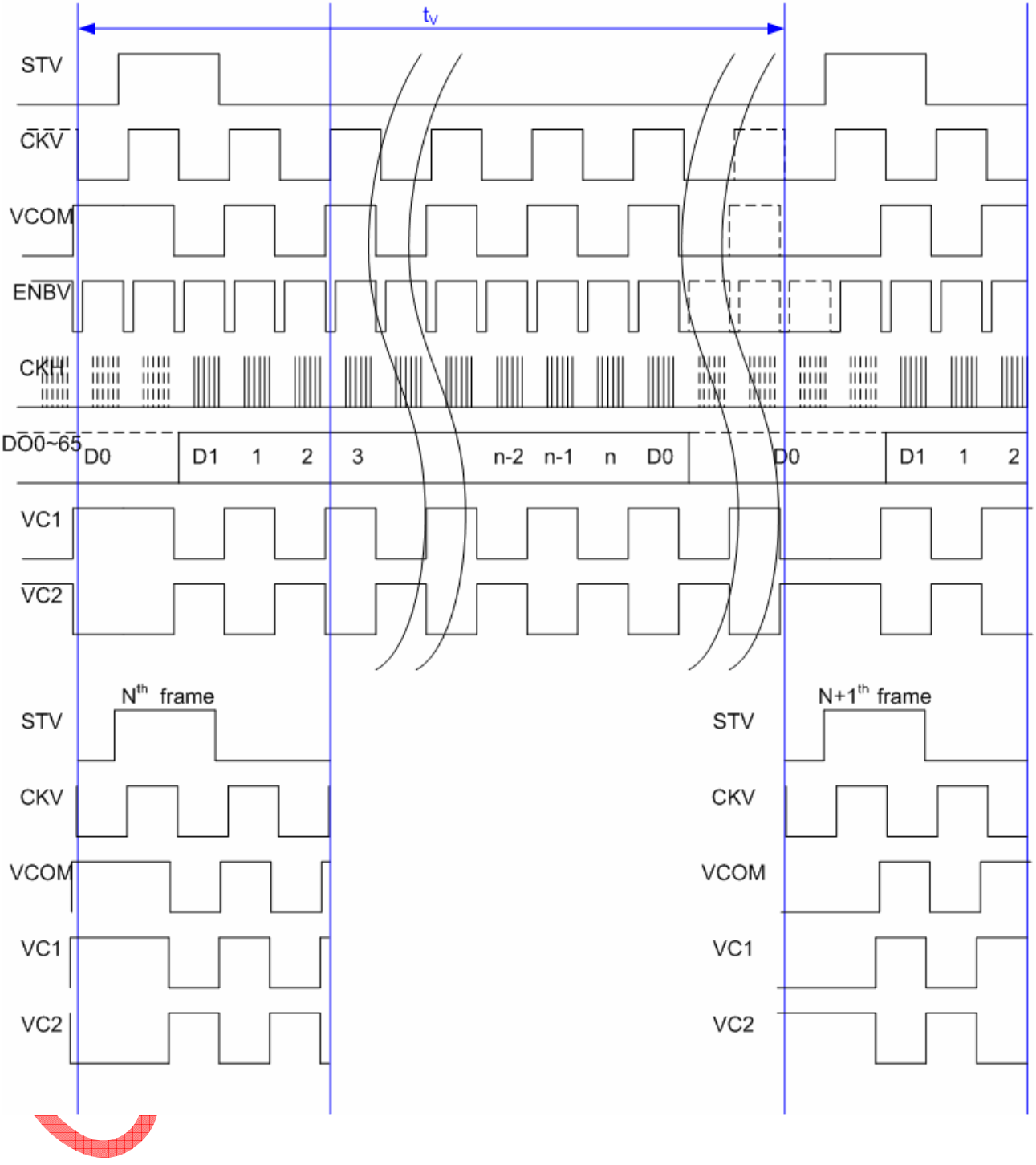
Note:

1. SRAM data can't be retained.
2. The VCO is stopped in sleep mode.
3. The power DVDD isn't off in sleep mode.
4. CPCLK10、PCLK55、XVDD off

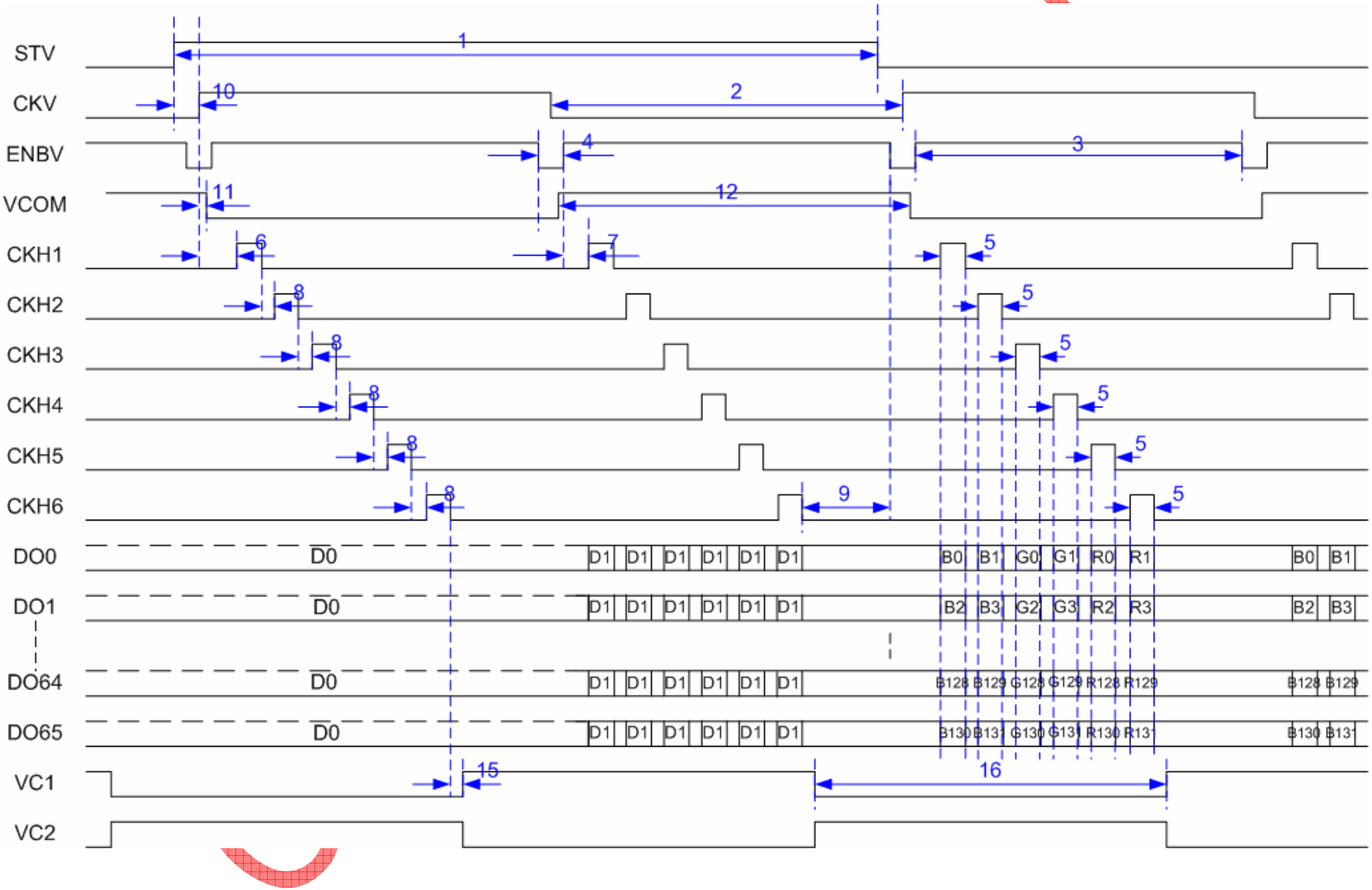


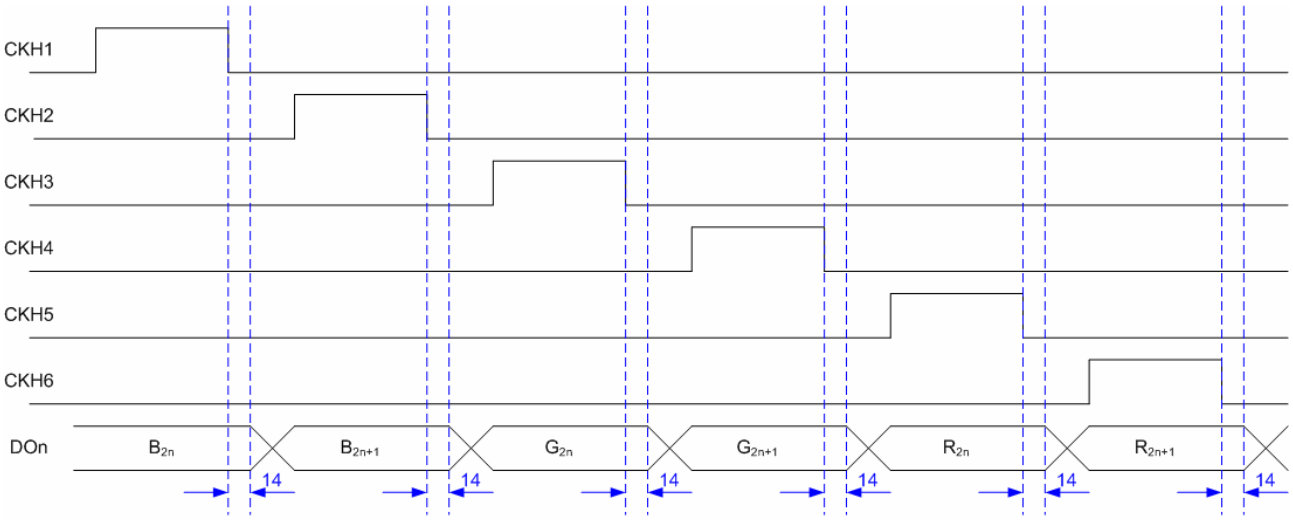
10.9 OUTPUT TIMING CHART

10.9.1 Vertical Timing CSV=H/L t_{Vdisp}=n



10.9.2 Horizontal Timing CSV=H/L t_{Vdisp}=n





10.10 CPU INTERFACE VCO FREQUENCE

10.10.1 128(132)X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		**1.77**	**1.82**	**1.87**	MHz
	Clock time	t_{clk}		566.4	549.5	534.76	ns
	High time	t_{clk_H}		—	0.5 t_{clk}	—	ns
	Low time	t_{clk_L}		—	0.5 t_{clk}	—	ns

10.10.2 128X128 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		**1.46**	**1.5**	**1.55**	MHz
	Clock time	t_{clk}		684.9	666.7	645.2	ns
	High time	t_{clk_H}		—	0.5 t_{clk}	—	ns
	Low time	t_{clk_L}		—	0.5 t_{clk}	—	ns

10.10.3 96X96 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		**0.87**	**0.9**	**0.93**	MHz
	Clock time	t_{clk}		1.15	1.1	1.08	us
	High time	t_{clk_H}		—	0.5 t_{clk}	—	ns
	Low time	t_{clk_L}		—	0.5 t_{clk}	—	ns

10.11 CPU INTERFACE TIMING COUNT

10.11.1 128(132)X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		—	176	—	t_{clk}
	Active	t_{Hdisp}		—	128	—	t_{clk}
Vertical	Period	t_V		—	172	—	t_H
	Active	t_{Vdsip}		—	160	—	t_H

10.11.2 128X128 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		—	176	—	t_{clk}
	Active	t_{Hdisp}		—	128	—	t_{clk}
Vertical	Period	t_V		—	140	—	t_H
	Active	t_{Vdsip}		—	128	—	t_H

10.11.3 96X96 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		—	140	—	t_{clk}
	Active	t_{Hdisp}		—	96	—	t_{clk}
Vertical	Period	t_V		—	108	—	t_H
	Active	t_{Vdsip}		—	96	—	t_H

10.12 OUTPUT TIMING CHARACTERISTIC

10.12.1 128(132)X160 Mode

No.	Min.	Typ.	Max.	unit	Note
1	—	352	—	t_{clk}	
2	—	176	—	t_{clk}	
3	—	163	—	t_{clk}	
4	—	13	—	t_{clk}	
5	—	16	—	t_{clk}	
6	—	14	—	t_{clk}	
7	—	7	—	t_{clk}	
8	—	5	—	t_{clk}	
9	—	41	—	t_{clk}	
10	—	5	—	t_{clk}	
11	—	2	—	t_{clk}	
12	—	176	—	t_{clk}	
13	—	t_V	—		
14	—	2	—	t_{clk}	
15	—	3	—	t_{clk}	
16	—	176	—	t_{clk}	

10.12.2 128X128 Mode

No.	Min.	Typ.	Max.	unit	Note
1	—	352	—	t_{clk}	
2	—	176	—	t_{clk}	
3	—	163	—	t_{clk}	
4	—	13	—	t_{clk}	
5	—	16	—	t_{clk}	
6	—	14	—	t_{clk}	
7	—	7	—	t_{clk}	
8	—	5	—	t_{clk}	
9	—	41	—	t_{clk}	
10	—	5	—	t_{clk}	
11	—	2	—	t_{clk}	
12	—	176	—	t_{clk}	
13	—	t_V	—		
14	—	2	—	t_{clk}	
15	—	3	—	t_{clk}	
16	—	176	—	t_{clk}	

10.12.3 96X96 Mode

No.	Min.	Typ.	Max.	unit	Note
1	—	280	—	t_{clk}	
2	—	140	—	t_{clk}	
3	—	127	—	t_{clk}	
4	—	13	—	t_{clk}	
5	—	13	—	t_{clk}	
6	—	14	—	t_{clk}	
7	—	6	—	t_{clk}	
8	—	3	—	t_{clk}	
9	—	28	—	t_{clk}	
10	—	5	—	t_{clk}	
11	—	2	—	t_{clk}	
12	—	140	—	t_{clk}	
13	—	t_V	—		
14	—	1	—	t_{clk}	
15	—	3	—	t_{clk}	
16	—	140	—	t_{clk}	

11. REGISTER DESCRIPTIONS

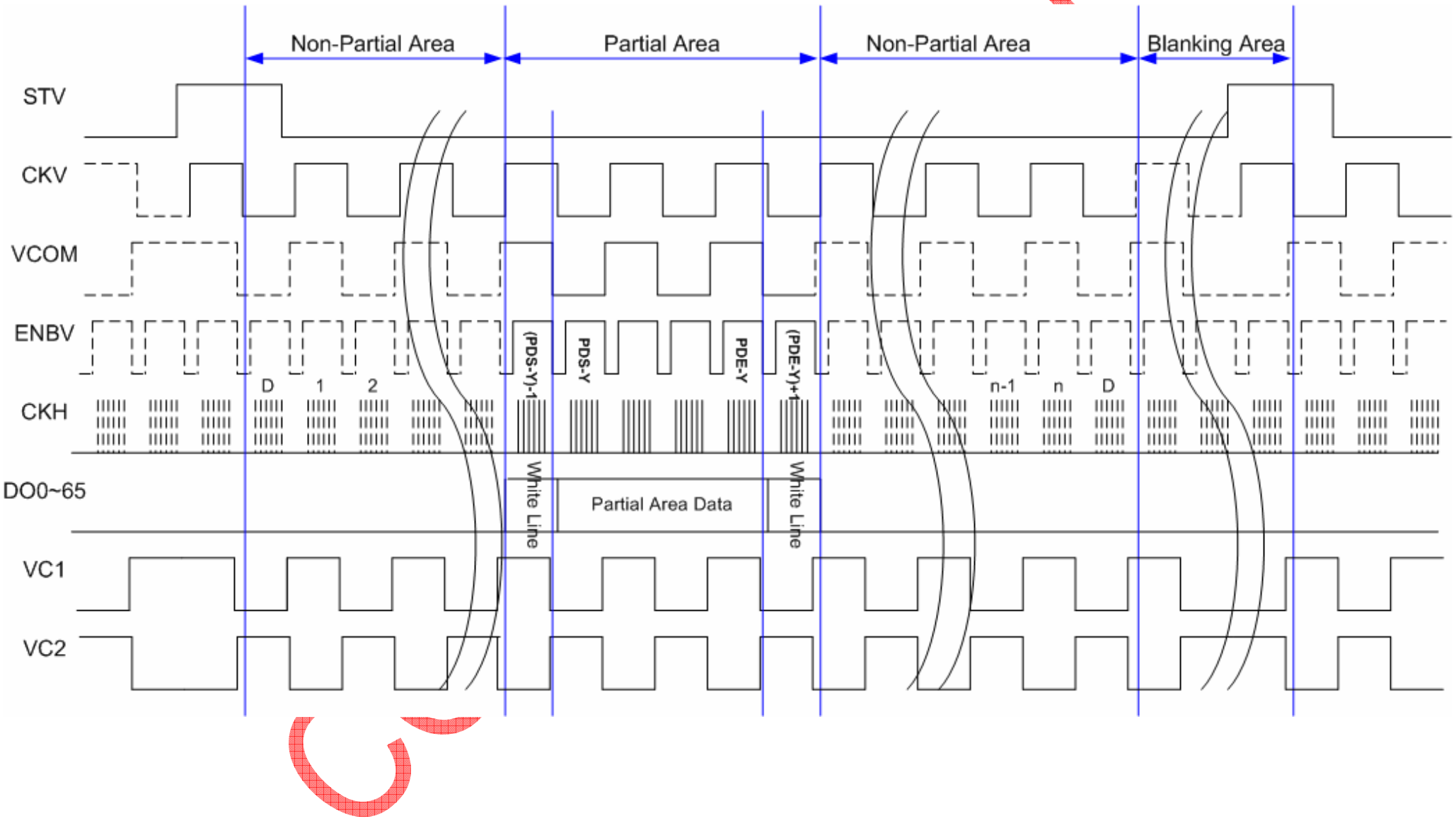
There are two interfaces for registers access, which are CPU interface and SPI interface. In the CPU mode, the registers access timing is similar to the memory except to the polarity of control signal RS. Please refer to the “CPU Interface Mode” section for the detailed timing and access sequence. In the RGB mode, the SPI interface is used to access the control registers, and the access timing is shown as following diagram.

Address	Register/ Bit Name	Reset Value	Meaning	Comment
0x00	CHIPID		[7:3]REVID (read only) [2:0]CHIPID (read only) 000:TP118 001:TP119	
0x01	MODE_SEL1	0000-001x	[7:6]Panel resolution select 00: 128 x 160 (Default) 01: 128 x 128 10 : 96 x 96 11 : 132 x 160 [5]VCOM output mask on non-partial area in partial mode 0: Normal (unmask) (Default) 1: VCOM output mask [4:2]display mode 000: 16/18 bit color(Default) 001: 16/18 bit color + partial 010: 1bit color 011: 8 color + partial 100: 8color + dithering 101: 8 color + dithering + partial [1]SLP: sleep mode 0: sleep 1: normal(Default)	Note1
0x02	MODE_SEL2	000x-001x	[7:6]Scan direction [7] 0 : CSV pin=1(V normal scan) (Default) 1 : CSV pin=0 (V reverse scan) [6] 0 : CSH=1(H normal scan) (Default) 1 : CSH=0(H reverse scan) [5]Line or frame inversion driving select 0 : Line inversion (Default) ; 1 : Frame inversion [4]x [3]STV signal output 0 : STV output (Default) 1 : STV NO output [2:1]Non-partial area data output control 00 : GND output 01 : VCOM output(Default) 1x : Hi-Z	

0x03	MODE_SEL3	0000-xxxx	[7:6]Input data selection 00 : 8 bit mode (Default) 01 : 16 bit mode 10 : 9 bit mode 11 : 18 bit mode [5:4]BODR : 16 bit data access control 00 : 1st cycle transfer only 2 bit data and 2nd cycle transfer 16 bit data (Default) 01 : 1st cycle transfer 16 bit data and 2nd cycle transfer only 2 bit data 1x : Transfer 16 bit data (R:G:B = 5:6:5)	
0x04	MODE_SEL4	0000-xxxx	[7]RGB interface mode selection 0 : DE(Default) 1 : VS + HS [6]SYNC polarity 0 : Negative(Default) 1 : Positive [5]Input data mapping selection 0 : 18 bits(Default) (R : G : B = 6:6:6) 1 : 16 bits (R : G : B = 5:6:5) [4]Input mode selection 0 : moving mode(Default) 1 : still mode	Only for Parallel RGB Mode Bit 5 for SPI Mode
0x05	VCO_Mode	xxx0-1000	[4:3]VCO bias mode select 00 : -5% 01 : typical (Default) 10 : +5% 11 : +10% [5] , [2:0]VCO frequency 0 , 000 : 1.82 MHz (Default) 1 , 000 : 1.82 × 3/4 MHz 0 , 001 : 1.82 / 2 MHz 0 , 010 : 1.5 MHz 1 , 010 : 1.5 × 3/4 MHz 0 , 011 : 1.5 / 2 MHz 0 , 100 : 0.9 MHz 1 , 100 : 0.9 × 3/4 MHz 0 , 101 : 0.9 / 2 MHz	
0x06	DAC_OP_CTRL2	1000-0101	[7]nPWDN signal select 0 : Input pin PWDN 1 : Internal register ([6]) (Default) [6]internal nPWDN control : 0 : nPWDN=L(Default) 1 : nPWDN=H [5:4]DAC bias select 00 : 100% (Default) 01 : 80% 10 : 60% 11 : 50% [3:2]Vcom bias select 00 : -20% × normal 01 : normal (Default) 10 : 20% × normal 11 : 40% × normal [1:0]RGB loading select 00 : Loading 1 01 : Loading 2 (Default) 10 : Loading 3 11 : Loading 4	

0x07	VCOMH_CTRL	x111-0100	[6:0]VCOM_H output Voltage control step = 2.1V/128 = 0.0164V **(Default = 4.0V)** **(** VCOM_H=2.1V in settting x000-0001)	Note2
0x08	VCOML_CTRL	x001-0010	[6:0]VCOM_L output Voltage control step = 2.1V/128 = 0.0164V **(Default = 0.295V)** **(** VCOM_L=0V in setting x000-0000)	Note2
SRAM control				
0x09	PWS-X	0000-0000	[7:0]: Write SRAM window start X point	
0x10	PWS-Y	0000-0000	[7:0]: Write SRAM window start Y point	
0x11	PWE-X	0111-1111	[7:0]: Write SRAM window end X point	
0x12	PWE-Y	1001-1111	[7:0]: Write SRAM window end Y point	
0x14	PDS-Y	0000-0000	[7:0]: Partial Display start Y point	
0x16	PDE-Y	0001-1111	[7:0]: Partial Display end Y point	
0x17	SRAM _Control	xxxx-0000	[3]if X or Y position is set over range, 0 : Ineffective writing. X or Y position are not changed. (Default) [2]ACX (SRAM X Address Counter) 0 : SRAM X position + 1 (Default) 1 : SRAM X position – 1 [1]ACY (SRAM Y Address Counter) 0 : SRAM Y position + 1 (Default) 1 : SRAM Y position –1 [0]ACXY (SRAM access control) 0 : add X position first then add Y position (Default) 1 : add Y position first then add X position	Note 3 [3] register always 0
0x18	SRAM_Position_X	0000-0000	[7:0]: SRAM X position 0<= X <=0x83	
0x19	SRAM_Position_Y	0000-0000	[7:0]: SRAM Y position 0<= Y <= 0x9F	
0x1A	Th	0001-0010	[7:0]t_{Hds} (min to max) : 1clk / step [0 ~ 255]	Only for Parallel RGB Mode
0x1B	Tv	xxx0-0110	[4:0]t_{Vds} (min to max) : 1t_H / step [0~31]	Only for Parallel RGB Mode
Gamma voltage adjustable level				
0x21	Gamma adjust 1		[7:4]: PV0 [3:0]: NV0	Note4
0x22	Gamma adjust 2		[7:4]: PV1 [3:0]: NV1	Note4
0x23	Gamma adjust 3		[7:4]: PV6 [3:0]: NV6	Note4
0x24	Gamma adjust 4		[7:4]: PV11 [3:0]: NV11	Note4
0x25	Gamma adjust 5		[7:4]: PV17 [3:0]: NV17	Note4
0x26	Gamma adjust 6		[7:4]: PV26 [3:0]: NV26	Note4
0x27	Gamma adjust 7		[7:4]: PV53 [3:0]: NV53	Note4
0x28	Gamma adjust 8		[7:4]: PV59 [3:0]: NV59	Note4
0x29	Gamma adjust 9		[7:4]: PV62 [3:0]: NV62	Note4

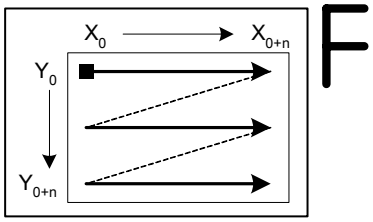
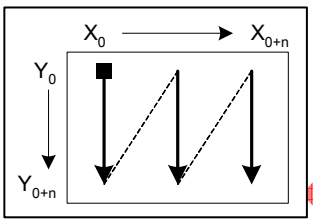
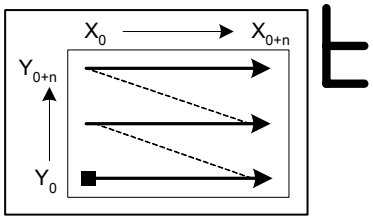
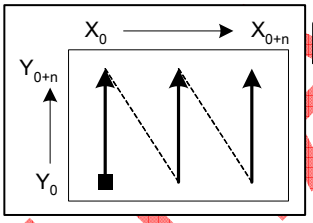
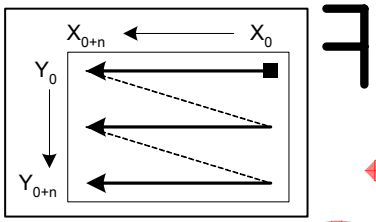
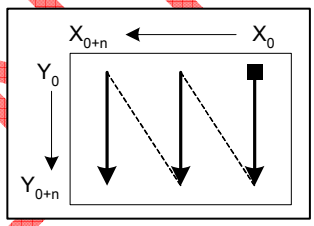
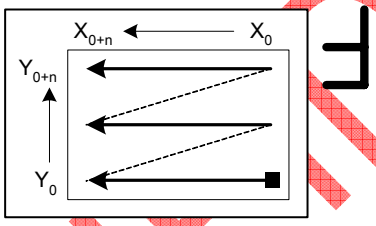
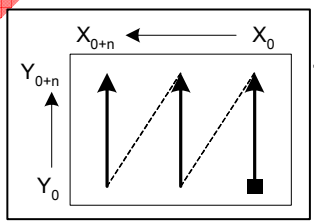
Note1: The timing of partial display is showed as below figure.



Note 2: The following table shows the VCOMH and VCOML voltage mapping to register step setting

Digital Input (Decimal)	VCOMH Output (V)	Digital Input (Decimal)	VCOML Output (V)
127	4.184	127	2.084
126	4.167	126	2.067
125	4.151	125	2.051
124	4.134	124	2.034
123	4.118	123	2.018
122	4.102	122	2.002
121	4.085	121	1.985
120	4.069	120	1.969
119	4.052	119	1.952
118	4.036	118	1.936
117	4.020	117	1.920
116	4.003	116	1.903
115	3.987	115	1.887
114	3.970	114	1.870
24	2.494	24	0.394
23	2.477	23	0.377
22	2.461	22	0.361
21	2.445	21	0.345
20	2.428	20	0.328
19	2.412	19	0.312
18	2.395	18	0.295
17	2.379	17	0.279
16	2.363	16	0.263
15	2.346	15	0.246
14	2.330	14	0.230
13	2.313	13	0.213
12	2.297	12	0.197
11	2.280	11	0.180
10	2.264	10	0.164
9	2.248	9	0.148
8	2.231	8	0.131
7	2.215	7	0.115
6	2.198	6	0.098
5	2.182	5	0.082
4	2.166	4	0.066
3	2.149	3	0.049
2	2.133	2	0.033
1	2.1	1	0.016

Note3: Addressing mode supported for CPU interface

ACX	ACY	ACXY	Scan Types	ACX	ACY	ACXY	Scan Types
0	0	0		0	0	1	
0	1	0		0	1	1	
1	0	0		1	0	1	
1	1	0		1	1	1	

Note 4:

The two type gamma circuits are switched by AVDD3_SEL and the default value of 0x21h to 0x29h is decided by AVDD3_SEL. The 3.8V Vlc Gamma voltage adjusted range is show as below table.

4 Bit Adjustable Level，PV									
Value	**PV0**	**PV1**	**PV6**	**PV11**	**PV17**	**PV26**	**PV53**	**PV59**	**PV62**
0000	4.08	3.98	3.28	2.91	2.64	2.39	1.78	1.56	1.11
0001	4.12	4.02	3.32	2.95	2.68	2.43	1.82	1.60	1.15
0010	4.16	4.06	3.36	2.99	2.72	2.47	1.86	1.64	1.19
0011	4.20	4.10	3.40	3.03	2.76	2.51	1.90	1.68	1.23
0100	4.24	4.14	3.44	3.07	2.80	2.55	1.94	1.72	1.27
0101	4.28	4.18	3.48	3.11	2.84	2.59	1.98	1.76	1.31
0110	4.32	4.22	3.52	3.15	2.88	2.63	2.02	1.80	1.35
0111	4.36	4.26	3.56	3.19	2.92	2.67	2.06	1.84	1.39
1000	4.40	4.30	3.60	3.23	2.96	2.71	2.10	1.88	1.43
1001	4.44	4.34	3.64	3.27	3.00	2.75	2.14	1.92	1.47
1010	4.48	4.38	3.68	3.31	3.04	2.79	2.18	1.96	1.51
1011	4.52	4.42	3.72	3.35	3.08	2.83	2.22	2.00	1.55
1100	4.56	4.46	3.76	3.39	3.12	2.87	2.26	2.04	1.59
1101	4.60	4.50	3.80	3.43	3.16	2.91	2.30	2.08	1.63
1110	4.64	4.54	3.84	3.47	3.20	2.95	2.34	2.12	1.67
1111	4.68	4.58	3.88	3.51	3.24	2.99	2.38	2.16	1.71

4 Bit Adjustable Level，NV									
Value	**NV0**	**NV1**	**NV6**	**NV11**	**NV17**	**NV26**	**NV53**	**NV59**	**NV62**
0000	0.82	0.92	1.62	1.99	2.26	2.51	3.12	3.34	3.79
0001	0.78	0.88	1.58	1.95	2.22	2.47	3.08	3.30	3.75
0010	0.74	0.84	1.54	1.91	2.18	2.43	3.04	3.26	3.71
0011	0.70	0.80	1.50	1.87	2.14	2.39	3.00	3.22	3.67
0100	0.66	0.76	1.46	1.83	2.10	2.35	2.96	3.18	3.63
0101	0.62	0.72	1.42	1.79	2.06	2.31	2.92	3.14	3.59
0110	0.58	0.68	1.38	1.75	2.02	2.27	2.88	3.10	3.55
0111	0.54	0.64	1.34	1.71	1.98	2.23	2.84	3.06	3.51
1000	0.50	0.60	1.30	1.67	1.94	2.19	2.80	3.02	3.47
1001	0.46	0.56	1.26	1.63	1.90	2.15	2.76	2.98	3.43
1010	0.42	0.52	1.22	1.59	1.86	2.11	2.72	2.94	3.39
1011	0.38	0.48	1.18	1.55	1.82	2.07	2.68	2.90	3.35
1100	0.34	0.44	1.14	1.51	1.78	2.03	2.64	2.86	3.31
1101	0.30	0.40	1.10	1.47	1.74	1.99	2.60	2.82	3.27
1110	0.26	0.36	1.06	1.43	1.70	1.95	2.56	2.78	3.23
1111	0.22	0.32	1.02	1.39	1.66	1.91	2.52	2.74	3.19

The 3.3V Vlc Gamma voltage adjusted range is show as below table.

4 Bit Voltage Adjustable Level，PV									
Value	**PV0**	**PV1**	**PV6**	**PV11**	**PV17**	**PV26**	**PV53**	**PV59**	**PV62**
0000	3.592	3.851	3.101	2.798	2.625	2.417	1.940	1.757	1.354
0001	3.632	3.861	3.131	2.823	2.645	2.432	1.950	1.767	1.364
0010	3.672	3.871	3.161	2.848	2.665	2.447	1.960	1.777	1.374
0011	3.712	3.881	3.191	2.873	2.685	2.462	1.970	1.787	1.384
0100	3.752	3.891	3.221	2.898	2.705	2.477	1.980	1.797	1.394
0101	3.792	3.901	3.251	2.923	2.725	2.492	1.990	1.807	1.404
0110	3.832	3.911	3.281	2.948	2.745	2.507	2.000	1.817	1.414
0111	3.872	3.921	3.311	2.973	2.765	2.522	2.010	1.827	1.424
1000	3.912	3.931	3.341	2.998	2.785	2.537	2.020	1.837	1.434
1001	3.952	3.941	3.371	3.023	2.805	2.552	2.030	1.847	1.444
1010	3.992	3.951	3.401	3.048	2.825	2.567	2.040	1.857	1.454
1011	4.032	3.961	3.431	3.073	2.845	2.582	2.050	1.867	1.464
1100	4.072	3.971	3.461	3.098	2.865	2.597	2.060	1.877	1.474
1101	4.112	3.981	3.491	3.123	2.885	2.612	2.070	1.887	1.484
1110	4.152	3.991	3.521	3.148	2.905	2.627	2.080	1.897	1.494
1111	4.192	4.001	3.551	3.173	2.925	2.642	2.090	1.907	1.504

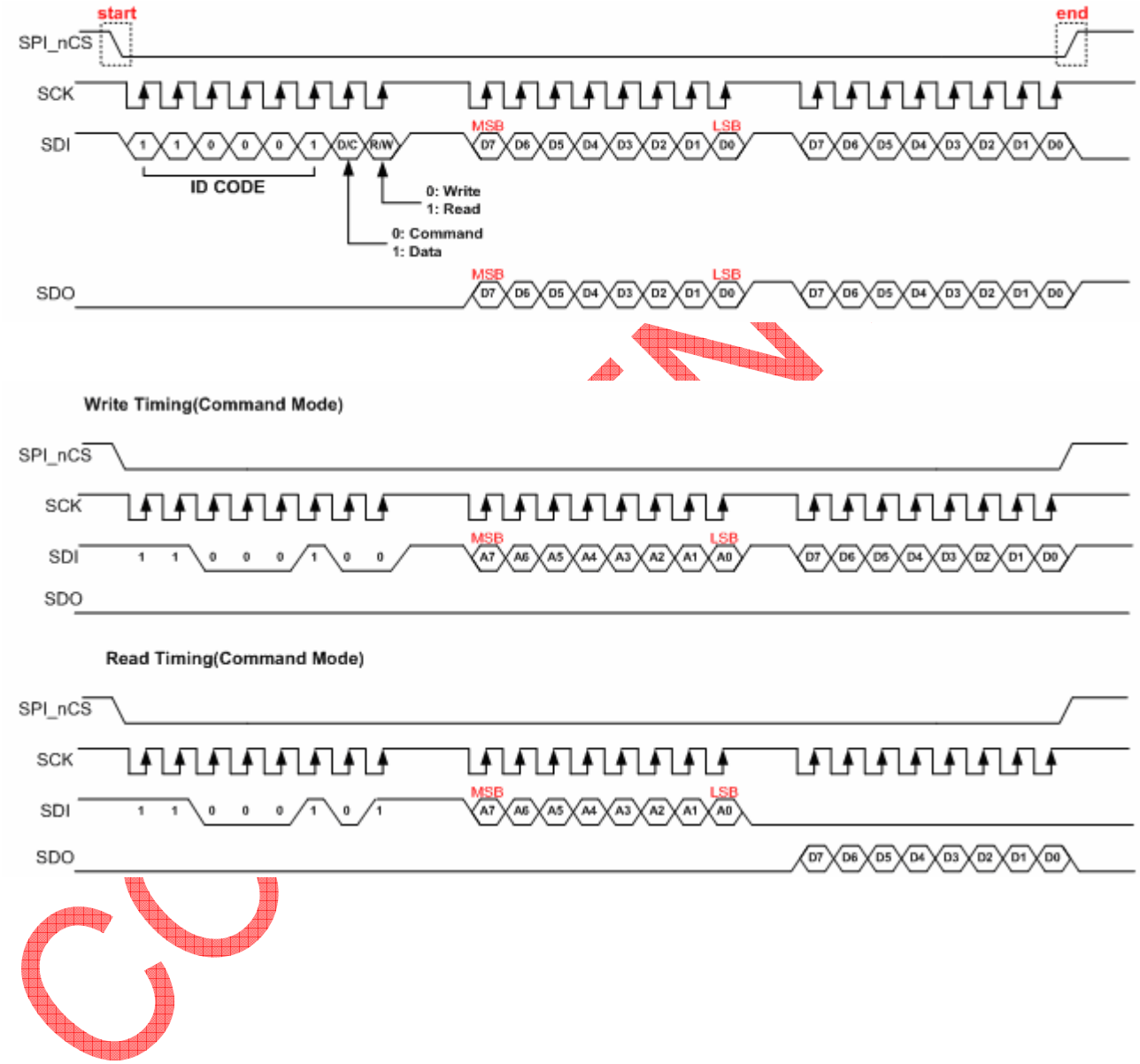
4 Bit Voltage Adjustable Level，NV									
Value	**NV0**	**NV1**	**NV6**	**NV11**	**NV17**	**NV26**	**NV53**	**NV59**	**NV62**
0000	1.438	1.179	1.929	2.232	2.405	2.613	3.090	3.273	3.676
0001	1.398	1.169	1.899	2.207	2.385	2.598	3.080	3.263	3.666
0010	1.358	1.159	1.869	2.182	2.365	2.583	3.070	3.253	3.656
0011	1.318	1.149	1.839	2.157	2.345	2.568	3.060	3.243	3.646
0100	1.278	1.139	1.809	2.132	2.325	2.553	3.050	3.233	3.636
0101	1.238	1.129	1.779	2.107	2.305	2.538	3.040	3.223	3.626
0110	1.198	1.119	1.749	2.082	2.285	2.523	3.030	3.213	3.616
0111	1.158	1.109	1.719	2.057	2.265	2.508	3.020	3.203	3.606
1000	1.118	1.099	1.689	2.032	2.245	2.493	3.010	3.193	3.596
1001	1.078	1.089	1.659	2.007	2.225	2.478	3.000	3.183	3.586
1010	1.038	1.079	1.629	1.982	2.205	2.463	2.990	3.173	3.576
1011	0.998	1.069	1.599	1.957	2.185	2.448	2.980	3.163	3.566
1100	0.958	1.059	1.569	1.932	2.165	2.433	2.970	3.153	3.556
1101	0.918	1.049	1.539	1.907	2.145	2.418	2.960	3.143	3.546
1110	0.878	1.039	1.509	1.882	2.125	2.403	2.950	3.133	3.536
1111	0.838	1.029	1.479	1.857	2.105	2.388	2.940	3.123	3.526

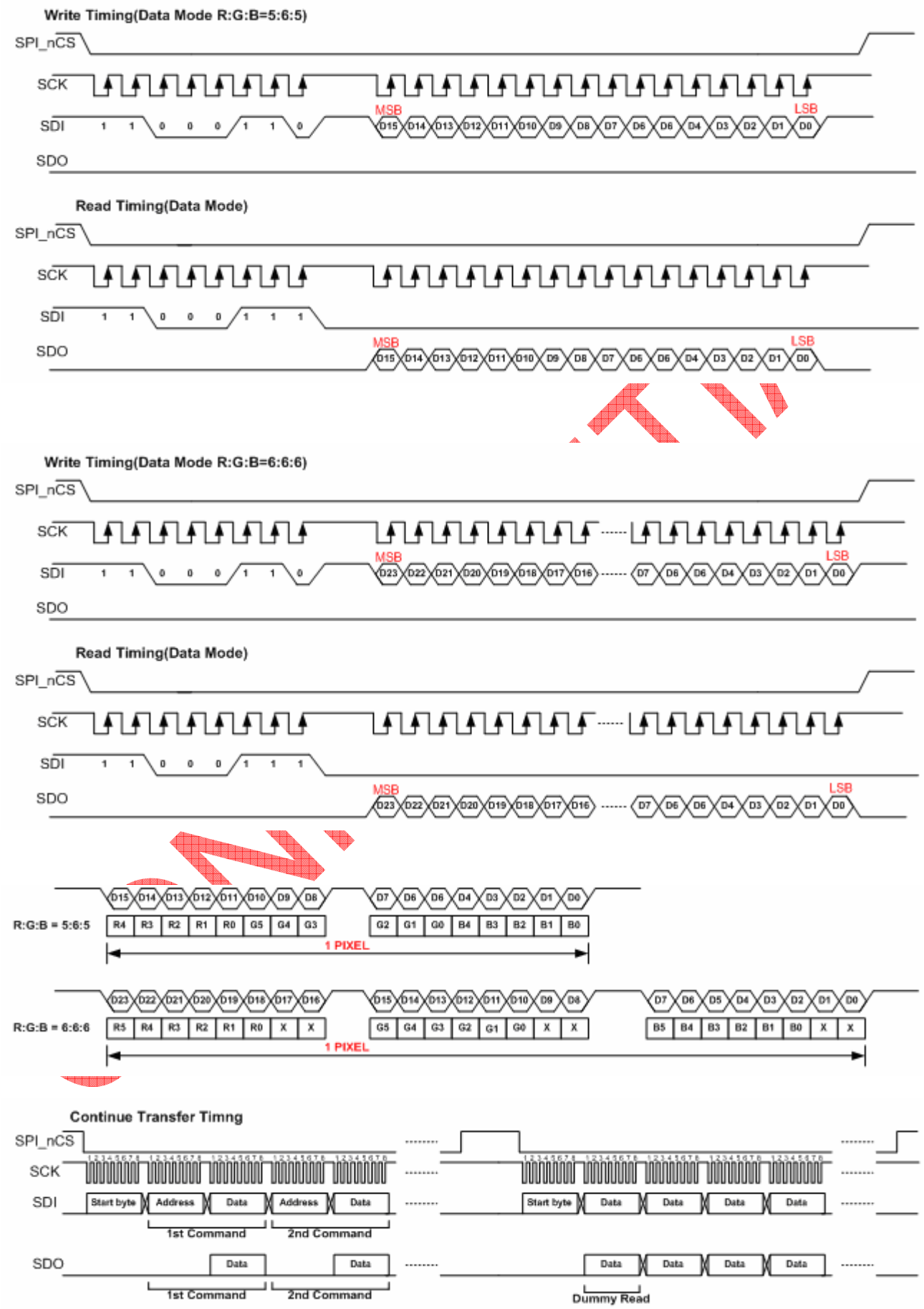
12. SPI & PARALLEL RGB I/F

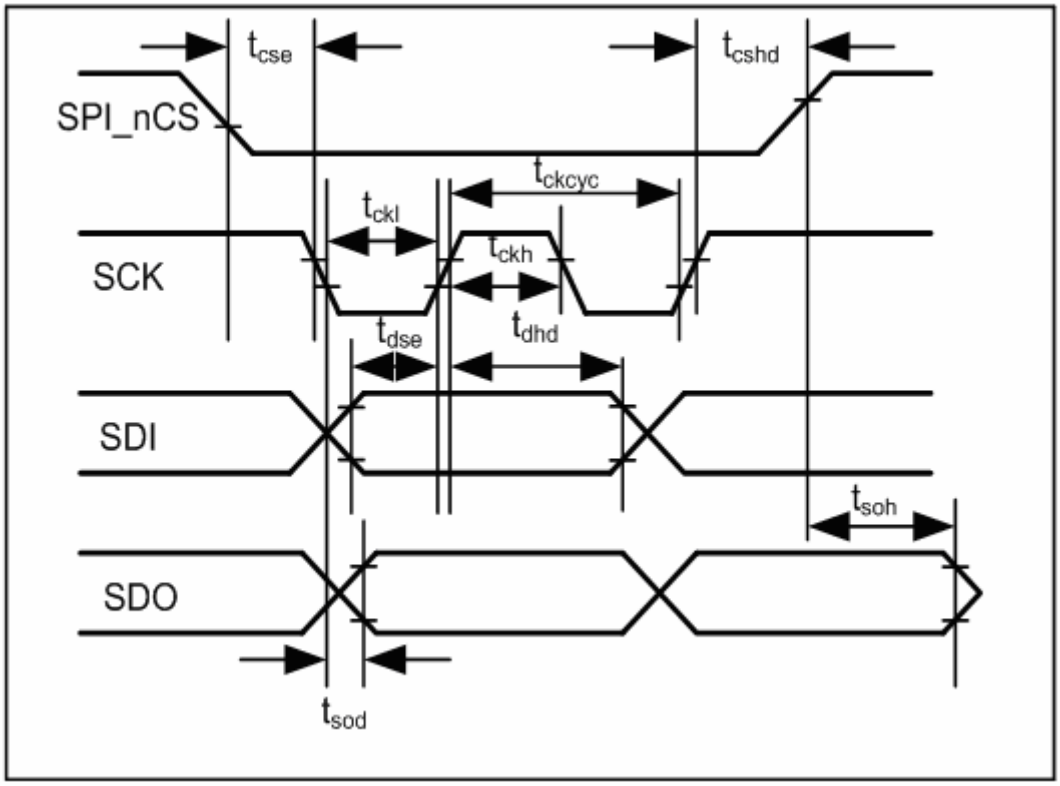
12.1 SERIAL PERIPHERAL INTERFACE(SPI)

C1L5-06 provides SPI interface to read/write registers and write the display memory. The HOST[1:0] pins are used to select the input interface. When writing the registers, the input data of SDI is latched on the rising edge of SCK; reading the register data, the system can latch output data on the rising edge of SCK.

12.1.1 3-Wire SPI Interface Timing



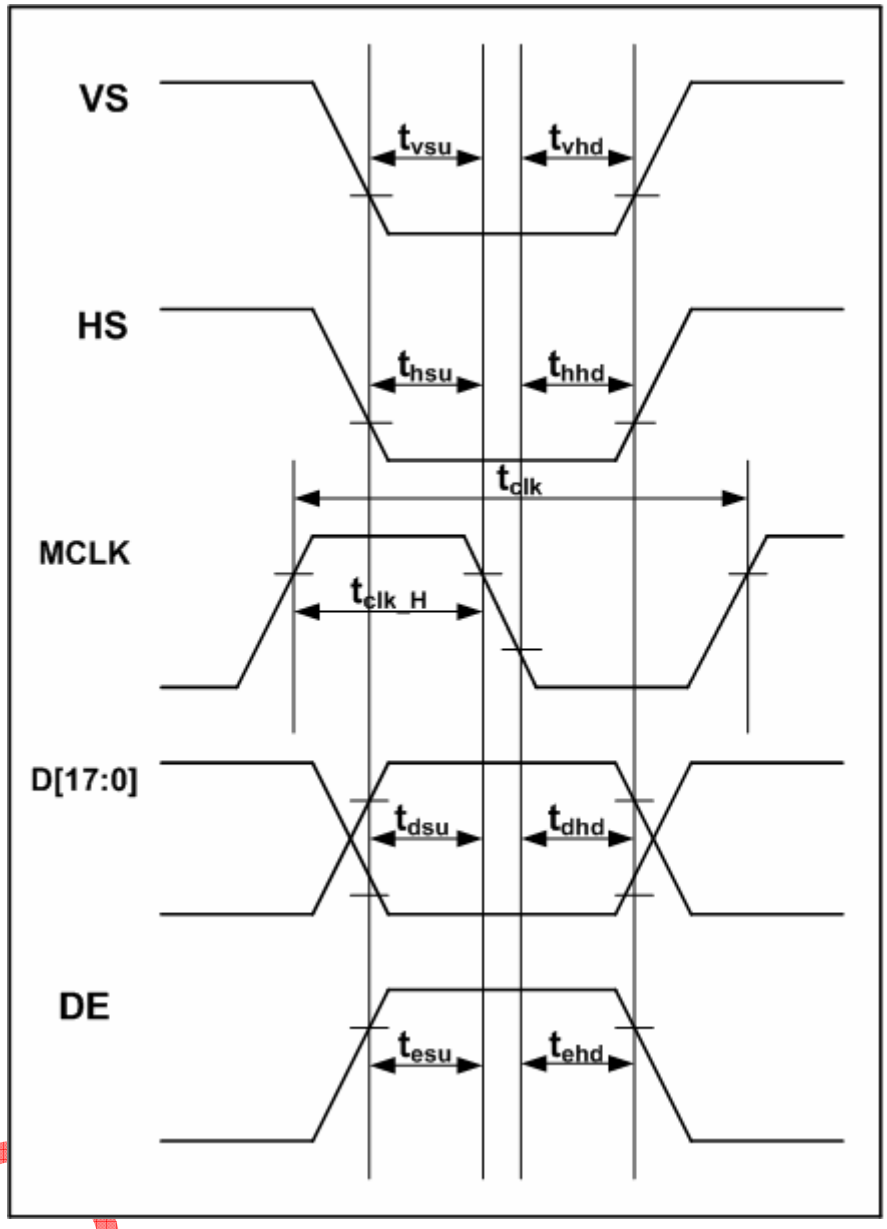




Normal Write Mode(18/16-Bit Interface): VDDIO=1.6 to 3.3 V

Item		Symbol	Min	Typ	Max	unit
Serial colock cycle time	write	t_{ckcyc}	40			ns
	read		40			us
Serial colock pulse width low	write	t_{ckl}	20			ns
	read		20			ns
Serial colock pulse width high	write	t_{ckh}	20			ns
	read		20			ns
Serial clock rise/fall time						ns
SPI_nCS Setup time		t_{cse}	20			ns
SPI_nCS hold time		t_{cshd}	20			ns
Data setup time		t_{dse}	10			ns
Data hold time		t_{dhd}	10			ns
Data output setup time		t_{sod}	10			ns
Data output hold time		t_{soh}	10			ns

12.2 Parallel RGB SINAL AC TIMING CHARACTERISTIC



12.2.1 128(132)X160 Mode

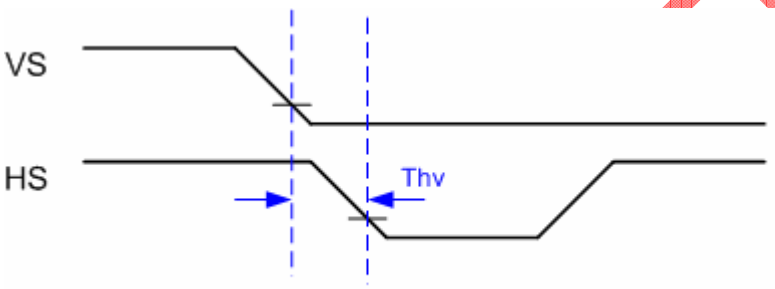
Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		1.7	1.82	2.1	MHz
	Clock time	t_{clk}		588	550	476	ns
	Clock high duration	t_{clk_H}		40		60	%
Data Enable	Setup time	t_{esu}		20	—	—	ns
	Hold Time	t_{ehd}		20	—	—	ns
Hsync	Setup time	t_{hsu}		20	—	—	ns
	Hold Time	t_{hhd}		20	—	—	ns
Vsync	Setup time	t_{vsu}		20	—	—	ns
	Hold Time	t_{vhd}		20	—	—	ns
data	Setup time	t_{dsu}		20	—	—	ns
	Hold time	t_{dhd}		20	—	—	ns

12.2.2 128X128 Mode

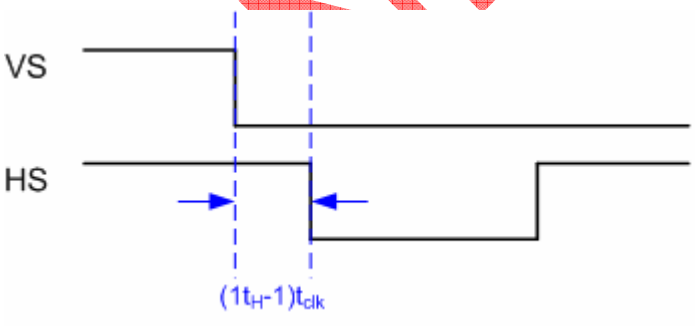
Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		1.25	1.5	1.65	MHz
	Clock time	t_{clk}		800	666.7	606	ns
	Clock high duration	t_{clk_H}		40		60	%
Data Enable	Setup time	t_{esu}		20	—	—	ns
	Hold Time	t_{ehd}		20	—	—	ns
Hsync	Setup time	t_{hsu}		20	—	—	ns
	Hold Time	t_{hhd}		20	—	—	ns
Vsync	Setup time	t_{vsu}		20	—	—	ns
	Hold Time	t_{vhd}		20	—	—	ns
data	Setup time	t_{dsu}		20	—	—	ns
	Hold time	t_{dhd}		20	—	—	ns

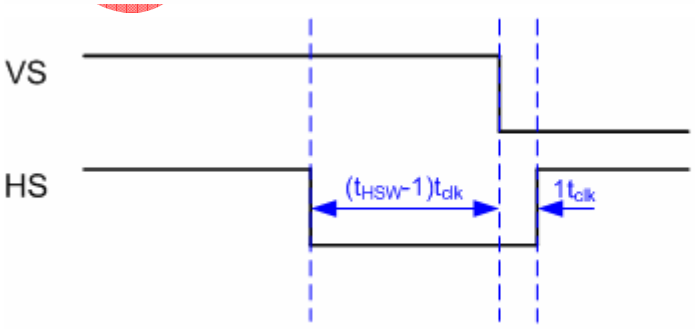
12.2.3 96X96 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Clock	frequency	f_{clk}		0.83	0.9	1	MHz
	Clock time	t_{clk}		1.2	1.1	1	us
	Clock high duration	t_{clk_H}		40		60	%
Data Enable	Setup time	t_{esu}		20	—	—	ns
	Hold Time	t_{ehd}		20	—	—	ns
Hsync	Setup time	t_{hsu}		20	—	—	ns
	Hold Time	t_{hhd}		20	—	—	ns
Vsync	Setup time	t_{vsu}		20	—	—	ns
	Hold Time	t_{vhd}		20	—	—	ns
data	Setup time	t_{dsu}		20	—	—	ns
	Hold time	t_{dhd}		20	—	—	ns



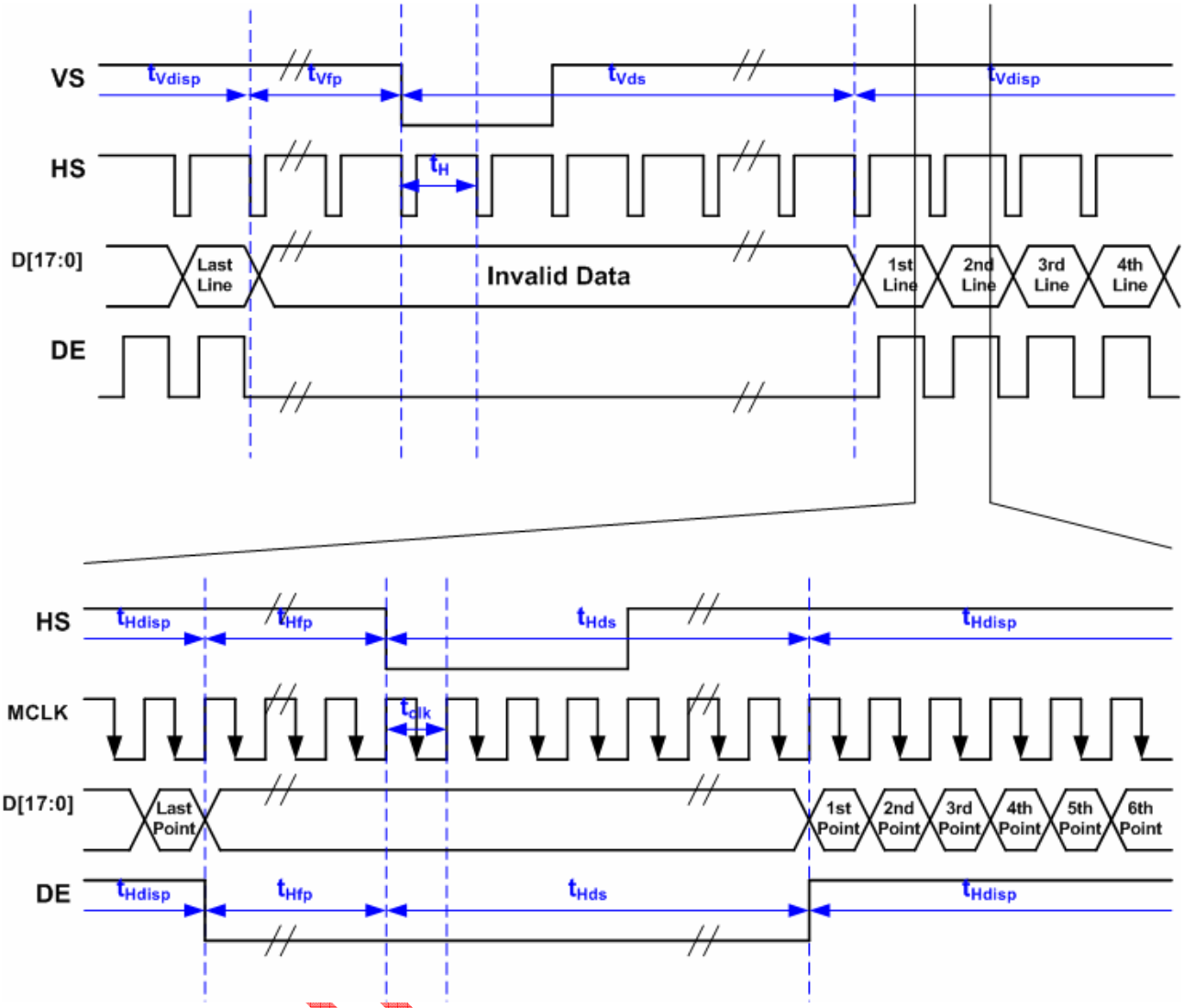
Thv:



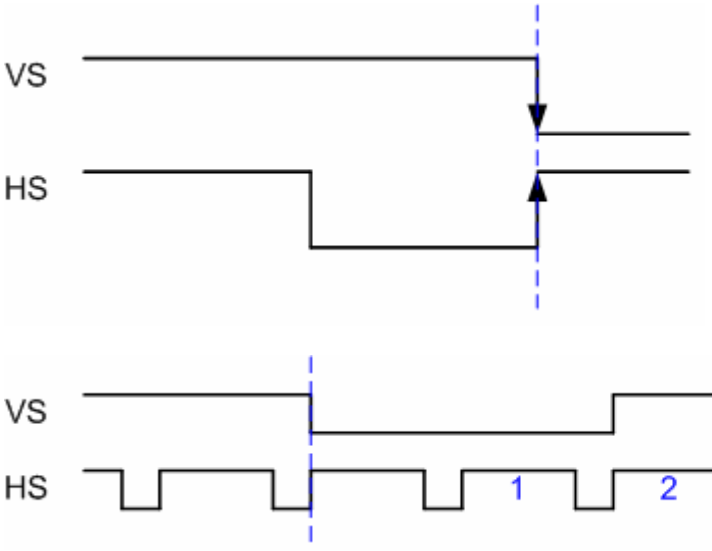


t_{HSW}=HS pulse low width

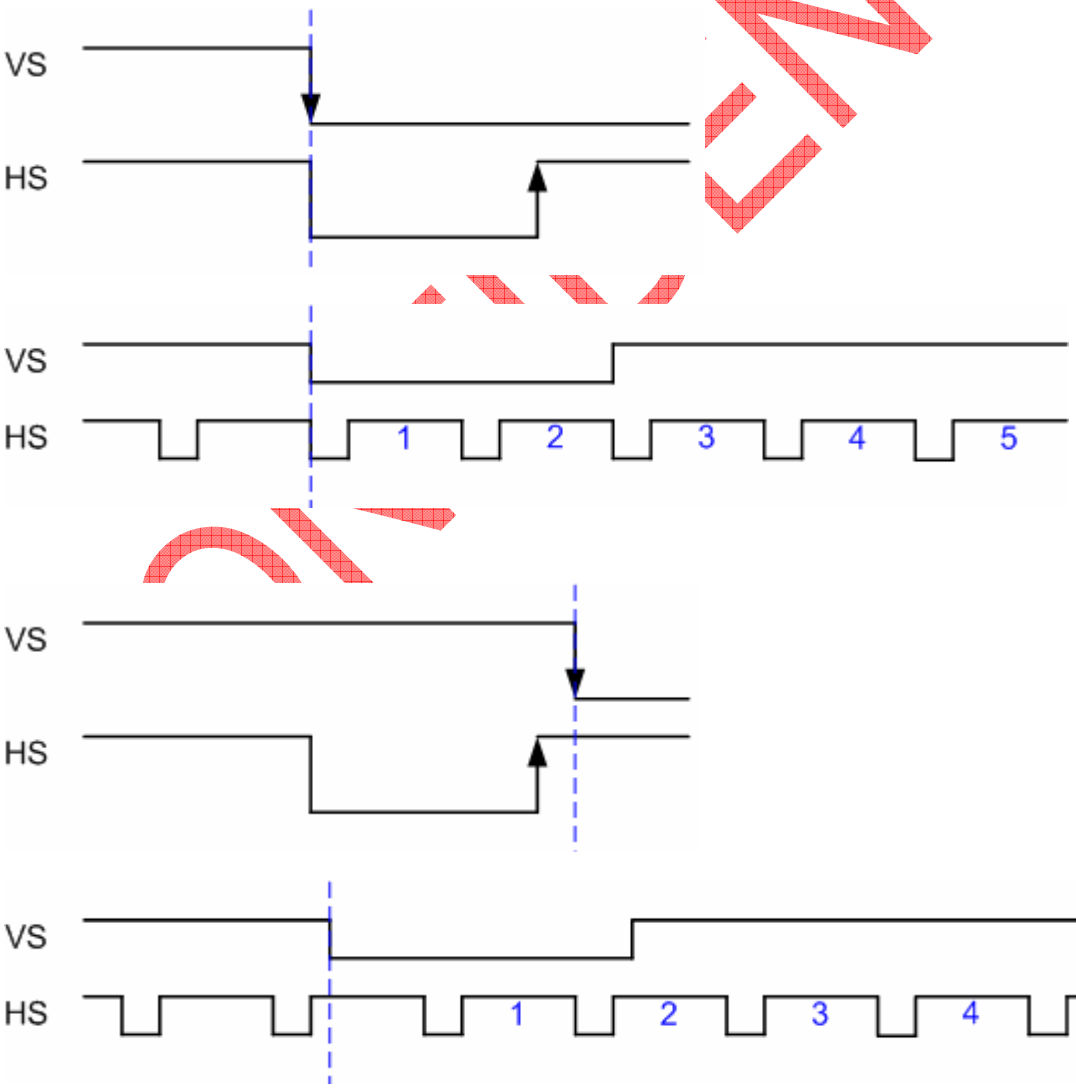
12.3 Parallel RGB INPUT SIGNAL TIMING CHART



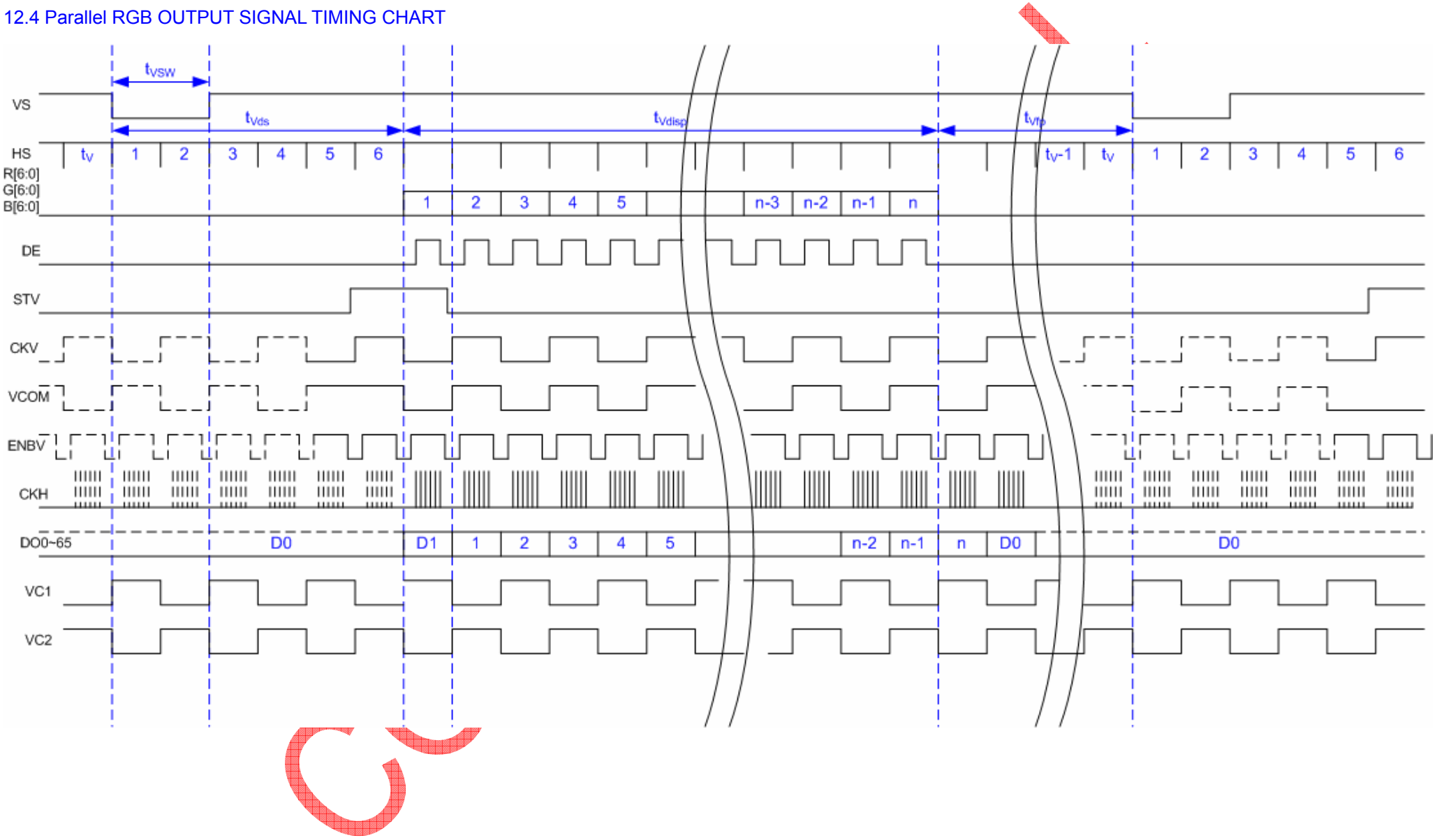
If VS falling edge and HS rising edge are at same time, it is in the margin and not surely which is the first valid data line. So we want it to cause the first valid data line to delay 1 t_H.

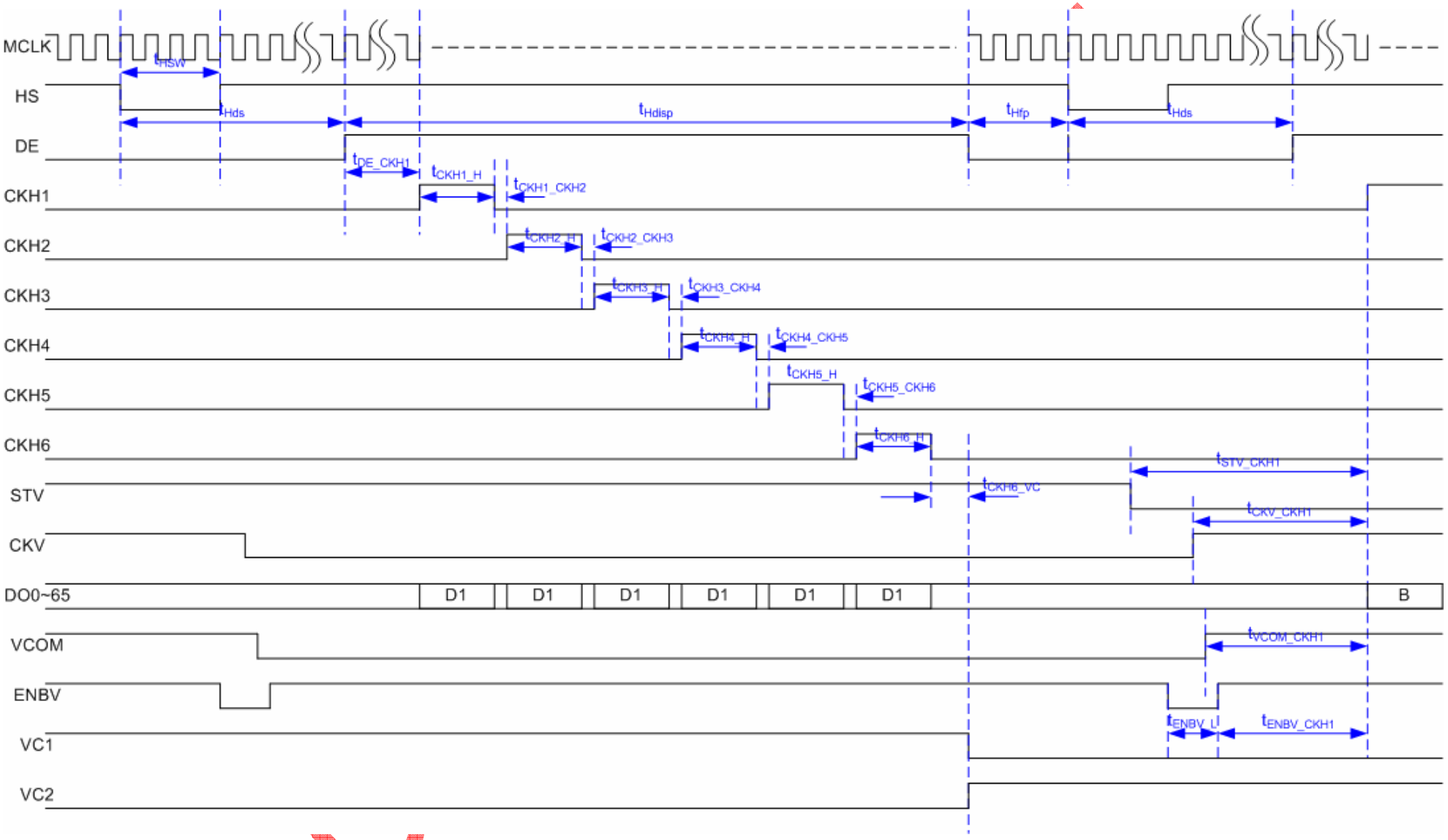


If VS falling edge is late after HS rising edge, it will cause the first valid data line to delay 1 t_H.



12.4 Parallel RGB OUTPUT SIGNAL TIMING CHART





12.5 DE MODE INPUT SIGNAL TIMING CHARACTERISTIC

12.5.1 132X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		132	132	132	t_{clk}
Vertical	Period	t_V		167	172	182	t_H
	Active	t_{Vdsip}		160	160	160	t_H

12.5.2 128X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		128	128	128	t_{clk}
Vertical	Period	t_V		167	172	182	t_H
	Active	t_{Vdsip}		160	160	160	t_H

12.5.3 128X128 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		128	128	128	t_{clk}
Vertical	Period	t_V		135	140	150	t_H
	Active	t_{Vdsip}		128	128	128	t_H

12.5.4 96X96 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		134	140	144	t_{clk}
	Active	t_{Hdisp}		96	96	96	t_{clk}
Vertical	Period	t_V		103	107	115	t_H
	Active	t_{Vdsip}		96	96	96	t_H

12.6 HS+VS MODE INPUT SIGNAL TIMING CHARACTERISTIC

12.6.1 132X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		132	132	132	t_{clk}
	Display start	t_{Hds}		18	—	—	t_{clk}
	Front porch	t_{Hfp}		16	—	—	t_{clk}
Vertical	Period	t_V		167	172	182	t_H
	Active	t_{Vdsip}		160	160	160	t_H
	Display start	t_{Vds}		6	—	—	t_H
	Front porch	t_{vfp}		1	—	—	t_H

12.6.2 128X160 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		128	128	128	t_{clk}
	Display start	t_{Hds}		18	—	—	t_{clk}
	Front porch	t_{Hfp}		20	—	—	t_{clk}
Vertical	Period	t_V		167	172	182	t_H
	Active	t_{Vdsip}		160	160	160	t_H
	Display start	t_{Vds}		6	—	—	t_H
	Front porch	t_{vfp}		1	—	—	t_H

12.6.3 128X128 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		166	176	182	t_{clk}
	Active	t_{Hdisp}		128	128	128	t_{clk}
	Display start	t_{Hds}		18	—	—	t_{clk}
	Front porch	t_{Hfp}		20	—	—	t_{clk}
Vertical	Period	t_V		135	140	150	t_H
	Active	t_{Vdsip}		128	128	128	t_H
	Display start	t_{Vds}		6	—	—	t_H
	Front porch	t_{vfp}		1	—	—	t_H

12.6.4 96X96 Mode

Item		Symbol	Conditions	Min.	Typ.	Max.	unit
Horizontal	Period	t_H		134	140	144	t_{clk}
	Active	t_{Hdisp}		96	96	96	t_{clk}
	Display start	t_{Hds}		18	—	—	t_{clk}
	Front porch	t_{Hfp}		20	—	—	t_{clk}
Vertical	Period	t_V		103	107	115	t_H
	Active	t_{Vdsip}		96	96	96	t_H
	Display start	t_{Vds}		6	—	—	t_H
	Front porch	t_{vfp}		1	—	—	t_H

12.7 DE MODE OUTPUT TIMING CHARACTERISTIC

12.7.1 128(132)X160 Mode

Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	16	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	5	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	16	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	5	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	16	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	5	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	16	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	5	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	16	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	5	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	16	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.7.2 128X128 Mode

Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	16	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	5	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	16	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	5	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	16	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	5	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	16	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	5	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	16	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	5	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	16	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.7.3 96X96 Mode

Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	13	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	3	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	13	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	3	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	13	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	3	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	13	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	3	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	13	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	3	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	13	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.8 HS+VS MODE OUTPUT TIMING CHARACTERISTIC

12.8.1 128(132)X160 Mode

Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	16	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	5	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	16	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	5	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	16	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	5	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	16	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	5	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	16	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	5	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	16	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.8.2 128X128 Mode

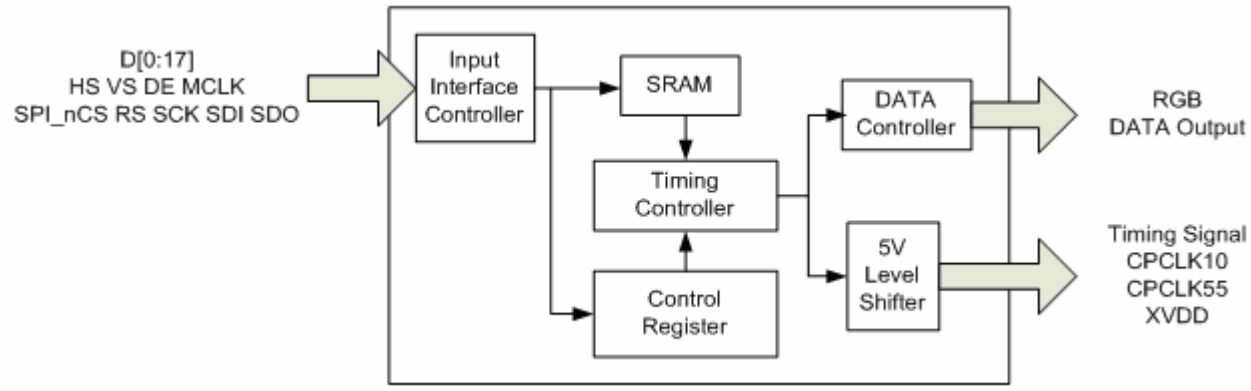
Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	16	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	5	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	16	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	5	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	16	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	5	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	16	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	5	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	16	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	5	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	16	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.8.3 96X96 Mode

Item	Symbol	Conditions	Min.	Typ.	Max.	unit	Note
DE to CKH3	t_{DE_CKH3}	—	—	4	—	t_{clk}	
CKH1 H time	t_{CKH1_H}	—	—	13	—	t_{clk}	
CKH3 to CKH2	t_{CKH1_CKH2}	—	—	3	—	t_{clk}	
CKH2 H time	t_{CKH2_H}	—	—	13	—	t_{clk}	
CKH2 to CKH3	t_{CKH2_CKH3}	—	—	3	—	t_{clk}	
CKH3 H time	t_{CKH3_H}	—	—	13	—	t_{clk}	
CKH3 to CKH4	t_{CKH3_CKH4}	—	—	3	—	t_{clk}	
CKH4 H time	t_{CKH4_H}	—	—	13	—	t_{clk}	
CKH4 to CKH5	t_{CKH4_CKH5}	—	—	3	—	t_{clk}	
CKH5 H time	t_{CKH5_H}	—	—	13	—	t_{clk}	
CKH5 to CKH6	t_{CKH5_CKH6}	—	—	3	—	t_{clk}	
CKH6 H time	t_{CKH6_H}	—	—	13	—	t_{clk}	
CKH6 to VC1/2	t_{CKH6_VC}	—	—	3	—	t_{clk}	
ENBV L time	t_{ENBV_L}	—	—	13	—	t_{clk}	
ENBV to CKH1	t_{ENBV_CKH1}	—	—	6	—	t_{clk}	
VCOM to CKH1	t_{VCOM_CKH1}	—	—	12	—	t_{clk}	
STV to CKH1	t_{STV_CKH1}	—	—	19	—	t_{clk}	
CKV to CKH1	t_{CKV_CKH1}	—	—	14	—	t_{clk}	

12.9 PARALLEL RGB OPERATION MODE

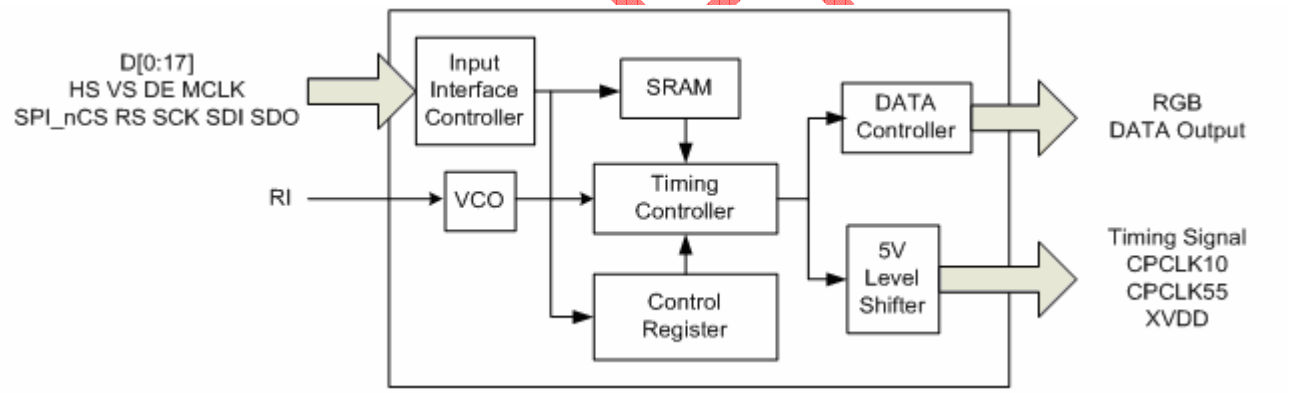
12.9.1 Moving(Normal) Mode



Note:

1. RGB DATA always input.
2. Operation clock is based on external MCLK signal.
3. CPCLK10、PCLK55、XVDD output.

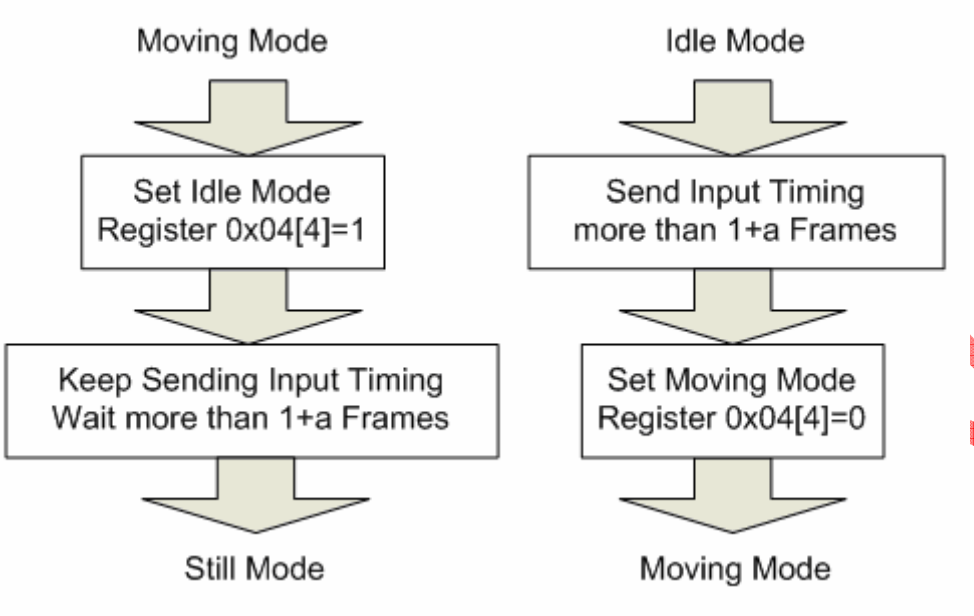
12.9.2 Still(Idle) Mode



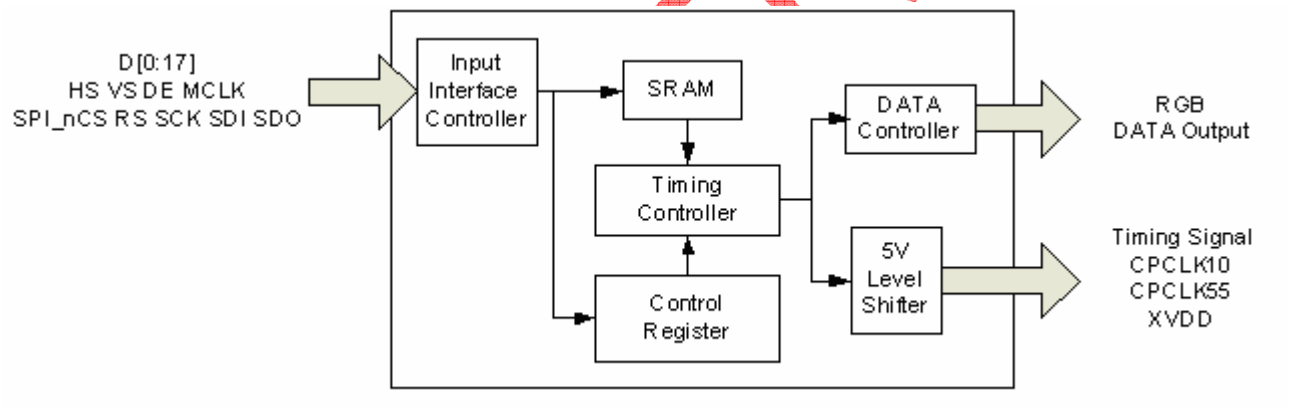
Note:

1. Parallel RGB interface is used for the SRAM update and internal operation clock is based on VCO clock.
2. CPCLK10、PCLK55、XVDD output.

12.9.3 Moving(Normal) Mode and Still(Idle) Mode Switching



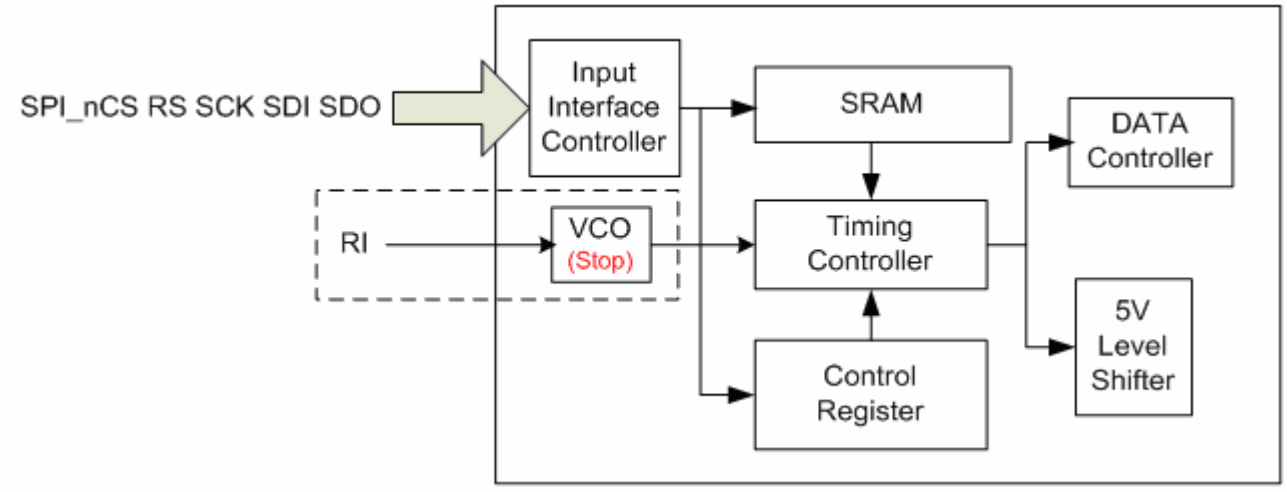
12.9.4 Partial Mode



Note:

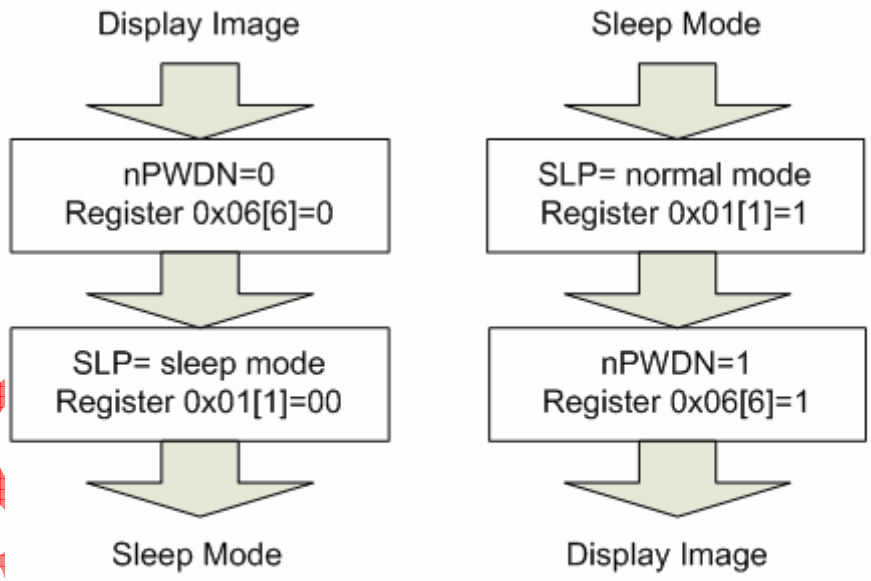
1. Only display area, other area no signal and no display
2. When full panel display mode change to partial display mode, ASIC must scan two frame white data at non-partial(no display) area.
3. CPCLK10、PCLK55、XVDD output

12.9.5 Sleep Mode

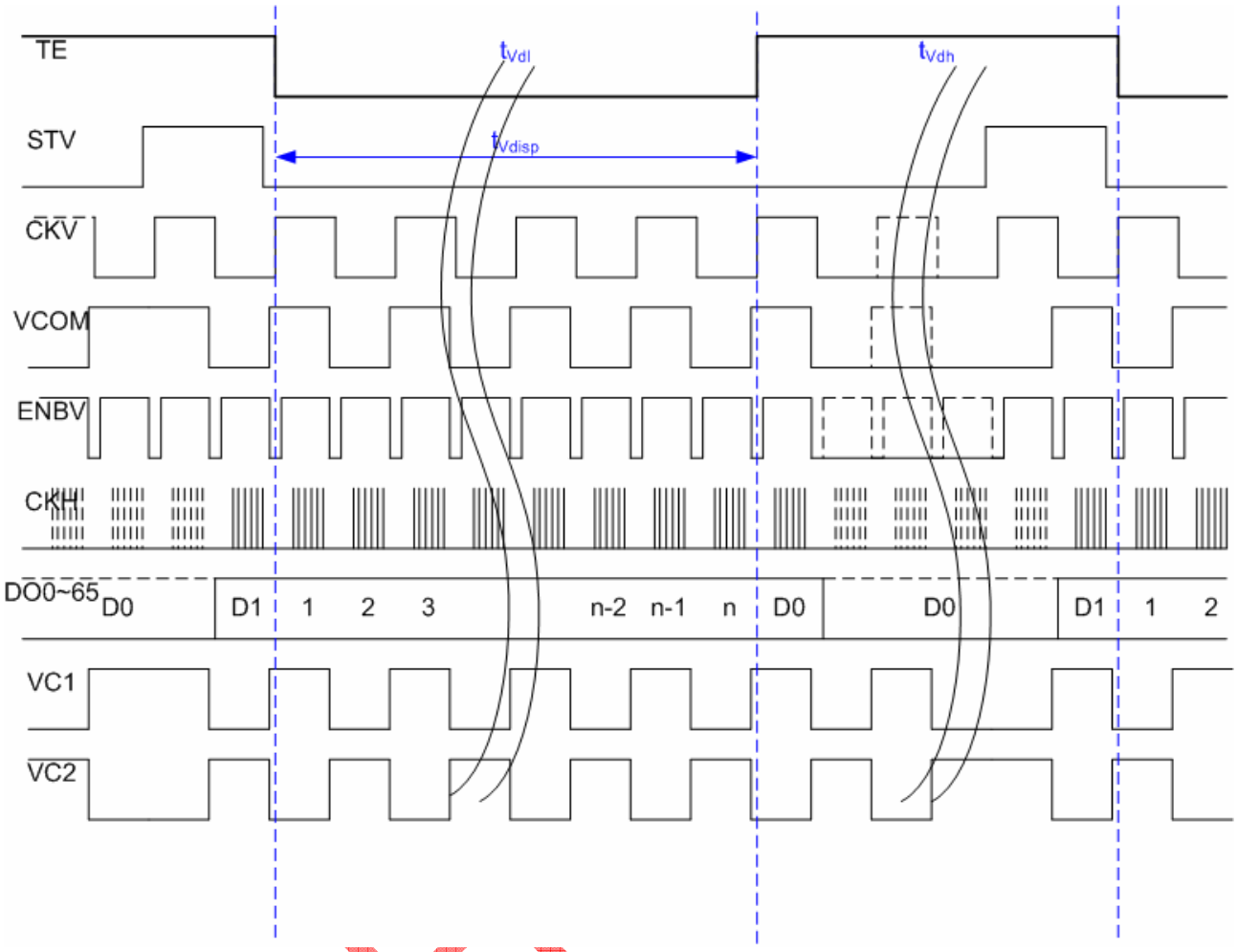


Note:

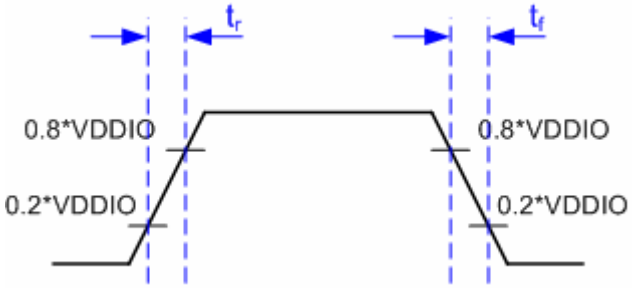
1. SRAM data can be retained.
2. The VCO is stopped in sleep mode.
3. The power DVDD is not off in sleep mode.
4. CPCLK10、PCLK55、XVDD off



13. Tearing Effect Output

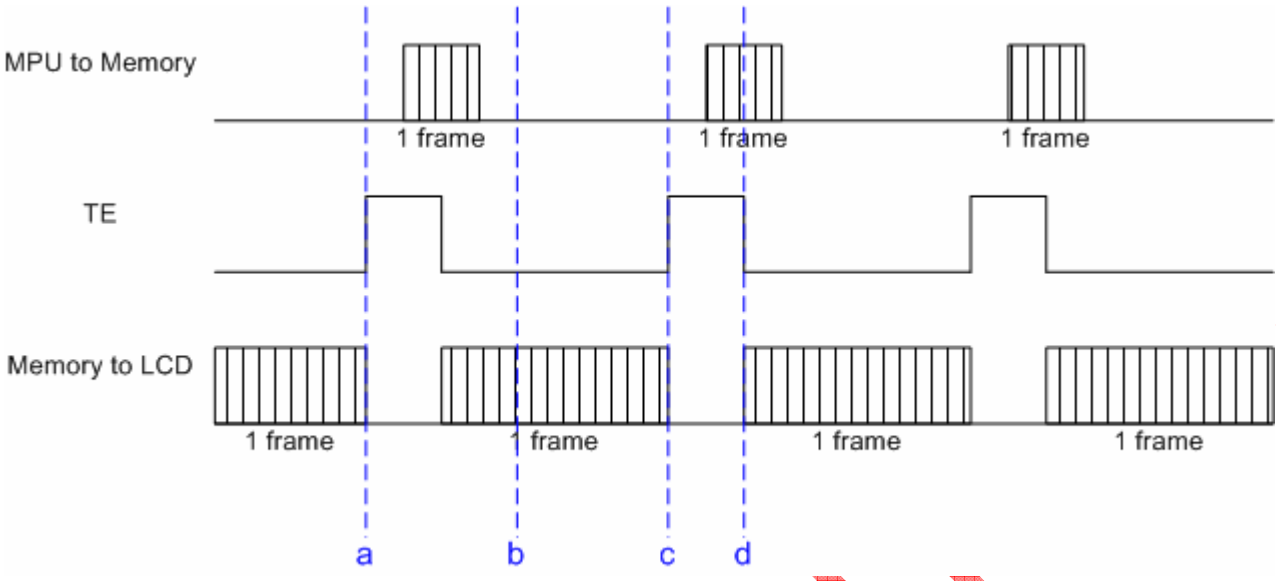


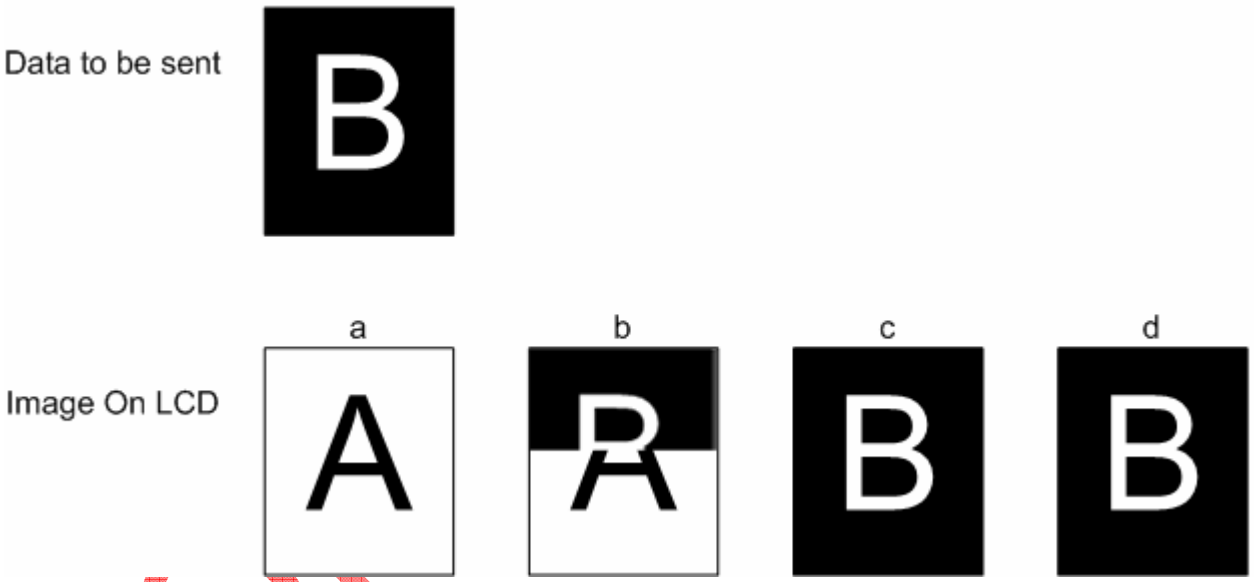
Symbol	min	Max.	unit
t_{vdh}	TBD	-	ms
t_{vdl}	1000	-	us



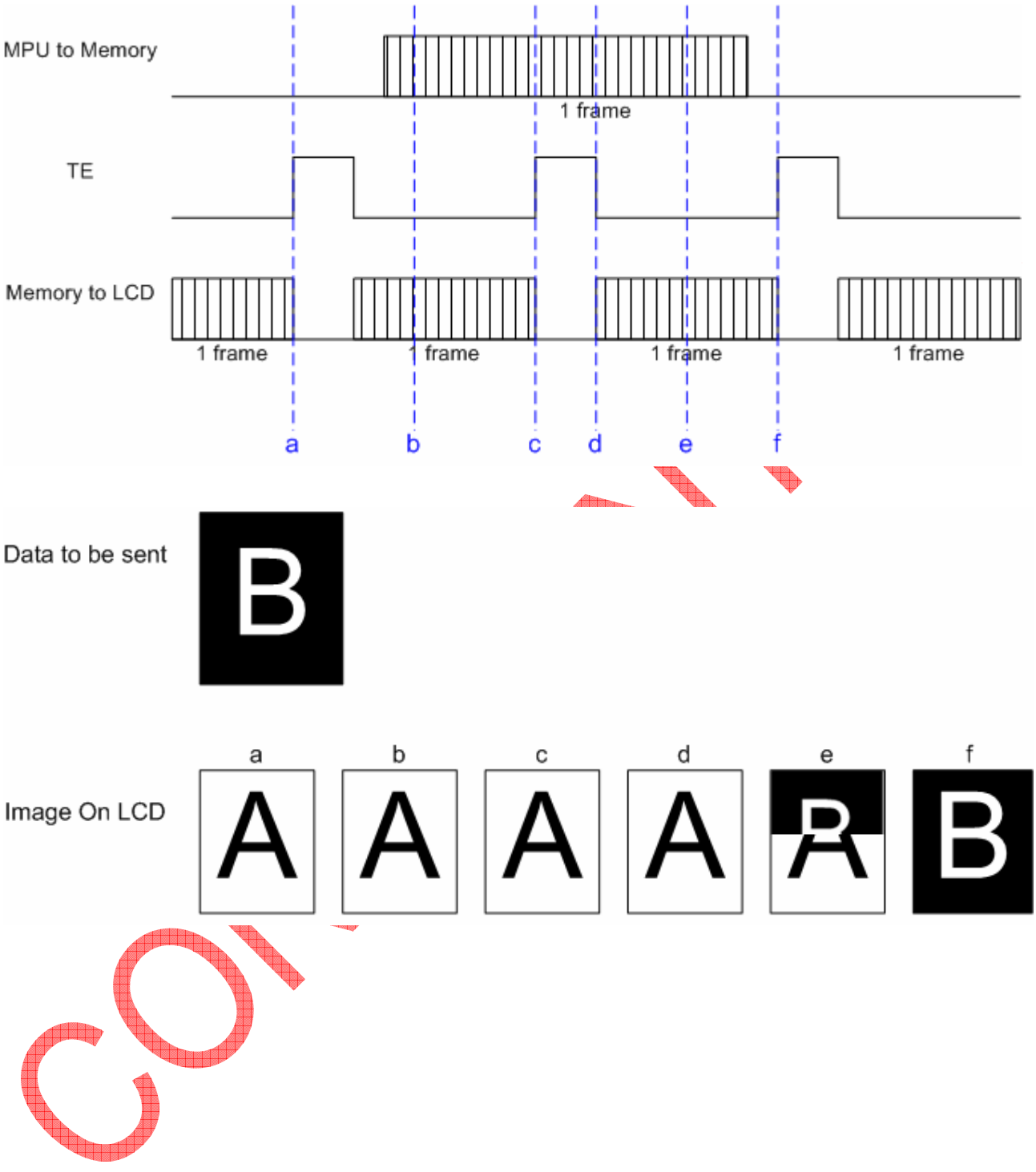
The rising time and falling of TE are stipulated to be equaled to or less than 15 ns.

13.1 Writing Speed of MPU is Faster than Panel Read

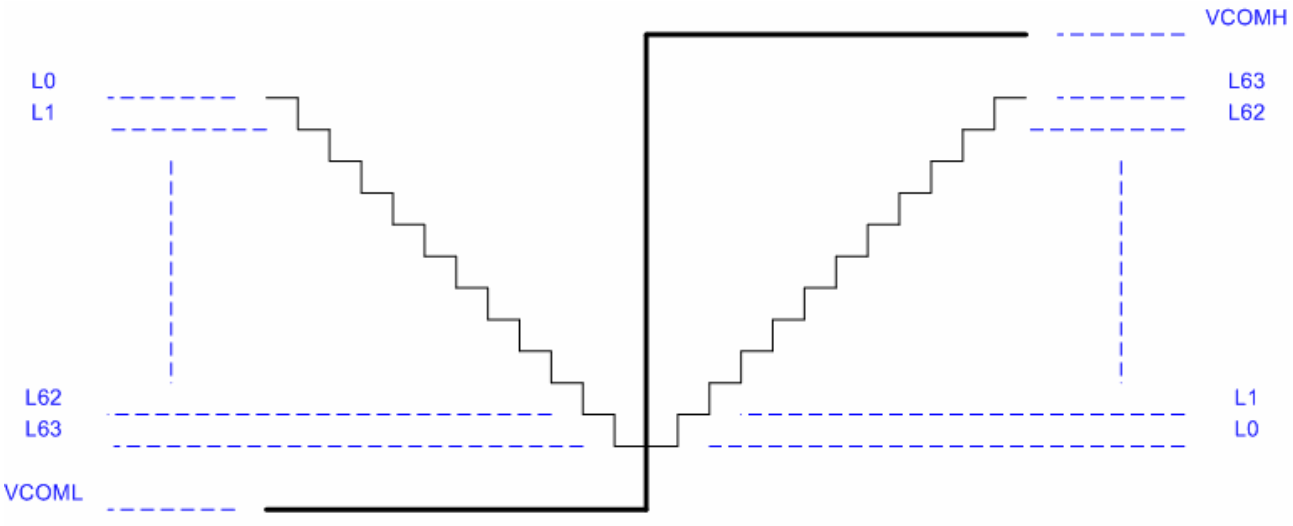




13.2 Writing Speed of MPU is Slower than Panel Read



14. OUTPUT VIODEO WAVEFORM



15. ANALOG OUTPUT DYNAMIC CHARACTERISTIC

R,G,B output characteristic(128(132)*160)

Item	symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	t1	1% - 99%	—	—	3	us
fall time	t2	99% - 1%	—	—	3	us

R,G,B output characteristic(128*128)

Item	symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	t1	1% - 99%	—	—	5	us
fall time	t2	99% - 1%	—	—	5	us

R,G,B output characteristic(96*96)

Item	symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	t1	1% - 99%	—	—	TBD	us
fall time	t2	99% - 1%	—	—	TBD	us

VCOM output characteristic

Item	symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	t1	1% - 99%	—	—	4	us
fall time	t2	99% - 1%	—	—	4	us

VC1 and VC2 output characteristic

Item	symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	t1	1% - 99%	—	—	5	us
fall time	t2	99% - 1%	—	—	5	us

16. ELECTRICAL CHARACTERISTIC

16.1 MAXIMUM RATING at Ta=25℃

Item	Symbol	Rating	Unit
Power supply voltage	VDD2.8	-0.3 to +4.6	V
Input Voltage	Vt	-0.3 to VDDIO+0.3	V
Operating temperature	Topr	-20~ +70	℃
Storage temperature	Tstg	-40 ~ +125	℃

16.2 OPERATION CONDITION at Ta=25℃

Parameter	Symbol	Conditions	Ratings			Unit
DC/DC Voltage	VDD2.8	Input Voltage for DC/DC	2.5	2.8	3.3	Volt
	DVDD	Logic Power	1.6	1.8	2.0	Volt
	AVDD1	Analog Power	5.1	5.2	5.3	Volt
	AVDD2	VCOM Power	4.65	4.70	4.75	Volt
	AVDD3	Gamma Circuit Power (Select by AVDD3_SEL)	4.65	4.70	4.75	Volt
			4.15	4.20	4.25	Volt
	VDDIO	Input Voltage for I/O	1.6	2.8	3.3	Volt

17. LEVEL SHIFT ELECTRICAL CHARACTERISTIC

17.1 MAIXMUM RATING at Ta=25℃

Symbol	Conditions	Min.	Typ.	Max.	Unit
VSS		-0.3	--	+0.3	Volt
AVDD1		-0.3	--	+6	Volt
DVDD		-0.3	--	+2.8	Volt

17.2 DC ELECTRICAL CHARACTERISTIC

VDD2.8=2.5V~3.3V, Topr= -20~ 70℃

Paramenter	Symbol	Condition	Min.	Typ.	Max.
STV CKV ENBV CSV GAS CKH/1/2/3/4/5/6 CPCLK55/10	V_{OH}	$I_{out(max)}$=10uA	0.9xAVDD1	AVDD1	-
	V_{OL}	$I_{out(max)}$=10uA	-	0	0.1xAVDD1
VC1/2*	V_{OH}		0.95xVCH	VCH	1.05xVCH
	V_{OL}		-	0	0.05xVCH

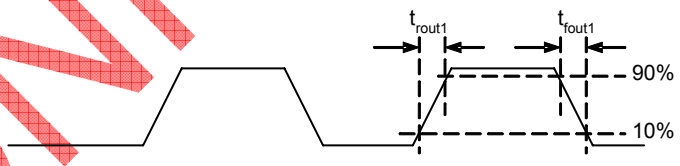
*VCH is the high level voltage of VC1 and VC2. The VCH can be adjusted by VC1/2 Control(0x7A)[5:3].

17.3 AC ELECTRICAL CHARACTERISTIC

Control Signal output characteristic

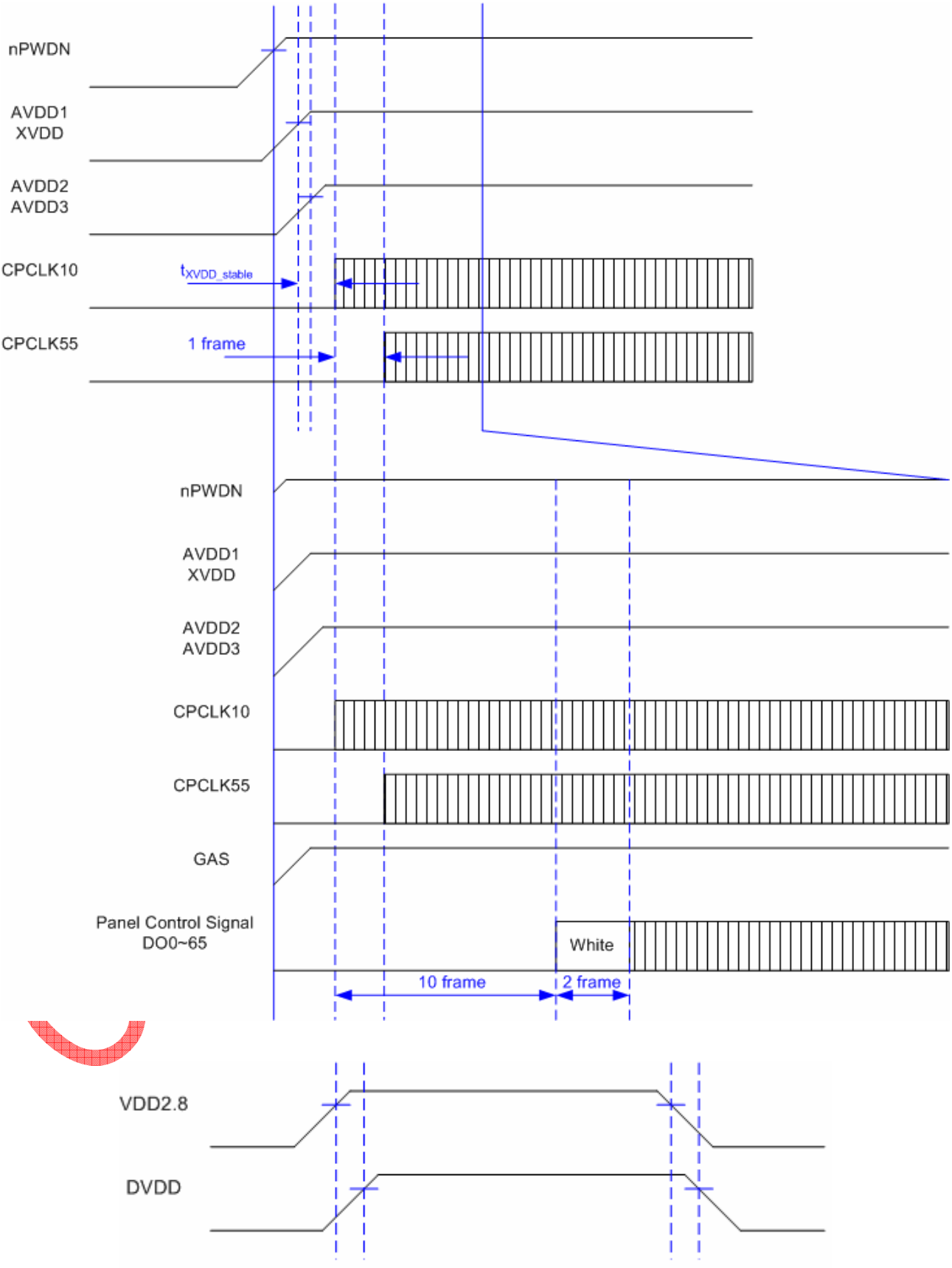
STV CKV ENBV CSV GAS CKH/1/2/3/4/5/6 CPCLK55/10

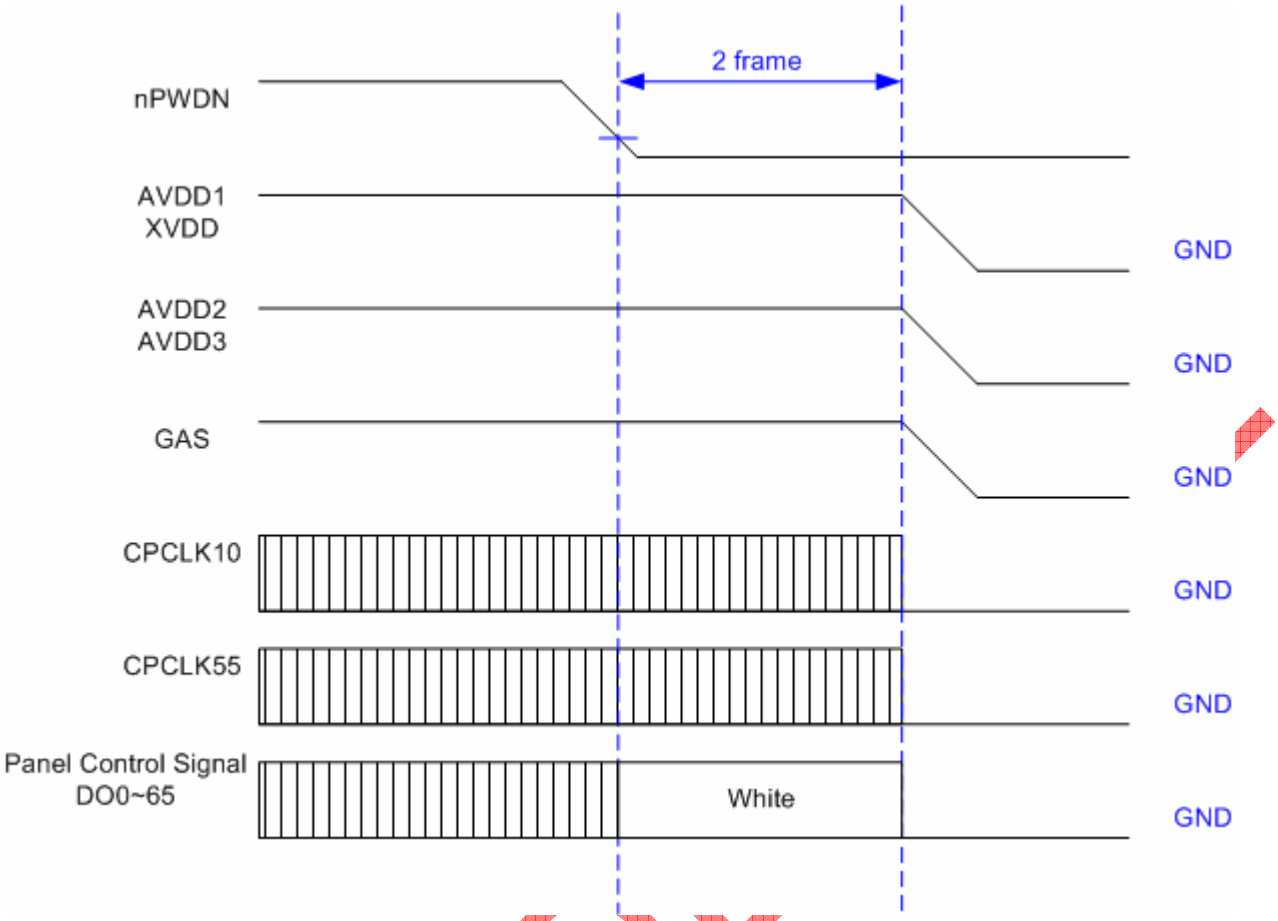
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Rise time	T_{rout1}	-	65	115	ns
Fall time	T_{fout1}	-	65	115	ns

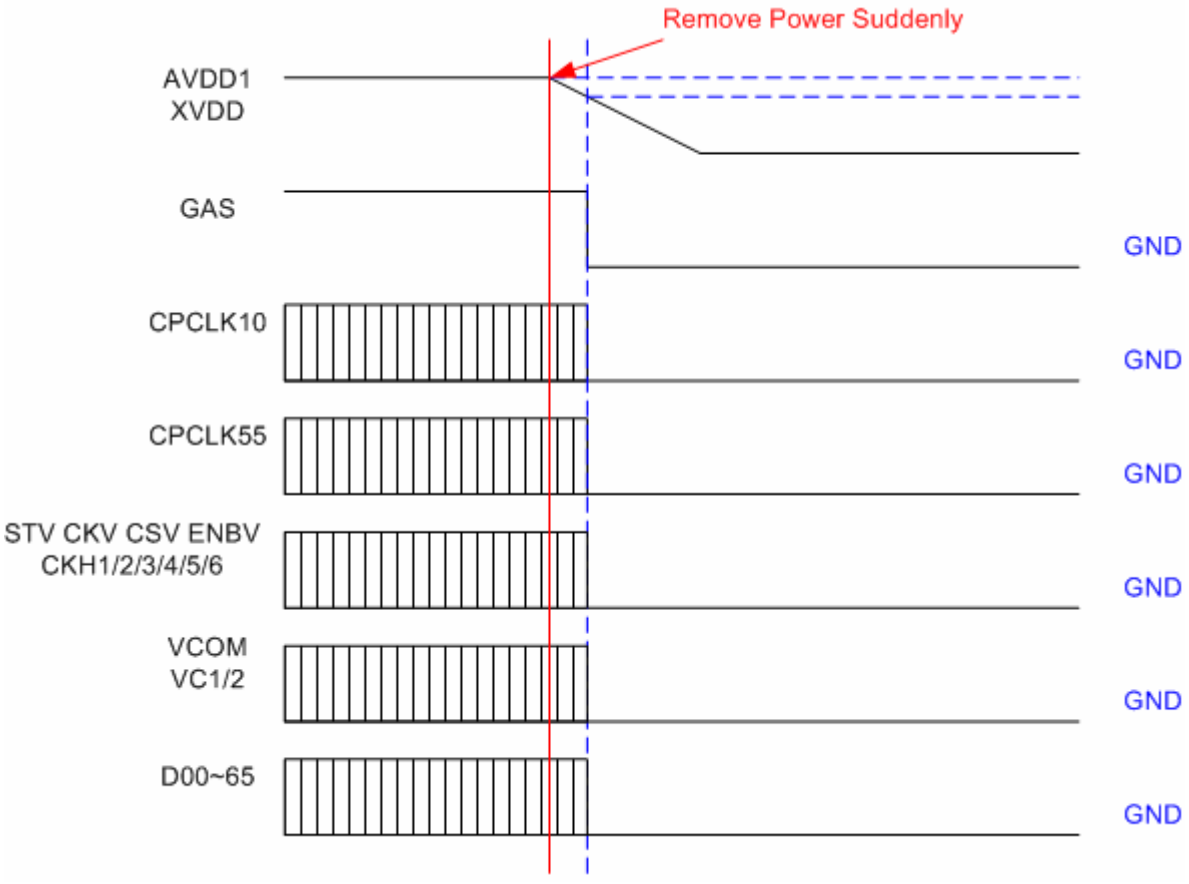


18. DC/DC CONVERTER

18.1 POWER SEQUENCE







19. APPLICATION CIRCUIT

19.1 APPLICATION CIRCUIT