REV	Description	Date
V1.0	First Release	2016-7-12

AX7010/AX7020 Schematics

ZYNQ硬件平台

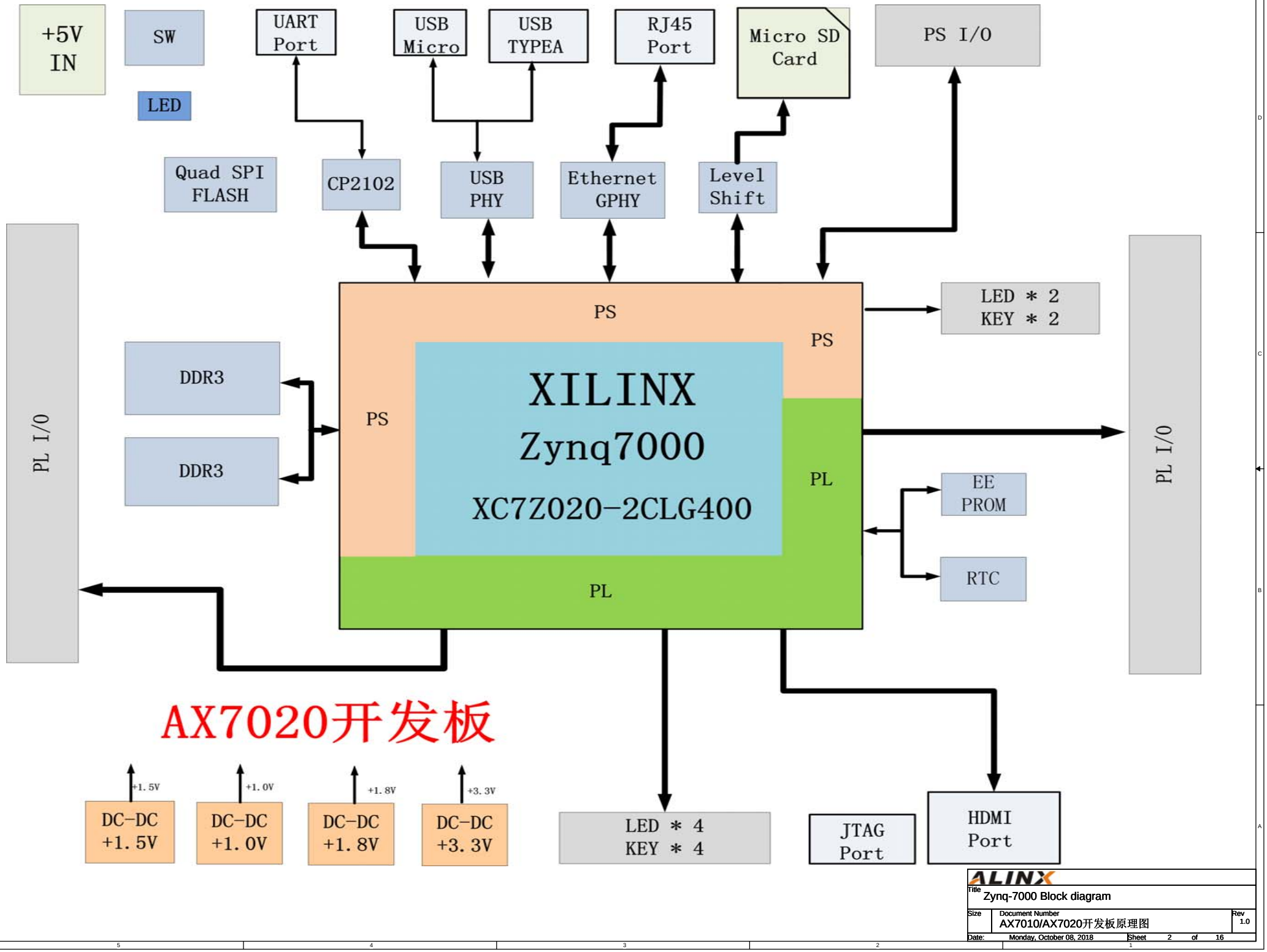
Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
Page06	Zynq-7000 Bank502
Page07	Zynq-7000 Power
Page08	DDR3
Page09	GPHY
Page10	USB OTG
Page11	FLASH, RTC, EEPROM
Page12	LED, KEY
Page13	UART, SD
Page14	HDMI
Page15	EXTEND IO
Page16	POWER

ALINX

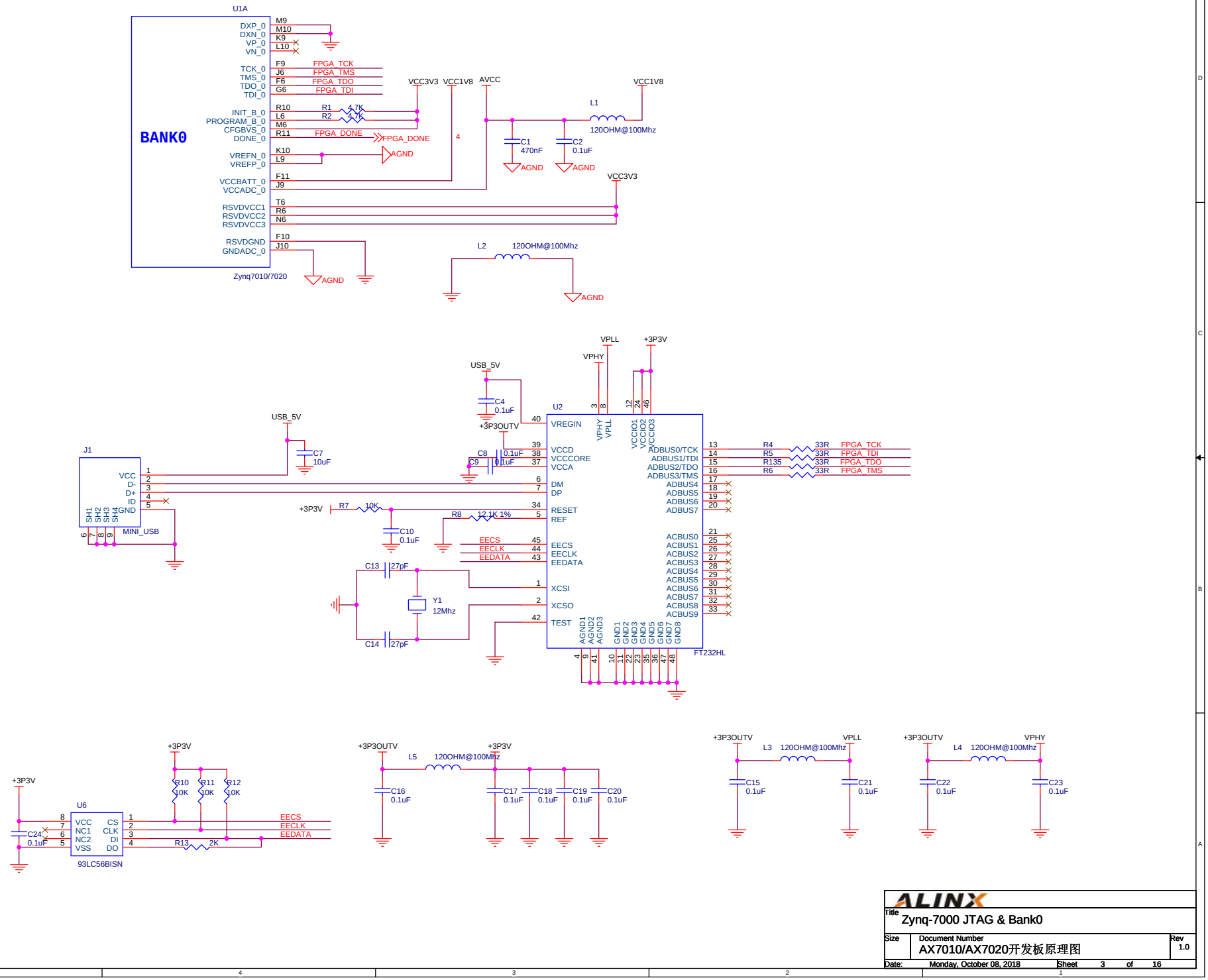
Title: Zynq-7000 Cover Page

Size | Document Number: AX7010/AX7020开发板原理图 | Rev: 1.0

Date: Monday, October 08, 2018 | Sheet 1 of 16

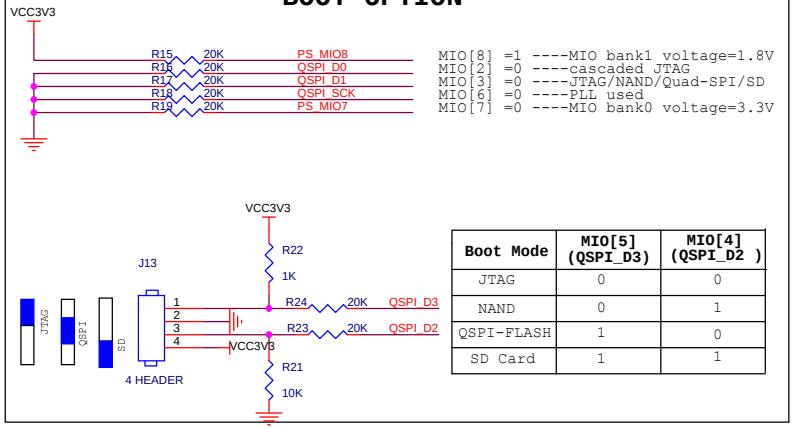


ALINX		
Title	Zynq-7000 Block diagram	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 2 of 16	



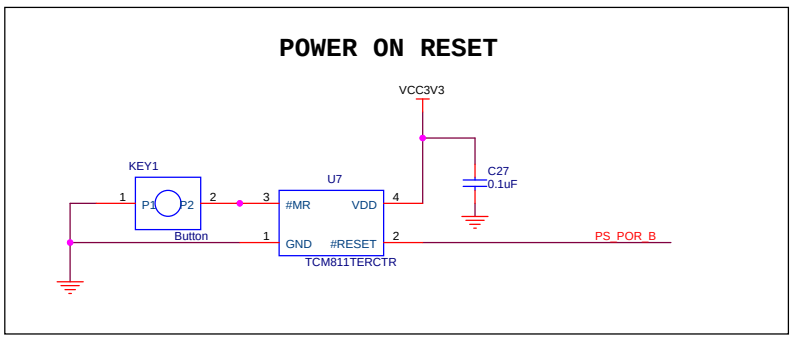
Title	Zynq-7000 JTAG & Bank0
Size	
Document Number	AX7010/AX7020开发板原理图
Rev	1.0
Date:	Monday, October 08, 2018
Sheet	3 of 16

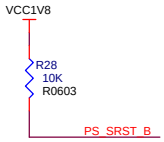
BOOT OPTION

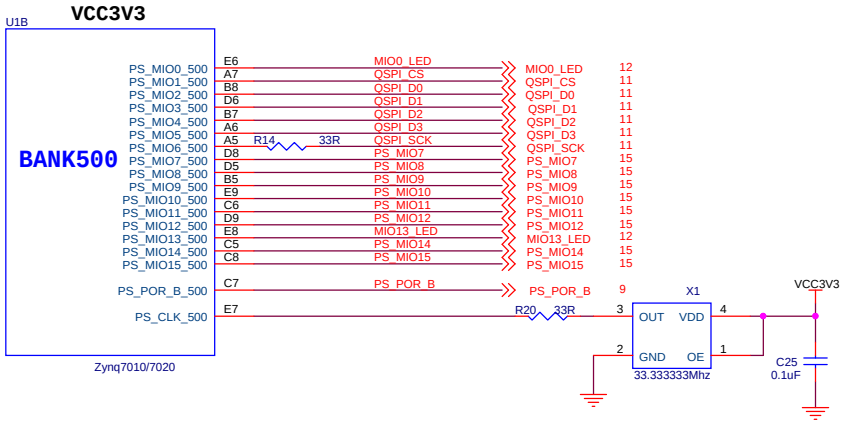


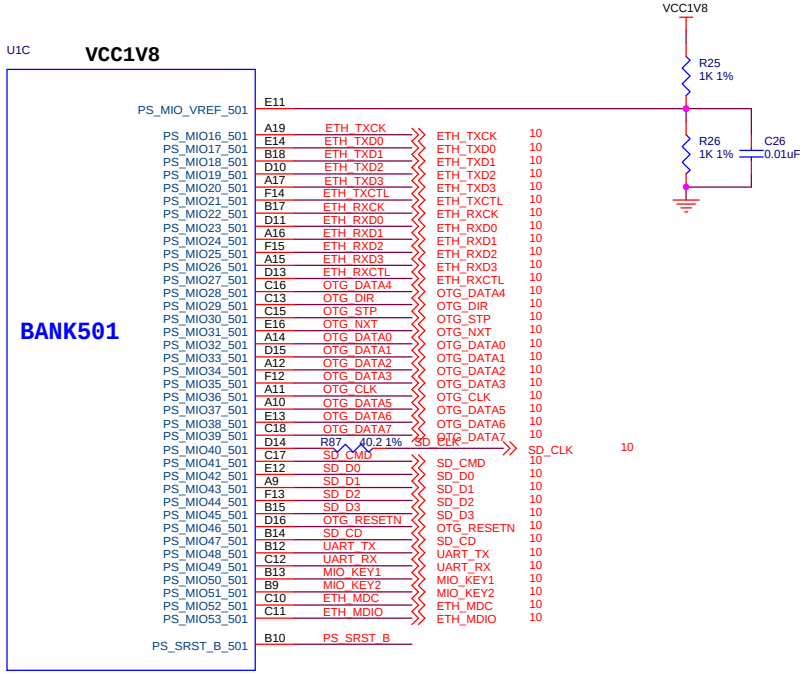
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET



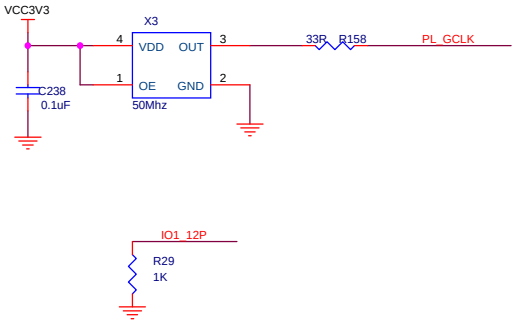


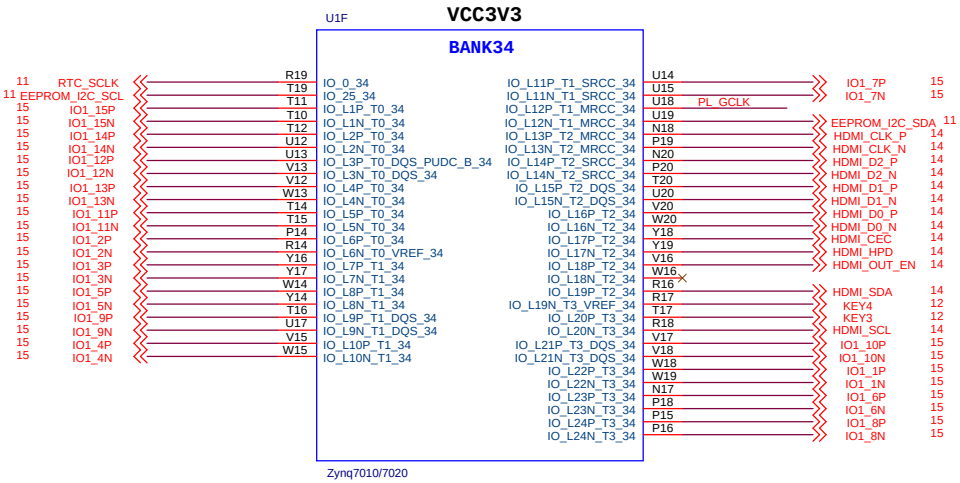


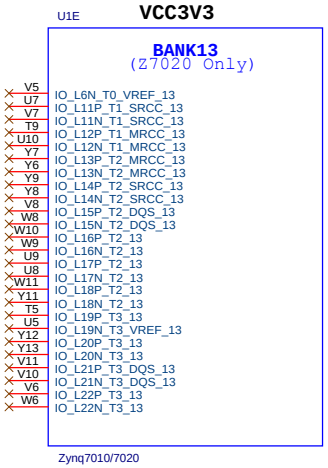


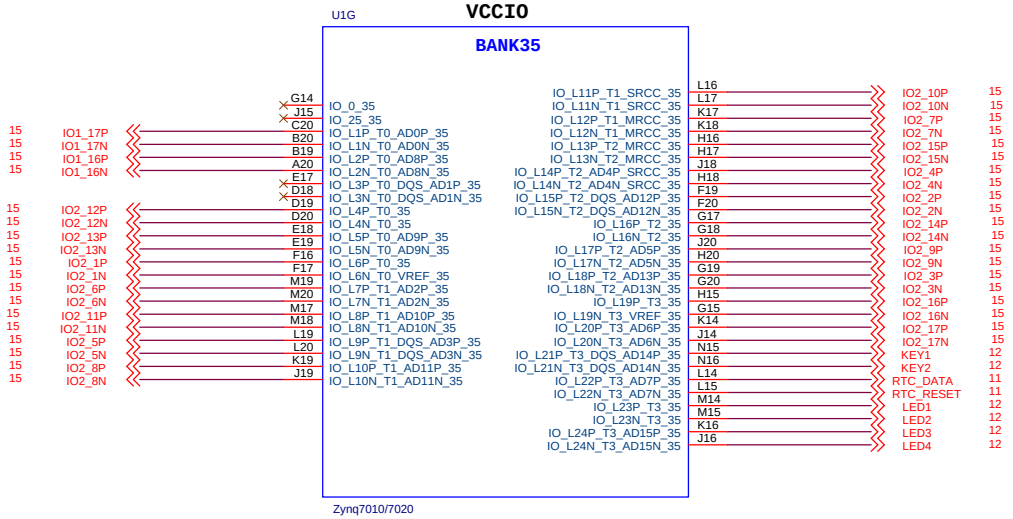
ALINX

Title	Zynq-7000 PS MIO	
Size	Document Number: AX7010/7020 开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 4 of 16	







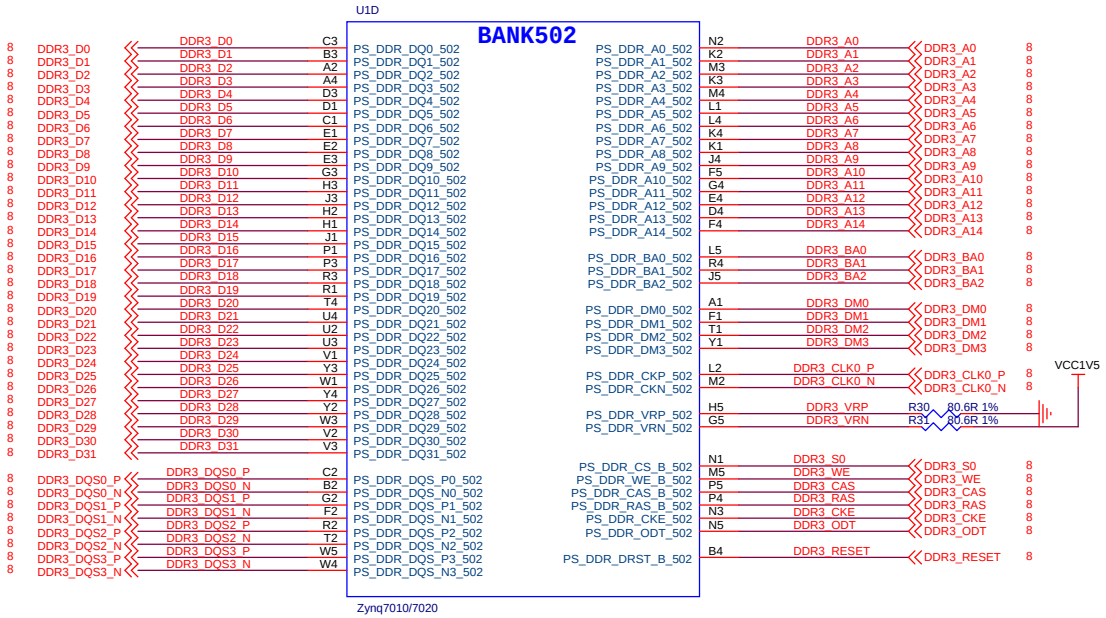


ALINX

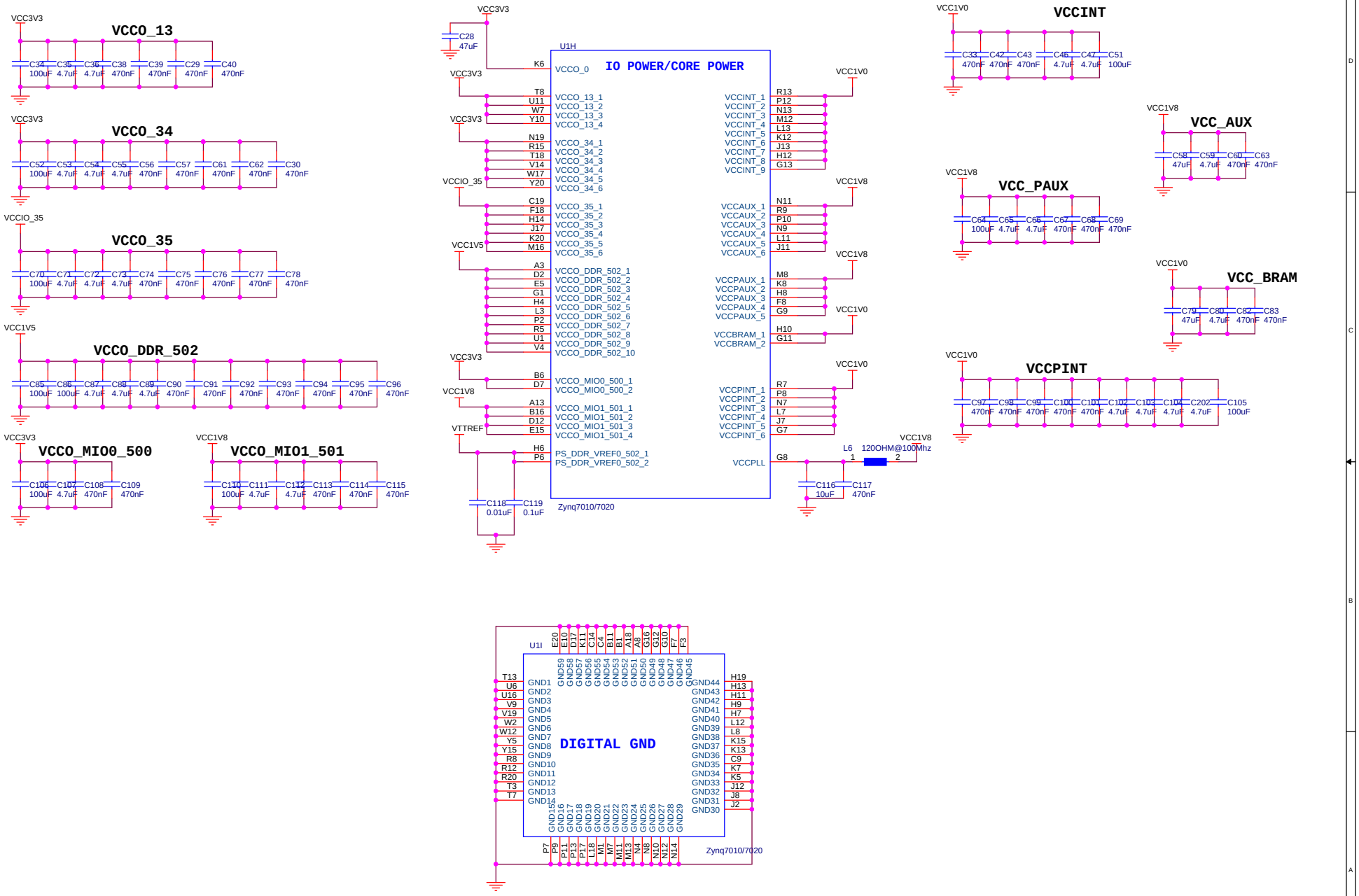
Title: Zynq-7000 Bank13 & 34 & 35

Size	Document Number	Rev
	AX7010/AX7020开发板原理图	1.0

Date: Monday, October 08, 2018 Sheet 5 of 16



Title	Zynq-7000 Bank502
Size	
Document Number	AX7010/AX7020开发板原理图
Rev	1.0
Date:	Monday, October 08, 2018
Sheet	6 of 16

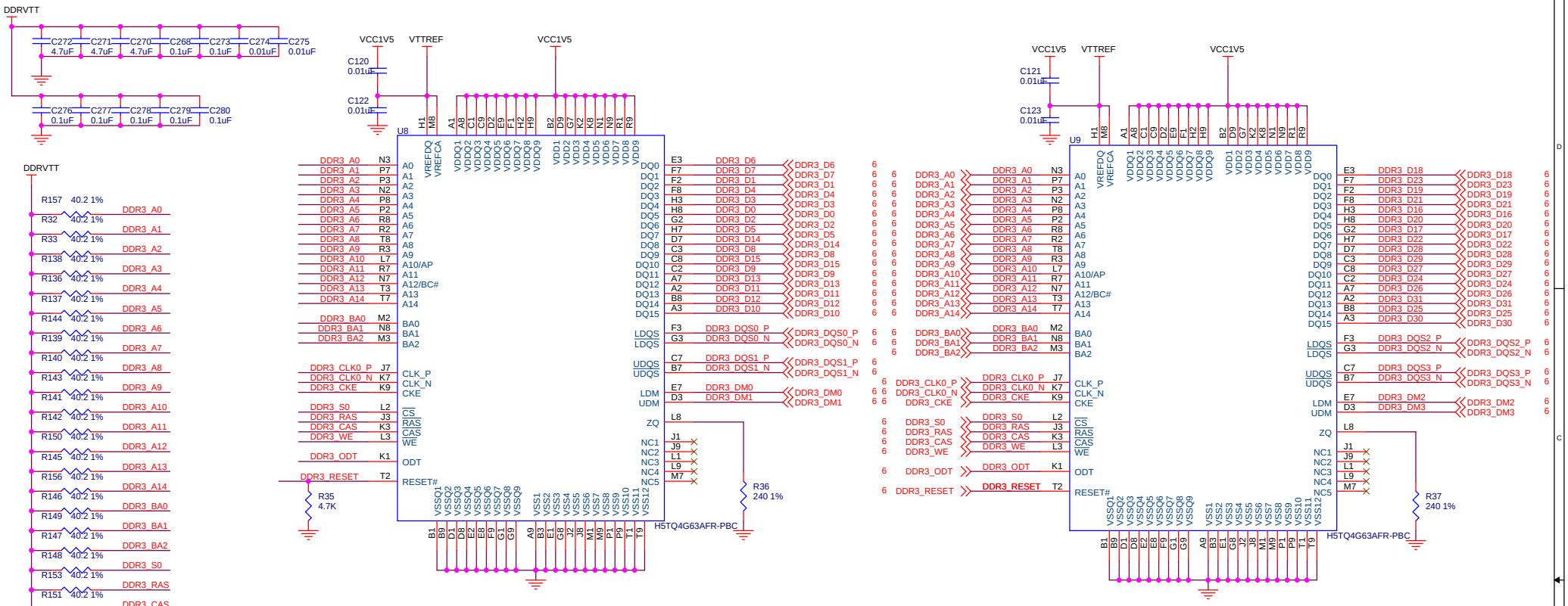


ALINX

Title: Zynq-7000 Cover Page

Size	Document Number	Rev
	AX7010/AX7020开发板原理图	1.0

Date: Monday, October 08, 2018 Sheet 7 of 16



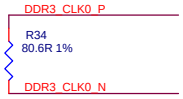
为了PCB走线方便，DDR3数据线组内（DQS除外）可以任意交换。
XILINX 的UG933文档的PAGE66有以下说明：

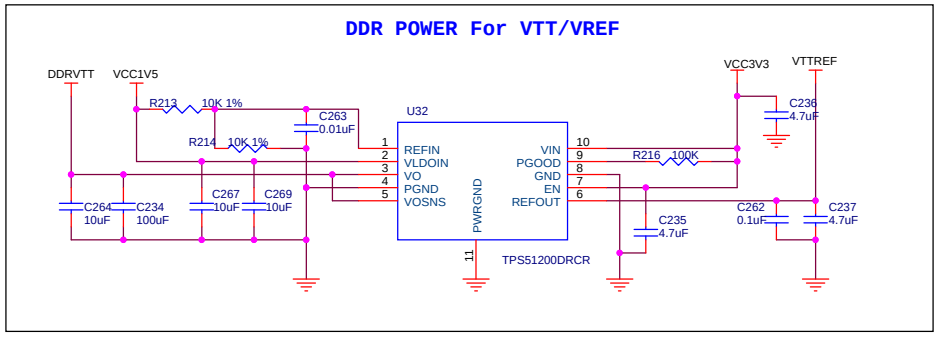
XILINX
ALL PROGRAMMABLE

Chapter 5: **Processing System (PS) Power and Signaling**

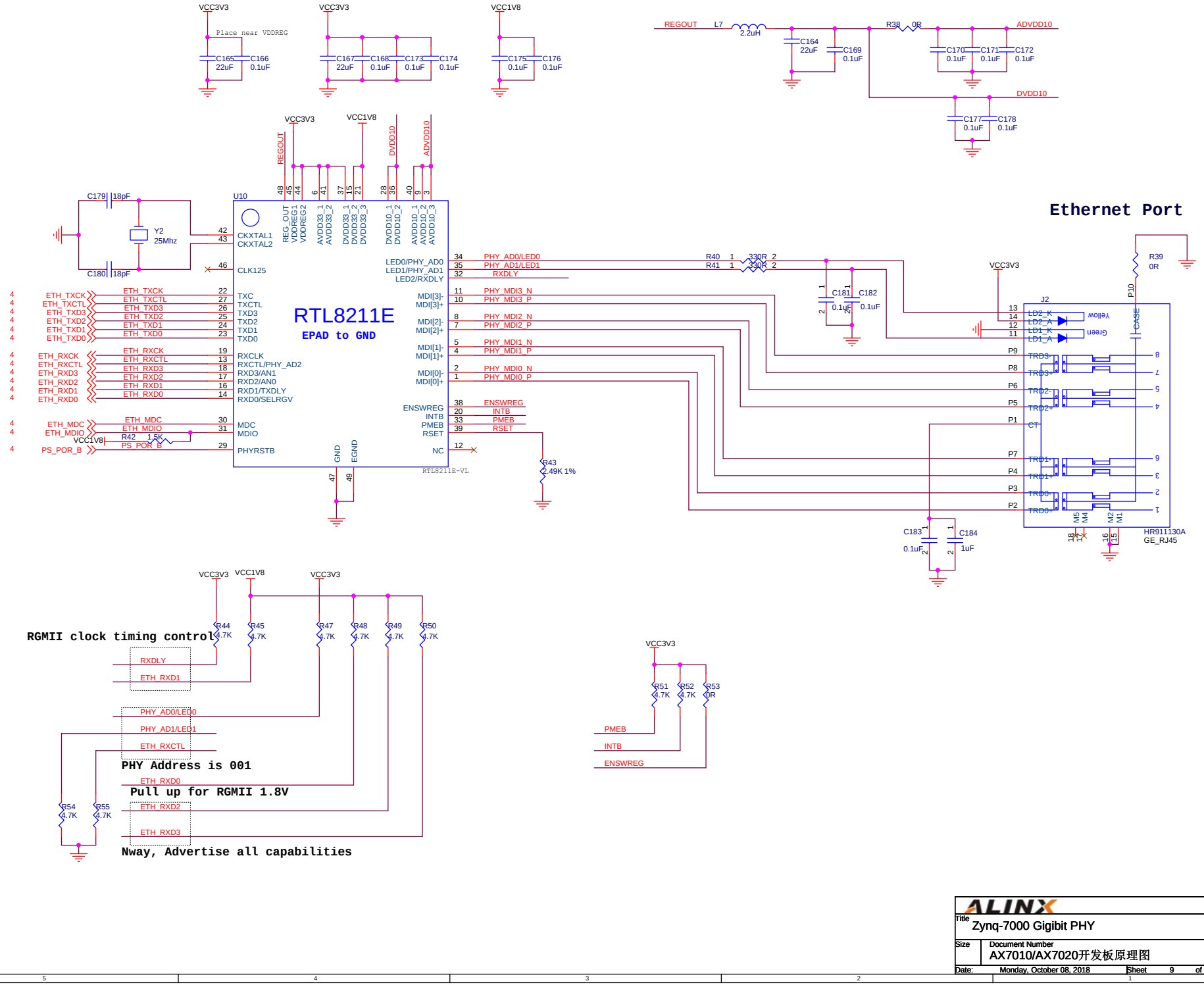
Table 5-12 shows the recommended routing topologies. Byte and bit swapping is allowed to facilitate PCB routing, except for LPDDR2, which specifically forbids swapping. When swapping bits, keep all bits within the same byte group.

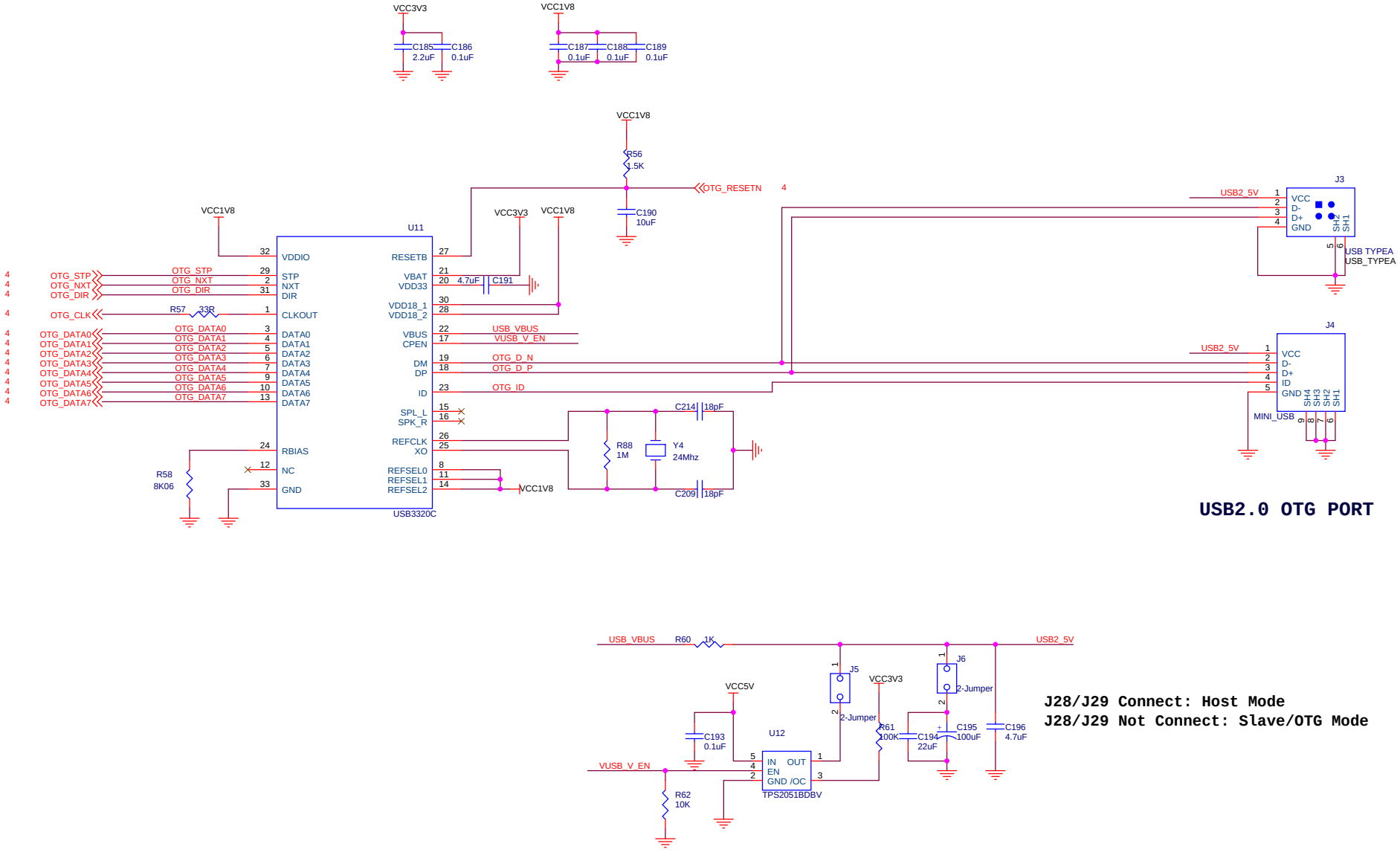
Table 5-12: **DDR Routing Topology**



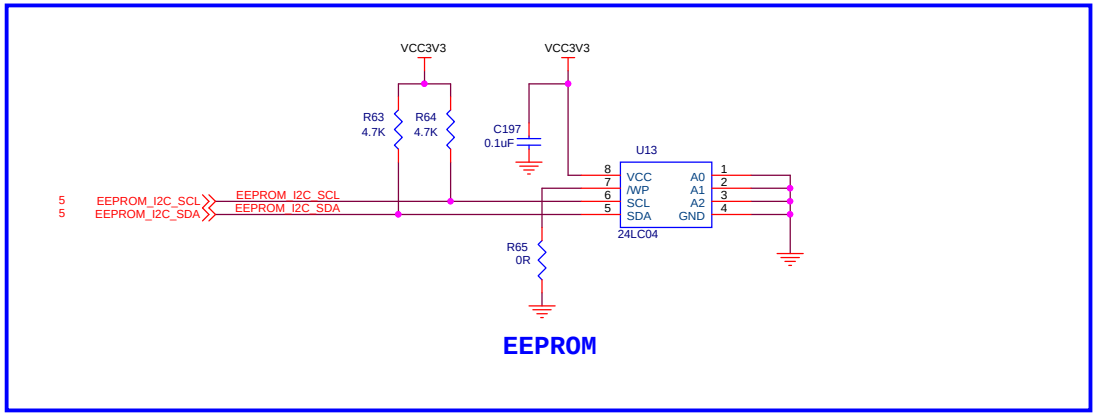


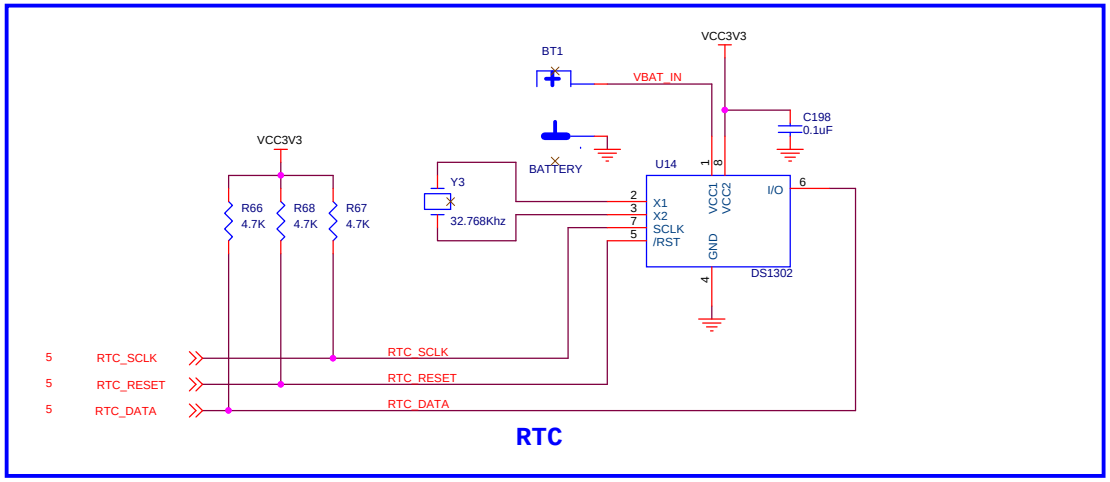
Title	Zynq-7000 DDR
Size	Document Number: AX7010/AX7020开发板原理图
Rev	1.0
Date:	Monday, October 08, 2018
Sheet	8 of 16

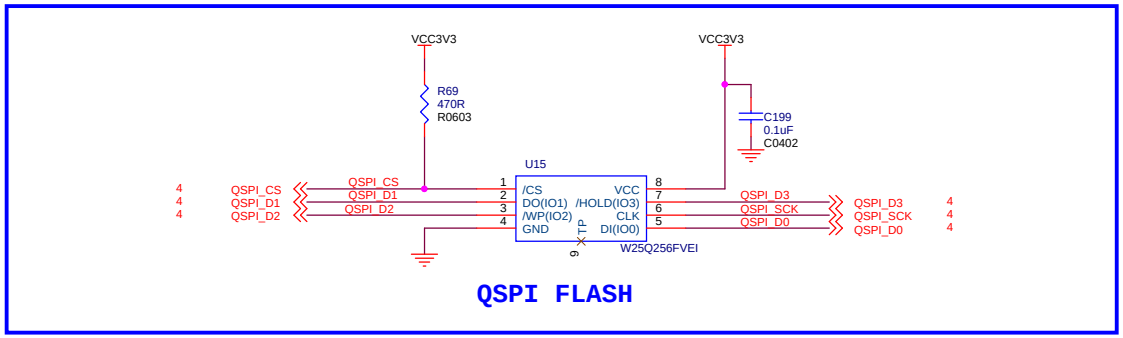

Ethernet Port
RTL8211E
EPAD to GND
RTL8211E-VL
RGMII clock timing control
PHY Address is 001
Pull up for RGMII 1.8V
Nway, Advertise all capabilities
HR911130A
GE_RJ45
Title
Zynq-7000 Gigibit PHY
Size
Document Number
AX7010/AX7020开发板原理图
Rev
1.0
Date:
Monday, October 08, 2018
Sheet
9
of
16



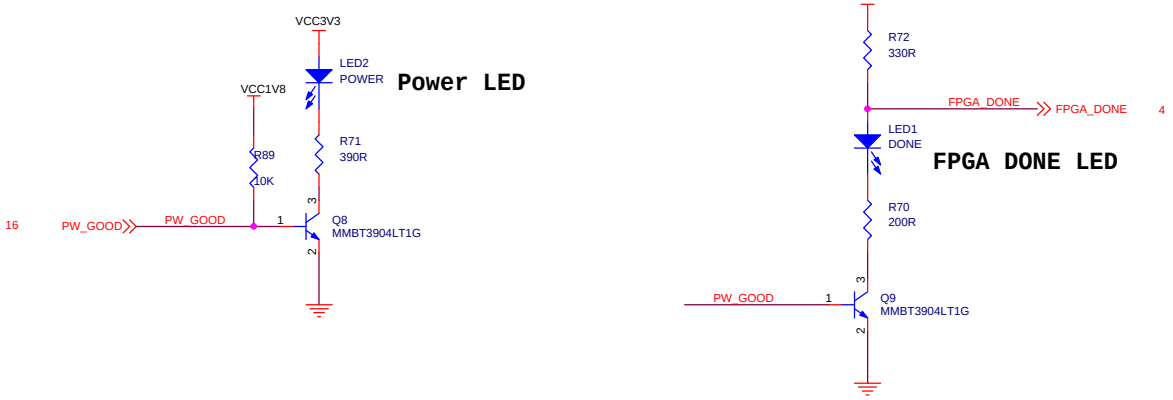
Title	Zynq-7000 OTG USB	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 10 of 16	

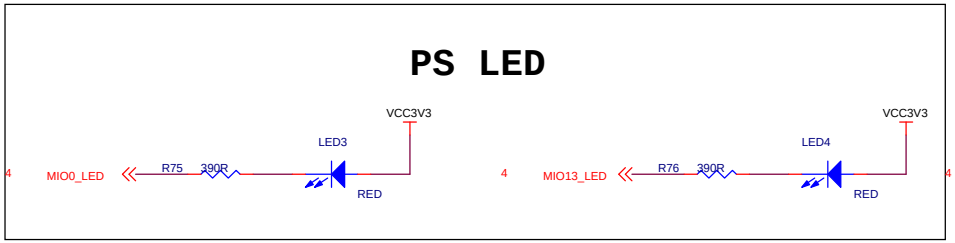


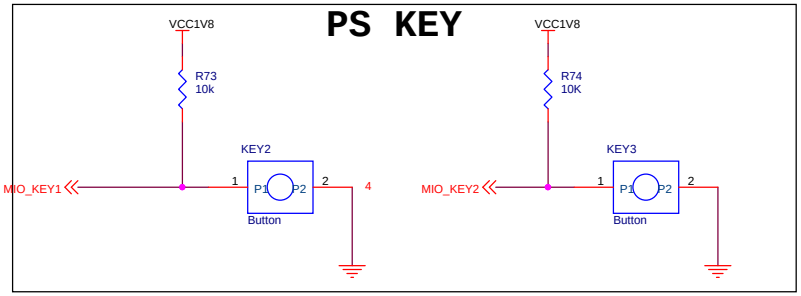


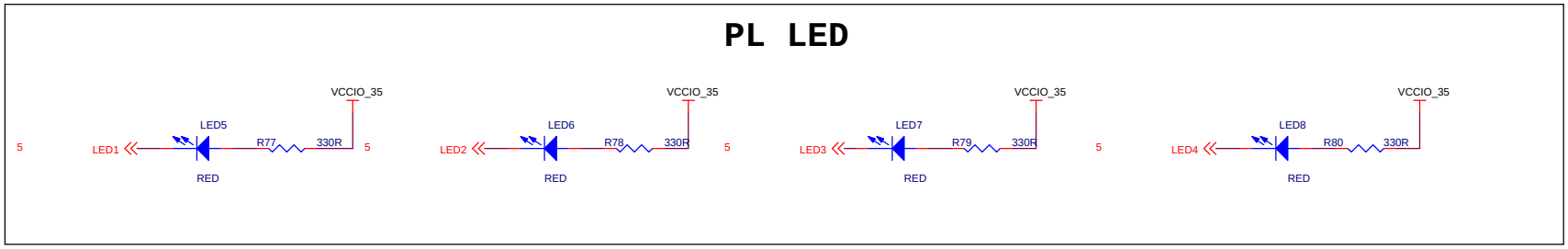


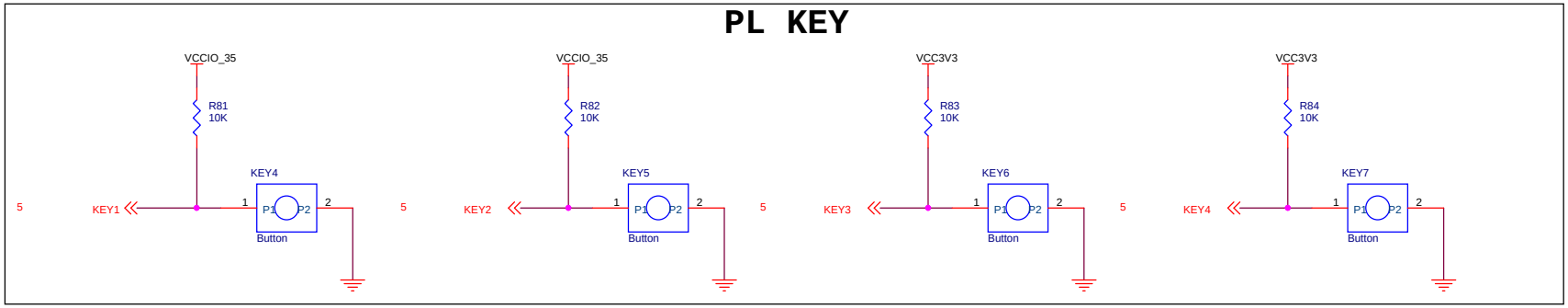
Title	Zynq-7000 QSPI & RTC & EEPROM	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 11 of 16	







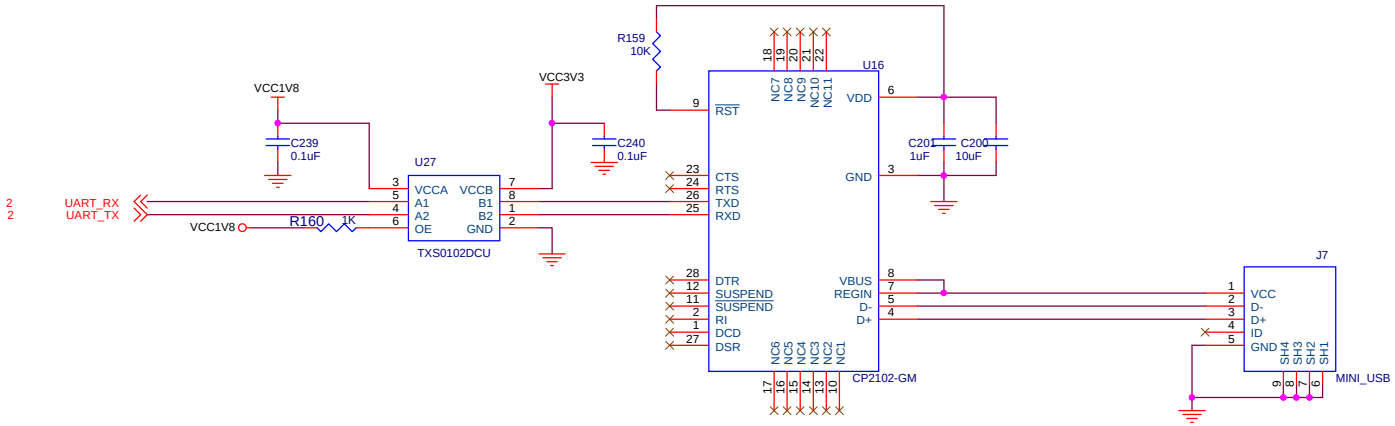




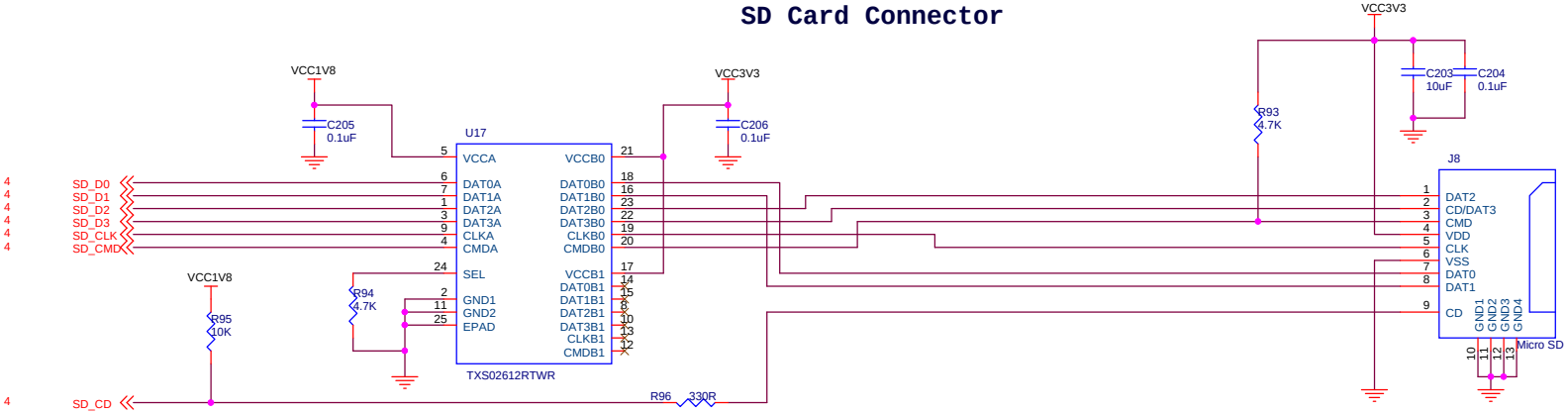
ALINX

Title	Zynq-7000 LED & KEY	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 12 of 16	

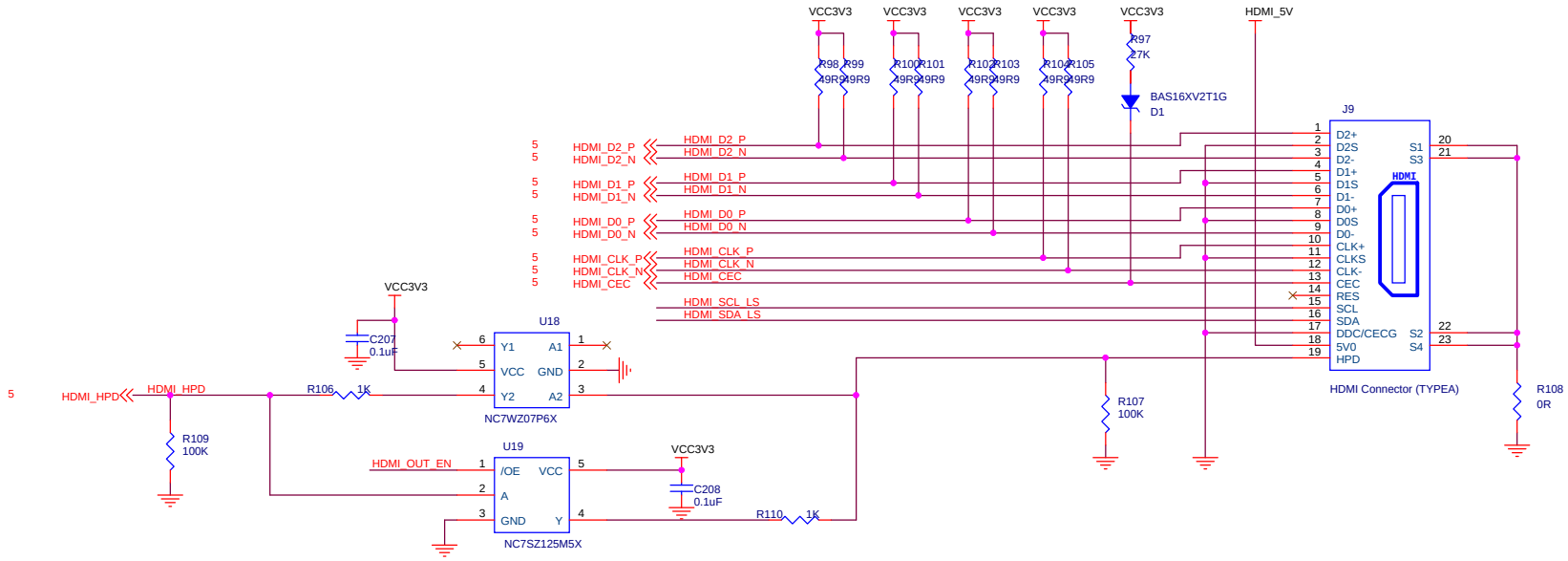
USB Uart



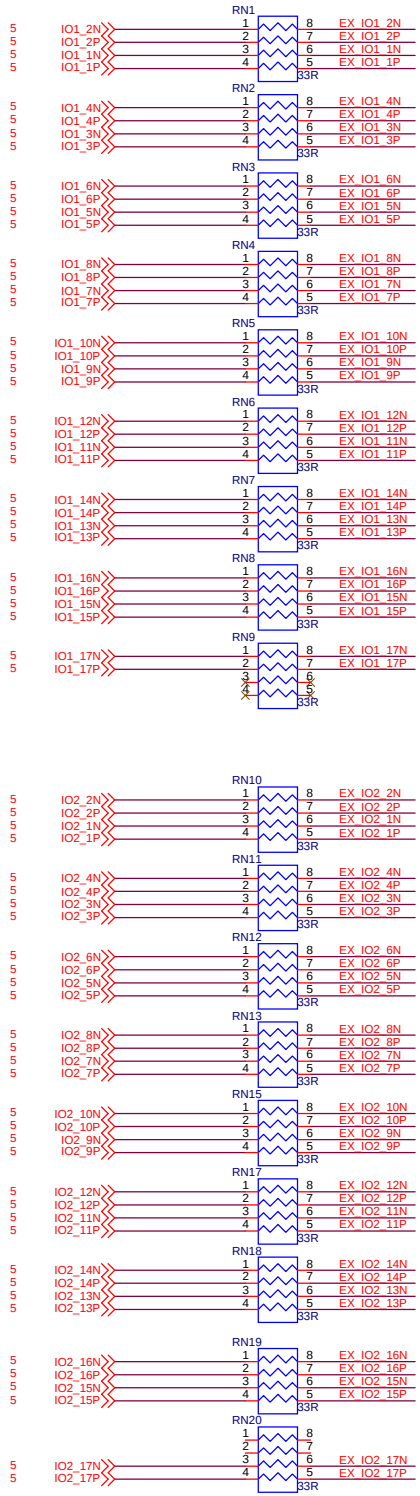
SD Card Connector



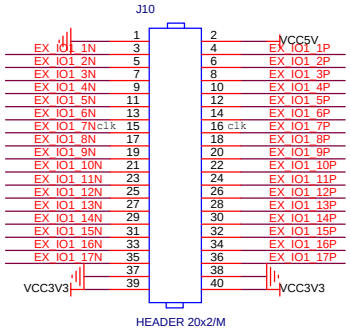
Title	Zynq-7000 UART & SD		
Size	Document Number AX7010/AX7020开发板原理图		Rev 1.0
Date: Monday, October 08, 2018	Sheet 13 of 16		

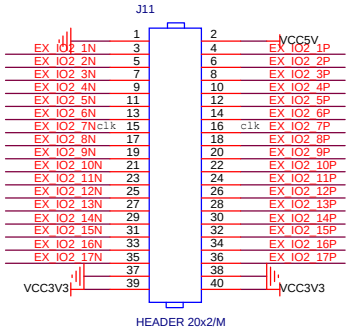


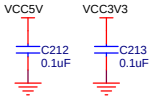
Title	Zynq-7000 HDMI	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 14 of 16	

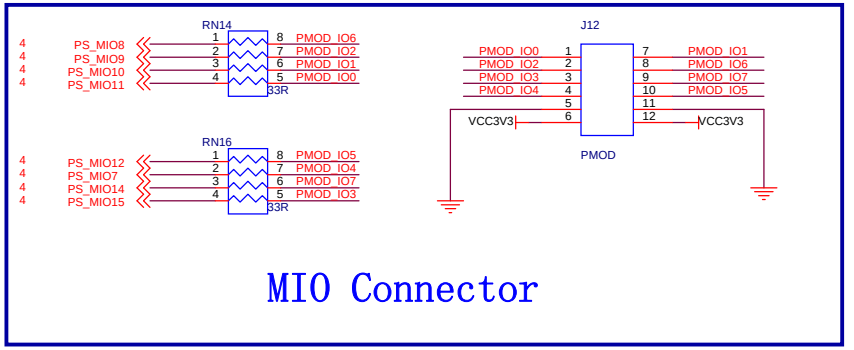


FPGA 40 PIN External IO





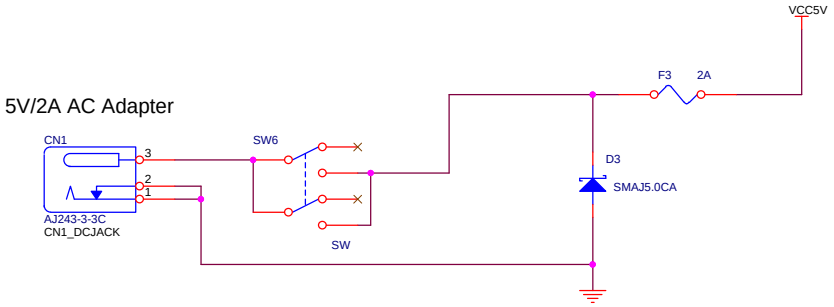


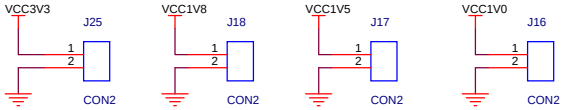


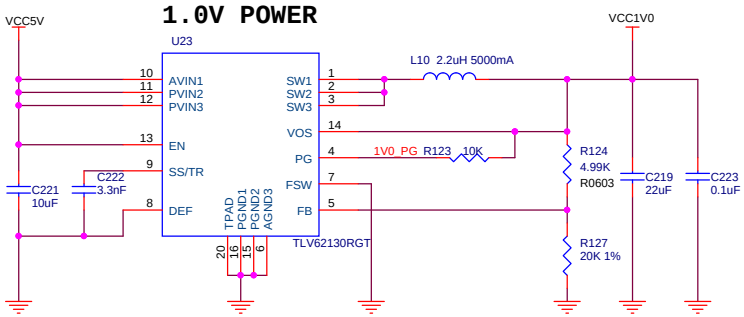
MIO Connector

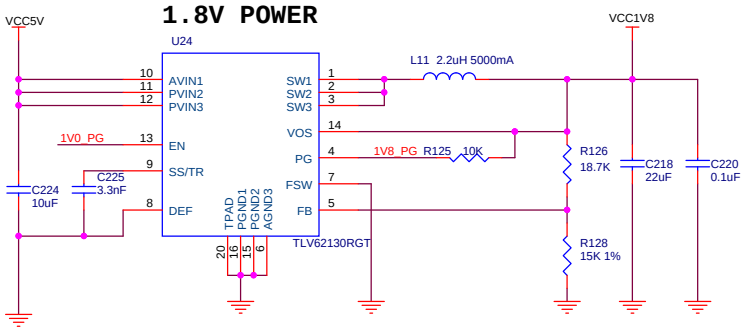
ALINX

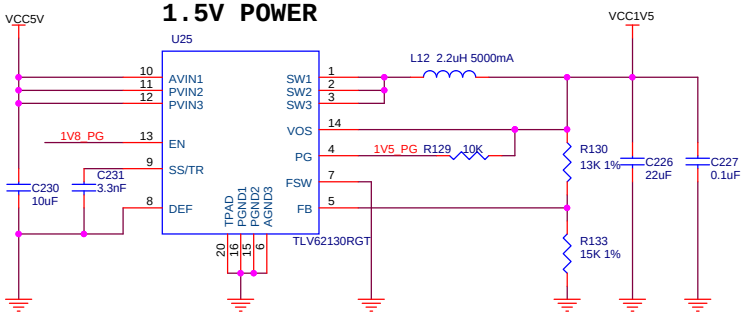
Title	Zynq-7000 LED & KEY & IO	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 15 of 16	

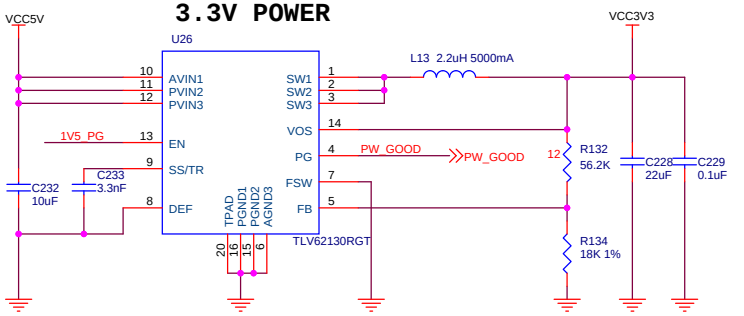






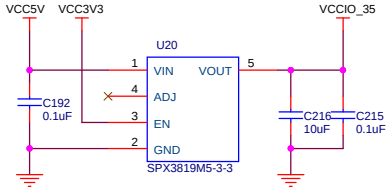






Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO



ALINX

Title	Power	
Size	Document Number: AX7010/AX7020开发板原理图	Rev: 1.0
Date: Monday, October 08, 2018	Sheet 16 of 16	