

## CSG324 Package—LX9, LX16, LX25, and LX45

The BUFIO2 clocking region column lists the BUFIO2 clock sources that connect to the I/O clock input for the associated pin. For more information see [Clock Inputs and BUFIO2 Clocking Regions in Chapter 1](#).

BUFIO2 Region	Description
TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).
LT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 3 (left).
LB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 3 (left).

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45

Bank	Pin Description	Pin Number	BUFIO2 Region	No Connect (NC)
0	IO_L1P_HSWAPEN_0	D4	TL	
0	IO_L1N_VREF_0	C4	TL	
0	IO_L2P_0	B2	TL	
0	IO_L2N_0	A2	TL	
0	IO_L3P_0	D6	TL	
0	IO_L3N_0	C6	TL	
0	IO_L4P_0	B3	TL	
0	IO_L4N_0	A3	TL	
0	IO_L5P_0	B4	TL	
0	IO_L5N_0	A4	TL	
0	IO_L6P_0	C5	TL	
0	IO_L6N_0	A5	TL	
0	IO_L7P_0	F7	TL	LX9, LX25, LX45
0	IO_L7N_0	E6	TL	LX9, LX25, LX45
0	IO_L8P_0	B6	TL	
0	IO_L8N_VREF_0	A6	TL	
0	IO_L9P_0	E7	TL	LX9, LX25, LX45
0	IO_L9N_0	E8	TL	LX9, LX25, LX45
0	IO_L10P_0	C7	TL	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
0	IO_L10N_0	A7	TL	
0	IO_L11P_0	D8	TL	
0	IO_L11N_0	C8	TL	
0	IO_L32P_0	G8	TL	LX9, LX25, LX45
0	IO_L32N_0	F8	TL	LX9, LX25, LX45
0	IO_L33P_0	B8	TL	
0	IO_L33N_0	A8	TL	
0	IO_L34P_GCLK19_0	D9	TL	
0	IO_L34N_GCLK18_0	C9	TL	
0	IO_L35P_GCLK17_0	B9	TL	
0	IO_L35N_GCLK16_0	A9	TL	
0	IO_L36P_GCLK15_0	D11	TR	
0	IO_L36N_GCLK14_0	C11	TR	
0	IO_L37P_GCLK13_0	C10	TR	
0	IO_L37N_GCLK12_0	A10	TR	
0	IO_L38P_0	G9	TR	
0	IO_L38N_VREF_0	F9	TR	
0	IO_L39P_0	B11	TR	
0	IO_L39N_0	A11	TR	
0	IO_L40P_0	G11	TR	LX9, LX45
0	IO_L40N_0	F10	TR	LX9, LX45
0	IO_L41P_0	B12	TR	
0	IO_L41N_0	A12	TR	
0	IO_L42P_0	F11	TR	LX9, LX45
0	IO_L42N_0	E11	TR	LX9, LX45
0	IO_L47P_0	D12	TR	LX9, LX45
0	IO_L47N_0	C12	TR	LX9, LX45
0	IO_L50P_0	C13	TR	LX9
0	IO_L50N_0	A13	TR	LX9
0	IO_L51P_0	F12	TR	LX9, LX45
0	IO_L51N_0	E12	TR	LX9, LX45
0	IO_L62P_0	B14	TR	
0	IO_L62N_VREF_0	A14	TR	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
0	IO_L63P_SCP7_0	F13	TR	
0	IO_L63N_SCP6_0	E13	TR	
0	IO_L64P_SCP5_0	C15	TR	
0	IO_L64N_SCP4_0	A15	TR	
0	IO_L65P_SCP3_0	D14	TR	
0	IO_L65N_SCP2_0	C14	TR	
0	IO_L66P_SCP1_0	B16	TR	
0	IO_L66N_SCP0_0	A16	TR	
NA	TCK	A17	NA	
NA	TDI	D15	NA	
NA	TMS	B18	NA	
NA	TDO	D16	NA	
1	IO_L1P_A25_1	F15	RT	
1	IO_L1N_A24_VREF_1	F16	RT	
1	IO_L29P_A23_M1A13_1	C17	RT	
1	IO_L29N_A22_M1A14_1	C18	RT	
1	IO_L30P_A21_M1RESET_1	F14	RT	
1	IO_L30N_A20_M1A11_1	G14	RT	
1	IO_L31P_A19_M1CKE_1	D17	RT	
1	IO_L31N_A18_M1A12_1	D18	RT	
1	IO_L32P_A17_M1A8_1	H12	RT	
1	IO_L32N_A16_M1A9_1	G13	RT	
1	IO_L33P_A15_M1A10_1	E16	RT	
1	IO_L33N_A14_M1A4_1	E18	RT	
1	IO_L34P_A13_M1WE_1	K12	RT	
1	IO_L34N_A12_M1BA2_1	K13	RT	
1	IO_L35P_A11_M1A7_1	F17	RT	
1	IO_L35N_A10_M1A2_1	F18	RT	
1	IO_L36P_A9_M1BA0_1	H13	RT	
1	IO_L36N_A8_M1BA1_1	H14	RT	
1	IO_L37P_A7_M1A0_1	H15	RT	
1	IO_L37N_A6_M1A1_1	H16	RT	
1	IO_L38P_A5_M1CLK_1	G16	RT	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
1	IO_L38N_A4_M1CLKN_1	G18	RT	
1	IO_L39P_M1A3_1	J13	RT (RB in LX25)	
1	IO_L39N_M1ODT_1	K14	RT (RB in LX25)	
1	IO_L40P_GCLK11_M1A5_1	L12	RT (RB in LX25)	
1	IO_L40N_GCLK10_M1A6_1	L13	RT (RB in LX25)	
1	IO_L41P_GCLK9_IRDY1_M1RASN_1	K15	RT (RB in LX25)	
1	IO_L41N_GCLK8_M1CASN_1	K16	RT (RB in LX25)	
1	IO_L42P_GCLK7_M1UDM_1	L15	RB	
1	IO_L42N_GCLK6_TRDY1_M1LDM_1	L16	RB	
1	IO_L43P_GCLK5_M1DQ4_1	H17	RB	
1	IO_L43N_GCLK4_M1DQ5_1	H18	RB	
1	IO_L44P_A3_M1DQ6_1	J16	RB	
1	IO_L44N_A2_M1DQ7_1	J18	RB	
1	IO_L45P_A1_M1LDQS_1	K17	RB	
1	IO_L45N_A0_M1LDQSN_1	K18	RB	
1	IO_L46P_FCS_B_M1DQ2_1	L17	RB	
1	IO_L46N_FOE_B_M1DQ3_1	L18	RB	
1	IO_L47P_FWE_B_M1DQ0_1	M16	RB	
1	IO_L47N_LDC_M1DQ1_1	M18	RB	
1	IO_L48P_HDC_M1DQ8_1	N17	RB	
1	IO_L48N_M1DQ9_1	N18	RB	
1	IO_L49P_M1DQ10_1	P17	RB	
1	IO_L49N_M1DQ11_1	P18	RB	
1	IO_L50P_M1UDQS_1	N15	RB	
1	IO_L50N_M1UDQSN_1	N16	RB	
1	IO_L51P_M1DQ12_1	T17	RB	
1	IO_L51N_M1DQ13_1	T18	RB	
1	IO_L52P_M1DQ14_1	U17	RB	
1	IO_L52N_M1DQ15_1	U18	RB	
1	IO_L53P_1	M14	RB	
1	IO_L53N_VREF_1	N14	RB	
1	IO_L61P_1	L14	RB	
1	IO_L61N_1	M13	RB	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
1	IO_L74P_AWAKE_1	P15	RB	
1	IO_L74N_DOUT_BUSY_1	P16	RB	
NA	SUSPEND	R16	NA	
2	CMPCS_B_2	P13	NA	
2	DONE_2	V17	NA	
2	IO_L1P_CCLK_2	R15	BR	
2	IO_L1N_M0_CMPMISO_2	T15	BR	
2	IO_L2P_CMPCLK_2	U16	BR	
2	IO_L2N_CMPMOSI_2	V16	BR	
2	IO_L3P_D0_DIN_MISO_MISO1_2	R13	BR	
2	IO_L3N_MOSI_CSI_B_MISO0_2	T13	BR	
2	IO_L5P_2	U15	BR	LX9
2	IO_L5N_2	V15	BR	LX9
2	IO_L12P_D1_MISO2_2	T14	BR	
2	IO_L12N_D2_MISO3_2	V14	BR	
2	IO_L13P_M1_2	N12	BR	
2	IO_L13N_D10_2	P12	BR	
2	IO_L14P_D11_2	U13	BR	
2	IO_L14N_D12_2	V13	BR	
2	IO_L15P_2	M11	BR	LX9
2	IO_L15N_2	N11	BR	LX9
2	IO_L16P_2	R11	BR	
2	IO_L16N_VREF_2	T11	BR	
2	IO_L19P_2	T12	BR	LX9
2	IO_L19N_2	V12	BR	LX9
2	IO_L20P_2	N10	BR	LX9
2	IO_L20N_2	P11	BR	LX9
2	IO_L22P_2	M10	BR	LX9
2	IO_L22N_2	N9	BR	LX9
2	IO_L23P_2	U11	BR	
2	IO_L23N_2	V11	BR	
2	IO_L29P_GCLK3_2	R10	BR	
2	IO_L29N_GCLK2_2	T10	BR	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
2	IO_L30P_GCLK1_D13_2	U10	BR	
2	IO_L30N_GCLK0_USERCCLK_2	V10	BR	
2	IO_L31P_GCLK31_D14_2	R8	BL	
2	IO_L31N_GCLK30_D15_2	T8	BL	
2	IO_L32P_GCLK29_2	T9	BL	
2	IO_L32N_GCLK28_2	V9	BL	
2	IO_L40P_2	M8	BL	LX9
2	IO_L40N_2	N8	BL	LX9
2	IO_L41P_2	U8	BL	
2	IO_L41N_VREF_2	V8	BL	
2	IO_L43P_2	U7	BL	
2	IO_L43N_2	V7	BL	
2	IO_L44P_2	N7	BL	LX9
2	IO_L44N_2	P8	BL	LX9
2	IO_L45P_2	T6	BL	
2	IO_L45N_2	V6	BL	
2	IO_L46P_2	R7	BL	
2	IO_L46N_2	T7	BL	
2	IO_L47P_2	N6	BL	LX9
2	IO_L47N_2	P7	BL	LX9
2	IO_L48P_D7_2	R5	BL	
2	IO_L48N_RDWR_B_VREF_2	T5	BL	
2	IO_L49P_D3_2	U5	BL	
2	IO_L49N_D4_2	V5	BL	
2	IO_L62P_D5_2	R3	BL	
2	IO_L62N_D6_2	T3	BL	
2	IO_L63P_2	T4	BL	
2	IO_L63N_2	V4	BL	
2	IO_L64P_D8_2	N5	BL	
2	IO_L64N_D9_2	P6	BL	
2	IO_L65P_INIT_B_2	U3	BL	
2	IO_L65N_CSO_B_2	V3	BL	
2	PROGRAM_B_2	V2	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
3	IO_L1P_3	N4	LB	
3	IO_L1N_VREF_3	N3	LB	
3	IO_L2P_3	P4	LB	
3	IO_L2N_3	P3	LB	
3	IO_L31P_3	L6	LB	
3	IO_L31N_VREF_3	M5	LB	
3	IO_L32P_M3DQ14_3	U2	LB	
3	IO_L32N_M3DQ15_3	U1	LB	
3	IO_L33P_M3DQ12_3	T2	LB	
3	IO_L33N_M3DQ13_3	T1	LB	
3	IO_L34P_M3UDQS_3	P2	LB	
3	IO_L34N_M3UDQSN_3	P1	LB	
3	IO_L35P_M3DQ10_3	N2	LB	
3	IO_L35N_M3DQ11_3	N1	LB	
3	IO_L36P_M3DQ8_3	M3	LB	
3	IO_L36N_M3DQ9_3	M1	LB	
3	IO_L37P_M3DQ0_3	L2	LB	
3	IO_L37N_M3DQ1_3	L1	LB	
3	IO_L38P_M3DQ2_3	K2	LB	
3	IO_L38N_M3DQ3_3	K1	LB	
3	IO_L39P_M3LDQS_3	L4	LB	
3	IO_L39N_M3LDQSN_3	L3	LB	
3	IO_L40P_M3DQ6_3	J3	LB	
3	IO_L40N_M3DQ7_3	J1	LB	
3	IO_L41P_GCLK27_M3DQ4_3	H2	LB	
3	IO_L41N_GCLK26_M3DQ5_3	H1	LB	
3	IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	LB	
3	IO_L42N_GCLK24_M3LDM_3	K3	LB	
3	IO_L43P_GCLK23_M3RASN_3	L5	LT (LB in LX25)	
3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	LT (LB in LX25)	
3	IO_L44P_GCLK21_M3A5_3	H4	LT (LB in LX25)	
3	IO_L44N_GCLK20_M3A6_3	H3	LT (LB in LX25)	
3	IO_L45P_M3A3_3	L7	LT (LB in LX25)	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
3	IO_L45N_M3ODT_3	K6	LT (LB in LX25)	
3	IO_L46P_M3CLK_3	G3	LT	
3	IO_L46N_M3CLKN_3	G1	LT	
3	IO_L47P_M3A0_3	J7	LT	
3	IO_L47N_M3A1_3	J6	LT	
3	IO_L48P_M3BA0_3	F2	LT	
3	IO_L48N_M3BA1_3	F1	LT	
3	IO_L49P_M3A7_3	H6	LT	
3	IO_L49N_M3A2_3	H5	LT	
3	IO_L50P_M3WE_3	E3	LT	
3	IO_L50N_M3BA2_3	E1	LT	
3	IO_L51P_M3A10_3	F4	LT	
3	IO_L51N_M3A4_3	F3	LT	
3	IO_L52P_M3A8_3	D2	LT	
3	IO_L52N_M3A9_3	D1	LT	
3	IO_L53P_M3CKE_3	H7	LT	
3	IO_L53N_M3A12_3	G6	LT	
3	IO_L54P_M3RESET_3	E4	LT	
3	IO_L54N_M3A11_3	D3	LT	
3	IO_L55P_M3A13_3	F6	LT	
3	IO_L55N_M3A14_3	F5	LT	
3	IO_L83P_3	C2	LT	
3	IO_L83N_VREF_3	C1	LT	
NA	GND	A1	NA	
NA	GND	A18	NA	
NA	GND	B13	NA	
NA	GND	B7	NA	
NA	GND	C16	NA	
NA	GND	C3	NA	
NA	GND	D10	NA	
NA	GND	D5	NA	
NA	GND	E15	NA	
NA	GND	G12	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
NA	GND	G17	NA	
NA	GND	G2	NA	
NA	GND	G5	NA	
NA	GND	H10	NA	
NA	GND	H8	NA	
NA	GND	J11	NA	
NA	GND	J15	NA	
NA	GND	J4	NA	
NA	GND	J9	NA	
NA	GND	K10	NA	
NA	GND	K8	NA	
NA	GND	L11	NA	
NA	GND	L9	NA	
NA	GND	M17	NA	
NA	GND	M2	NA	
NA	GND	M6	NA	
NA	GND	N13	NA	
NA	GND	R1	NA	
NA	GND	R14	NA	
NA	GND	R18	NA	
NA	GND	R4	NA	
NA	GND	R9	NA	
NA	GND	T16	NA	
NA	GND	U12	NA	
NA	GND	U6	NA	
NA	GND	V1	NA	
NA	GND	V18	NA	
NA	VCCAUX	B1	NA	
NA	VCCAUX	B17	NA	
NA	VCCAUX	E14	NA	
NA	VCCAUX	E5	NA	
NA	VCCAUX	E9	NA	
NA	VCCAUX	G10	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
NA	VCCAUX	J12	NA	
NA	VCCAUX	K7	NA	
NA	VCCAUX	M9	NA	
NA	VCCAUX	P10	NA	
NA	VCCAUX	P14	NA	
NA	VCCAUX	P5	NA	
NA	VCCINT	G7	NA	
NA	VCCINT	H11	NA	
NA	VCCINT	H9	NA	
NA	VCCINT	J10	NA	
NA	VCCINT	J8	NA	
NA	VCCINT	K11	NA	
NA	VCCINT	K9	NA	
NA	VCCINT	L10	NA	
NA	VCCINT	L8	NA	
NA	VCCINT	M12	NA	
NA	VCCINT	M7	NA	
0	VCCO_0	B10	NA	
0	VCCO_0	B15	NA	
0	VCCO_0	B5	NA	
0	VCCO_0	D13	NA	
0	VCCO_0	D7	NA	
0	VCCO_0	E10	NA	
1	VCCO_1	E17	NA	
1	VCCO_1	G15	NA	
1	VCCO_1	J14	NA	
1	VCCO_1	J17	NA	
1	VCCO_1	M15	NA	
1	VCCO_1	R17	NA	
2	VCCO_2	P9	NA	
2	VCCO_2	R12	NA	
2	VCCO_2	R6	NA	
2	VCCO_2	U14	NA	

Table 2-7: CSG324 Package—LX9, LX16, LX25, and LX45 (Cont'd)

Bank	Pin Description	Pin Number	BUFI02 Region	No Connect (NC)
2	VCCO_2	U4	NA	
2	VCCO_2	U9	NA	
3	VCCO_3	E2	NA	
3	VCCO_3	G4	NA	
3	VCCO_3	J2	NA	
3	VCCO_3	J5	NA	
3	VCCO_3	M4	NA	
3	VCCO_3	R2	NA	