



## SiI9013 HDMI Receiver

### Data Sheet

Document # SiI-DS-0232-D01

This document was watermarked on 27-04-2011 at 16:37:42 local time.

June 2010

### Copyright Notice

Copyright © 2008-2010 Silicon Image, Inc. All rights reserved. These materials contain proprietary and confidential information (including trade secrets, copyright and other interests) of Silicon Image, Inc. You may not use these materials except only for your bona fide non-commercial evaluation of your potential purchase of products and/or services from Silicon Image or its affiliates, and/or only in connection with your purchase of products and/or services from Silicon Image or its affiliates, and only in accordance with the terms and conditions herein. You have no right to copy, modify, transfer, sublicense, publicly display, create derivative works of or distribute these materials, or otherwise make these materials available, in whole or in part, to any third party.

### Patents

The subject matter described herein contains one or more inventions claimed in patents and/or patents pending owned by Silicon Image, Inc., including but not limited to the inventions claimed in US patents #6,914,637, #6,151,334, #6,026,124, #5,974,464 and #5,825,824.

### Trademark Acknowledgment

Silicon Image™, VastLane™, SteelVine™, PinnaClear™, Simplay™, Simplay HD™, Satalink™, and TMDST™ are trademarks or registered trademarks of Silicon Image, Inc. in the United States and other countries. HDMI®, the HDMI logo and High-Definition Multimedia Interface™ are trademarks or registered trademarks of, and are used under license from, HDMI Licensing, LLC.

### Export Controlled Document

This document contains information subject to the Export Administration Regulations (EAR) and has a classification of EAR99 or is controlled for Anti-Terrorism (AT) purposes. Transfer of this information by any means to an EAR Country Group E:1 or foreign national thereof (whether in the U.S. or abroad) may require an export license or other approval from the U.S. Department of Commerce. For more information, contact the Silicon Image Director of Global Trade Compliance.

### Further Information

To request other materials, documentation, and information, contact your local Silicon Image, Inc. sales office or visit the Silicon Image, Inc. web site at [www.siliconimage.com](http://www.siliconimage.com).

### Revision History

Revision	Date	Comment
A	12/2006	First Production release
B	12/2006	Updated packaging information
C	8/2007	Updated template and packaging information
D	7/2008	Updated S/PDIF Frequency support and MCLK properties
D01	6/2010	Updated page 1 and layout to prepare Data Brief; minor editing throughout.

© 2008-2010 Silicon Image, Inc. All rights reserved.

## Table of Contents

General Description.....	1
Digital Video Interface .....	1
Digital Audio Interface.....	1
HDCP .....	1
Package.....	1
Comparison of the SiI9013 with SiI9993 and SiI9025 receivers.....	2
Pin Diagram.....	3
System Applications.....	4
Functional Description .....	4
TMDS Digital Core .....	4
Active Port Detection .....	4
HDCP Decryption Engine/XOR Mask.....	4
HDCP Keys .....	5
HDCP BIST.....	6
Data Input and Conversion .....	6
Mode Control Logic .....	6
Video Data Conversion and Video Output.....	6
Automatic Video Configuration .....	8
Audio Processing Logic.....	9
Auto Audio Configuration.....	9
Soft Mute.....	9
I <sup>2</sup> S Channel Mapping.....	9
Control and Configuration.....	10
Registers/Configuration Logic.....	10
I <sup>2</sup> C Ports.....	10
Electrical Specifications .....	11
Absolute Maximum Conditions.....	11
Normal Operating Conditions.....	12
DC Specifications.....	13
Digital I/O Specifications.....	13
DC Power Supply Specifications.....	14
AC Specifications.....	15
Video AC Timing Specifications.....	15
Interrupt Timings.....	17
Audio AC Timing Specifications .....	18
Timing Diagrams.....	20
TMDS Input Timing Diagrams .....	20
Power Supply Control Timings .....	20
Power Supply Sequencing .....	20
Configuring Standby Power Mode.....	20
Digital Video Output Timing Diagrams .....	21
Calculating Setup and Hold Times .....	22
24-Bit SDR Mode.....	22
12-Bit DDR Mode .....	22
Audio Output Timings.....	23
Control Timings.....	24
Reset Timings.....	24
Pin Descriptions.....	25
Digital Video Output Pins .....	25
Digital Audio Output Pins .....	26
Configuration/Programming Pins .....	26
Differential Signal Data Pins .....	27
Power and Ground Pins .....	27

Video Path .....	28
HDMI Input Modes to SiI9013 HDMI Receiver Output Modes .....	28
HDMI RGB 4:4:4 Input Processing .....	29
HDMI YCbCr 4:4:4 Input Processing .....	30
HDMI YCbCr 4:2:2 Input Processing .....	31
SiI9013 HDMI Receiver Output Mode Configuration .....	32
RGB and YCbCr 4:4:4 Formats with Separate Syncs .....	33
YC 4:2:2 Formats with Separate Syncs .....	34
YC 4:2:2 Formats with Embedded Syncs .....	35
YC Mux (4:2:2) Formats with Separate Syncs .....	36
YC Mux 4:2:2 Formats with Embedded Syncs .....	37
48-Bit Output Mode .....	38
12-Bit DDR RGB 4:4:4 and YCbCr 4:4:4 Formats with Separate Syncs .....	39
I <sup>2</sup> C Interfaces .....	40
HDCP E-DDC / I <sup>2</sup> C Interface .....	40
Local I <sup>2</sup> C Interface .....	41
Video Requirement for I <sup>2</sup> C Access .....	41
HDCP Registers .....	41
Design Recommendations .....	42
Power Control .....	42
Power Pin Current Demands .....	42
Crystal Clock Source Requirement .....	42
Receiver DDC Bus Protection .....	42
PWR5V Input .....	43
Voltage Ripple Regulation .....	43
Decoupling Capacitors .....	43
Receiver Layout .....	43
ESD Protection .....	44
EMI Considerations .....	44
Thermal and Electrical Benefits of Exposed Pads .....	45
Typical Circuits .....	45
Power Supply Decoupling .....	45
HDMI Port TMDS Connections .....	46
Digital Video Output Connections .....	46
Digital Audio Output Connections .....	47
Control Signal Connections .....	48
Layout .....	48
TMDS Input Port Connections .....	49
Routing with ESD Devices .....	49
Packaging .....	50
Package Dimensions .....	50
Marking Specification .....	51
Ordering Information .....	51
References .....	52
Standards Documents .....	52
Silicon Image Documents .....	52

## List of Figures

Figure 1. DTV Block Diagram .....	1
Figure 2. Pin Diagram .....	3
Figure 3. DTV Block Diagram .....	4
Figure 4. Functional Block Diagram .....	5
Figure 5. Default Video Processing Path .....	6
Figure 6. I <sup>2</sup> C Register Domains .....	10
Figure 7. Test Point VCCTP for VCC Noise Tolerance Spec .....	12
Figure 8. SCDT and CKDT Timing from DE or RXC Inactive/Active .....	17
Figure 9. Audio Crystal Schematic .....	18
Figure 10. TMDS Channel-to-Channel Skew Timing .....	20
Figure 11. Power Supply Sequencing .....	20
Figure 12. Configuring Standby Power Mode .....	20
Figure 13. Video Digital Output Transition Times .....	21
Figure 14. Receiver Clock-to-Output Delay and Duty Cycle Limits .....	21
Figure 15. 24-Bit SDR Mode Receiver Output Setup and Hold Times .....	22
Figure 16. 12-Bit DDR Mode Receiver Output Setup and Hold Times .....	23
Figure 17. I <sup>2</sup> S Output Timings .....	23
Figure 18. S/PDIF Output Timings .....	23
Figure 19. MCLK Timings .....	24
Figure 20. RESET# Minimum Timings .....	24
Figure 21. Receiver Video and Audio Data Processing Paths .....	28
Figure 22. HDMI RGB 4:4:4 Input to Video Output Transformations .....	29
Figure 23. HDMI YCbCr 4:4:4 Input to Video Output Transformations .....	30
Figure 24. HDMI YCbCr 4:2:2 Input to Video Output Transformations .....	31
Figure 25. 4:4:4 Timing Diagram .....	33
Figure 26. YC Timing Diagram .....	34
Figure 27. YC 4:2:2 Embedded Sync Timing Diagram .....	35
Figure 28. YC Mux 4:2:2 Timing Diagram .....	36
Figure 29. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram .....	37
Figure 30. 48-Bit 4:4:4 Timing Diagram .....	38
Figure 31. 12-Bit DDR Output 4:4:4 Timing Diagram .....	39
Figure 32. I <sup>2</sup> C Byte Read .....	40
Figure 33. I <sup>2</sup> C Byte Write .....	40
Figure 34. Short Read Sequence .....	40
Figure 35. Decoupling and Bypass Capacitor Placement .....	43
Figure 36. HDMI to Receiver Routing – Top View .....	44
Figure 37. Power Supply Decoupling and PLL Filtering Schematic .....	45
Figure 38. HDMI Port Connections Schematic .....	46
Figure 39. Digital Display Schematic .....	47
Figure 40. Audio Output Schematic .....	47
Figure 41. XTALIN Connection with External Clock Source .....	48
Figure 42. Controller Connections Schematic .....	48
Figure 43. TMDS Input Signal Assignments .....	49
Figure 44. TMDS Input Layout through ESD Devices .....	49
Figure 45. Package Diagram .....	50
Figure 46. Marking Diagram .....	51

## List of Tables

Table 1. Comparison of 9993/9025/9013 Features .....	2
Table 2. Digital Video Output Formats .....	6
Table 3. Default Video Processing .....	7
Table 4. Color Space versus Video Format .....	7
Table 5. YCbCr-to-RGB Color Space Conversion Formulas .....	8
Table 6. OutMode Programming .....	8
Table 7. AVI InfoFrame Video Path Details .....	9
Table 8. Supported MCLK Frequencies in MHz .....	9
Table 9. Control of Local I <sup>2</sup> C Address with CI2CA Pin .....	10
Table 10. Absolute Maximum Conditions <sup>1</sup> .....	11
Table 11. Normal Operating Conditions .....	12
Table 12. Digital I/O Specifications .....	13
Table 13. Total Power versus Power-Down Modes .....	14
Table 14. Power Down Mode Definitions .....	15
Table 15. Output Rise and Fall Times (All Output Modes) .....	15
Table 16. 12-Bit DDR Output Timings .....	15
Table 17. 8/10/12/16/20/24-Bit SDR Output Timings .....	15
Table 18. 48-Bit SDR Output Timings .....	16
Table 19. TMDS Input Timings .....	16
Table 20. Interrupt Output Pin Timings .....	17
Table 21. I <sup>2</sup> S Output Port Timings .....	18
Table 22. S/PDIF Output Port Timings .....	18
Table 23. Audio Crystal Timings .....	18
Table 24. Miscellaneous Timings .....	19
Table 25. Calculation of 24-Bit SDR Output Setup and Hold Times .....	22
Table 26. Calculation of 12-Bit DDR Output Setup and Hold Times .....	22
Table 27. Translating HDMI Formats to Output Formats .....	28
Table 28. Output Video Formats .....	32
Table 29. 4:4:4 Mappings .....	33
Table 30. YC 4:2:2 non-Encoded-Sync Pin Mappings .....	34
Table 31. YC 4:2:2 Embedded Sync Pin Mappings .....	35
Table 32. YC Mux 4:2:2 Mappings .....	36
Table 33. YC Mux 4:2:2 Embedded Sync Pin Mapping .....	37
Table 34. 12-Bit DDR Output 4:4:4 Mappings .....	39
Table 35. Maximum Power Domain Currents versus Video Mode .....	42
Table 36. Referenced Documents .....	52
Table 37. Standards Groups Contact Information .....	52
Table 38. Silicon Image Publications .....	52

## General Description

The SiI9013 HDMI Receiver is a third generation HDMI<sup>®</sup> receiver that has been cost-optimized for direct view CRTs, plasma displays, LCD TVs and front projectors. Backward compatibility with DVI 1.0 allows HDMI systems to connect to existing DVI 1.0 hosts (DVD players, HD set top boxes, D-VHS players and receivers, PCs) over a single cable. The device is fully compatible at the register level with its related Silicon Image devices, including the SiI9993, SiI9033, and SiI9025 receivers.

The SiI9013 device can receive and output 2 to 8 channels of digital audio of up to 192 kHz. An industry-standard I<sup>2</sup>S port allows direct connection to low-cost audio DACs. An S/PDIF port supports up to 192 kHz audio. The device also offers automatic audio error detection.

The SiI9013 receiver comes pre-programmed with HDCP keys, and an HDCP repeater that can support as many as 12 downstream devices greatly simplifying the manufacturing process, lowering costs, and providing the highest level of HDCP key security.

Silicon Image HDMI receivers use the latest generation of integrated TMDST<sup>™</sup> core technology, supporting the entire range of DTV resolutions, from 480i/p to 1080i/p and PC resolutions up to 162 MHz from VGA to UXGA.

## Digital Video Interface

- 24-bit and 48-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- 12-bit DDR RGB/YCbCr 4:4:4 (clocked with rising and falling edges)
- Color Space Conversion for both RGB-to-YCbCr and YCbCr-to-RGB (601 or 709)
- Auto video mode detection simplifies system firmware design

## Digital Audio Interface

- Improved audio clock recovery enables designs capable of 100 dB THD + N/SNR
- Four programmable I<sup>2</sup>S outputs for connection to low-cost audio DACs
- Sample rates up to 192 kHz
- S/PDIF output supports both IEC 60958 and IEC 61937 for PCM, Dolby Digital, DTS digital or any S/PDIF type audio transmission (32–192 kHz Fs)

## HDCP

- Integrated HDCP decryption engine for receiving protected audio and video content
- HDCP Repeater support up to 12 downstream devices

## Package

- 128-pin, 14 mm by 14 mm, 0.4 mm pitch, LQFP package with an ePad

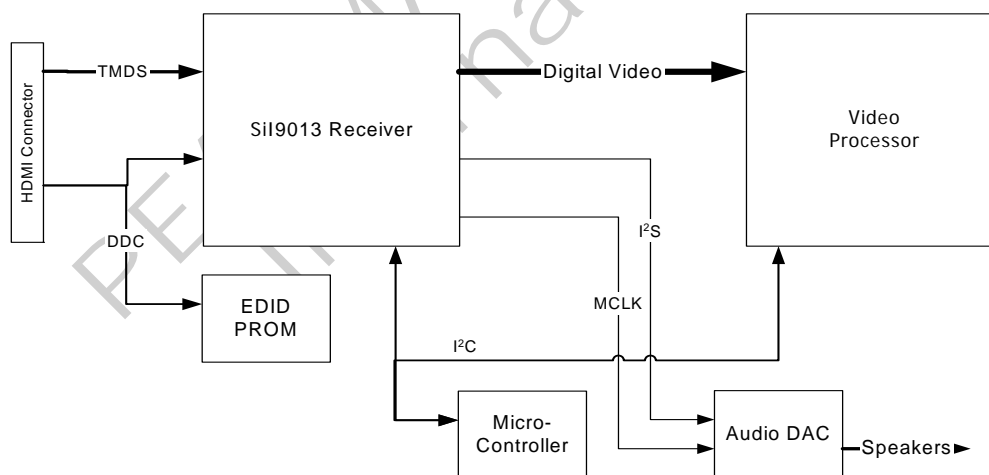


Figure 1. DTV Block Diagram

## Comparison of the SiI9013 with SiI9993 and SiI9025 receivers

Table 1 summarizes the differences between the SiI9993, SiI9025 and SiI9013 receivers.

Table 1. Comparison of 9993/9025/9013 Features

	SiI9993	SiI9025	SiI9013
<b>HDMI Input Connections</b>			
<b>TMDs Input Ports</b>	1	2	1
<b>DDC Input Ports</b>	1	2	1
<b>Output Ports</b>			
<b>Digital Video Output Ports</b>	1	1	1
<b>Maximum Output Bus Width</b>	24	24	48
<b>Analog Video Output Ports</b>	1	1	—
<b>S/PDIF Output Ports</b>	1	1	1
<b>I<sup>2</sup>S Output Ports</b>	2 channels	2 channels	8 channels
<b>Maximum Audio Sample Rate (Fs)</b>	48 kHz	192 kHz	192 kHz
<b>Maximum Pixel Clock Rate (RxCLK)</b>	81 MHz	150 MHz	162 MHz
<b>HDMI/HDCP Repeater Support</b>	No	No	Yes
<b>Local I<sup>2</sup>C Device Address</b>	0x60/0x68	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A
<b>Pin Count</b>	100	144	128
<b>Package</b>	TQFP	TQFP	LQFP

## Pin Diagram

Individual pin functions are described beginning on page 25.

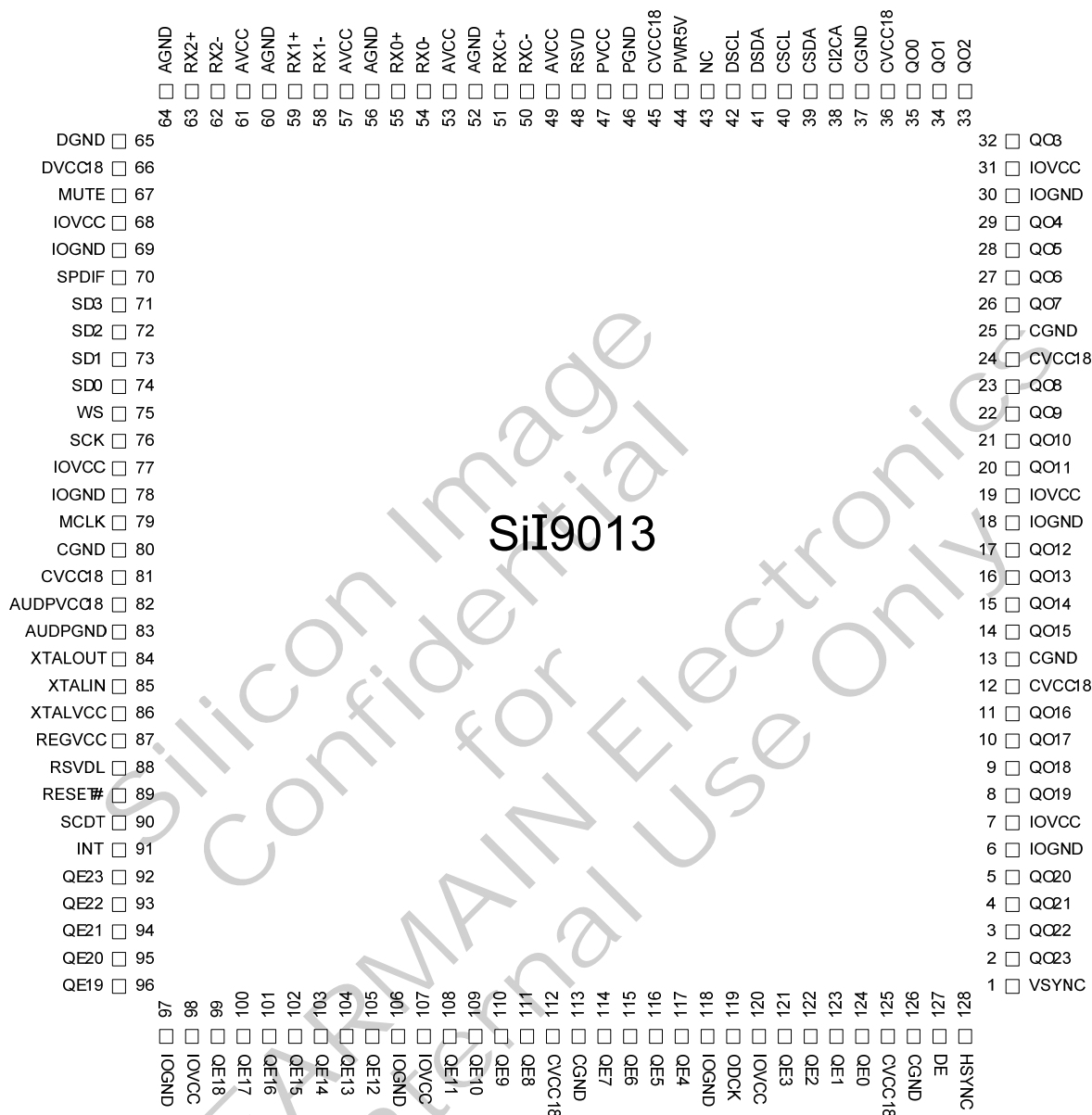


Figure 2. Pin Diagram

## System Applications

The SiI9013 HDMI Receiver provides one HDMI input port. The video output goes to a video processor while the audio output goes to an audio DAC.

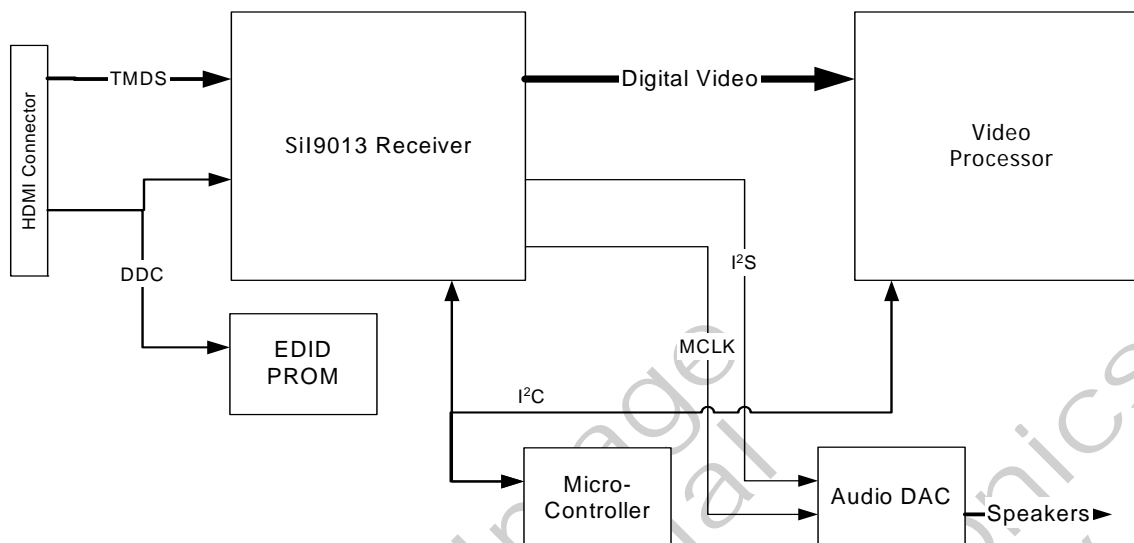


Figure 3. DTV Block Diagram

## Functional Description

The SiI9013 HDMI Receiver provides a complete solution for receiving HDMI compliant digital audio and video. Specialized audio and video processing is available within the SiI9013 HDMI Receiver to easily and cost effectively add HDMI capability to consumer electronics devices such as digital TVs, plasma displays, LCD TVs and projectors. Figure 4 on the next page shows the functional blocks of the chip.

### TMDS Digital Core

The TMDS digital core performs 10-to-8-bit TMDS decoding on the audio and video data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core supports link clock rates to 162 MHz, including CE modes to 720p/1080i/1080p and PC modes to XGA, SXGA and UXGA.

### Active Port Detection

The PanelLink core detects an active TMDS clock and detects an actively toggling DE signal. These states are accessible in register bits, useful for monitoring the status of the HDMI input or for automatically powering down the receiver.

The +5 V supply from the HDMI connector is used as a cable detect indicator. The SiI9013 HDMI Receiver can monitor the presence of this +5 V supply and provide a fast audio mute without pops when it senses the HDMI cable is disconnected. The microcontroller can also poll registers in the SiI9013 receiver to check whether an HDMI cable is connected.

### HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host microprocessor through a set sequence of register reads and writes through the DDC channel. Pre-programmed HDCP keys and Key Selection Vector (KSV) are used in the decryption

process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio and video data in sync with the host.

The SiI9013 HDMI Receiver also contains all the necessary logic to support HDCP repeater operation. The KSV values of downstream devices (up to 12 total) are written into the SiI9013 HDMI Receiver through the local I<sup>2</sup>C bus (CSDA/CSCL). As defined in the HDCP Specification,  $V_i'$  is calculated and made available to the host on the DDC bus (DSDA/DSCL).

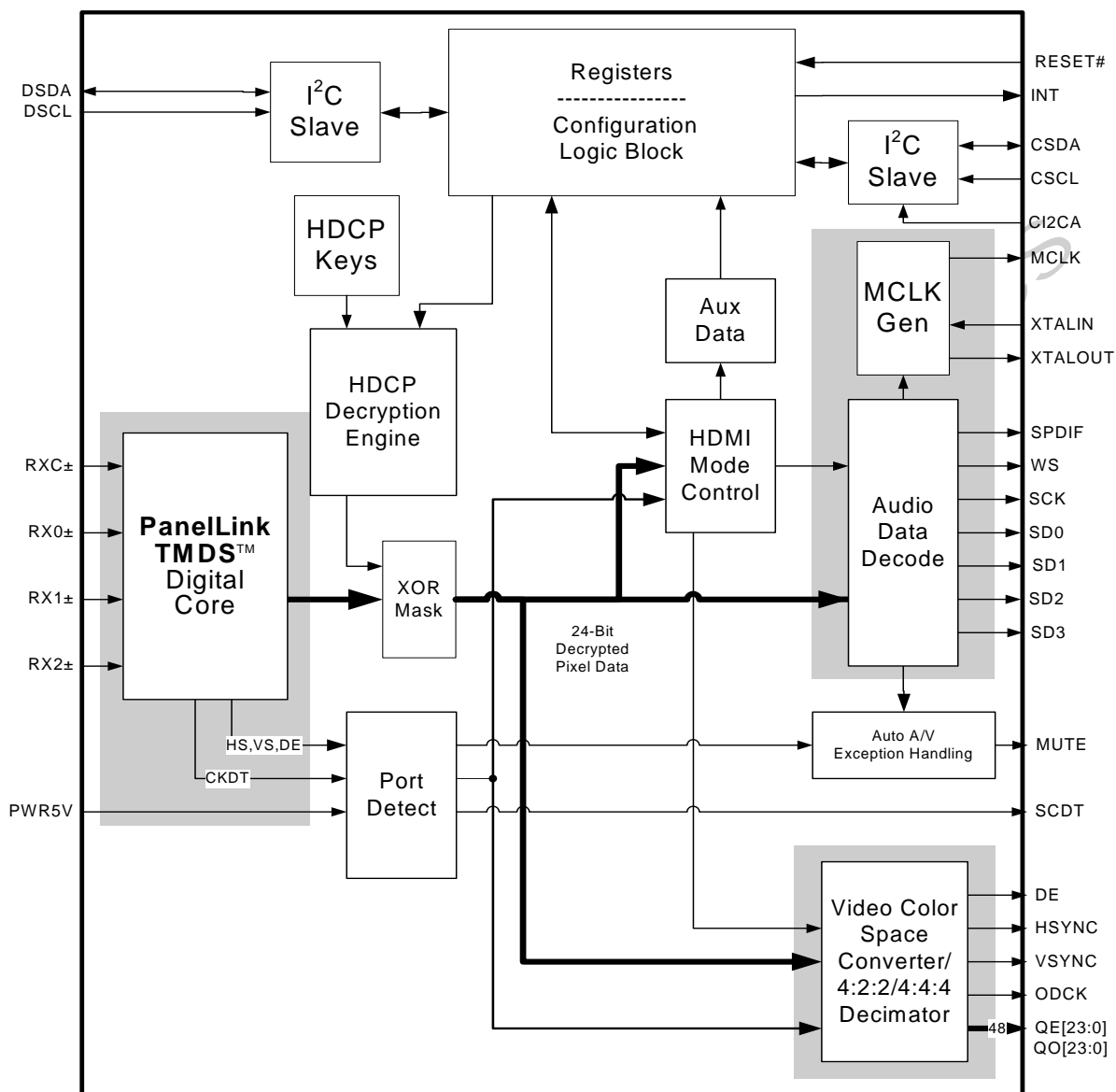


Figure 4. Functional Block Diagram

## HDCP Keys

The SiI9013 HDMI Receiver comes pre-programmed with a set of production HDCP keys. System manufacturers do not need to purchase key sets from the Digital-Content LLC. All purchasing, programming, and security for the HDCP keys is handled by Silicon Image. The pre-programmed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the SiI9013 HDMI Receiver, customers must have signed the HDCP license agreement (<http://www.digital-cp.com>) or a special NDA with Silicon Image.

## HDCP BIST

A built-in self test feature is available with the SiI9013 device to allow users a quick way to diagnose HDCP functionality. The BIST controls are available through the HDCP Key Command register (0x60:0xFA) and it includes self authentication tests along with a CRC test to confirm the proper function of the HDCP key storage. The results of the tests are read back from the HDCP Key Status register (0x60:0xF9). Refer to the SiI9013 HDMI Receiver Programmer's Reference (SiI-PR-1012) for more details.

## Data Input and Conversion

### Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information, and directs it to the appropriate logic block.

### Video Data Conversion and Video Output

The SiI9013 HDMI Receiver can output video in many different formats (see examples in Table 2). The receiver can also process the video data before it is output, as shown in Figure 5. Each of the processing blocks can be bypassed by setting the appropriate register bits. (See page 28 for a more detailed path diagram.)

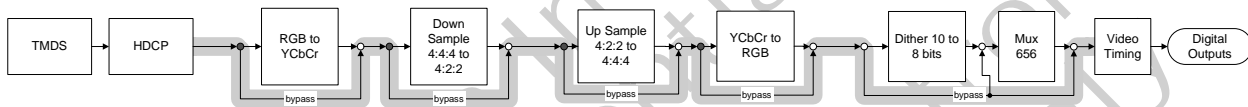


Figure 5. Default Video Processing Path

### Digital Video Output Formats

Table 2 lists the available video output formats.

Table 2. Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz) <sup>3</sup>							Notes
				480i	480p	XGA	720p	1080i	1080p	UXGA	
RGB	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	—
YCbCr	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	—
YCbCr	4:2:2	16/20/24	Sep, Emb.	13.25 / 27	27	—	74.25	74.25	148.5	162	1, 2
YCbCr	4:2:2	8/10/12	Sep, Emb.	27	54	135	148.5	148.5	—	—	1, 4
RGB	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
YCbCr	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
RGB	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:2:2	8/10/12	Sep, Emb.	13.25/27	27	65	74.25	74.25	—	81	1, 4

#### Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480p 54 MHz digital output can be achieved if the input differential clock is 54 MHz.
3. Output clock frequency depends on programming of internal registers. Differential TMDS input clock is always 25 MHz or faster.
4. Luma and chroma are multiplexed onto the same set of pins. Output clock is 2x the pixel rate. This mode is possible only when the link clock is also 2x the pixel rate, as shown in the table for 480i through 1080i.
5. 48-bit modes use half the output clock frequency of the 24-bit RGB/YCbCr 4:4:4 modes.
6. Output clock supports 12-bit mode by using both clock edges. These modes can run at a maximum of 81 MHz only.

Refer also to the list of output modes and configuration mappings on page 32.

## Color Range Scaling

The color range depends on the video format, according to the CEA-861B specification. In some applications, the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The receiver cannot detect the incoming video data range, and there is no required range specification in the HDMI AVI packet. Therefore the receiver's firmware will have to program the scaling depending on the detected video format. Refer to the *SiI9013 HDMI Receiver Programmer's Reference* (SiI-PR-1012) for more details.

When the receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr output values to 1 to 254.

## 4:2:2/4:4:4 Decimator

Additional logic can convert from 4:2:2 to 4:4:4 or from 4:4:4 to 4:2:2 YCbCr format.

## Default Video Configuration

After hardware RESET, the receiver chip is configured in its default mode. This is summarized in [Table 3](#). For more details, and a complete register listing, refer to the *SiI9013 HDMI Receiver Programmers' Reference* (SiI-PR-1012).

**Table 3. Default Video Processing**

Video Control	Default after Hardware Reset	Notes
HDCP Decryption	HDCP decryption is OFF	1
Color Space Conversion	No color space conversion	1
Color Space Selection	BT.601 used	2
Color Range Scaling	No range scaling	1
4:2:2/4:4:4 Decimator	No conversion	—
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC	—
Data Bit Width	Pixel data is decoded as 8-bit RGB values	1, 3
Pixel Clock Replication	No pixel clock replication	1
Power Down	Everything is powered down	4
Video Output Bus	24-bit SDR mode	—
HDCP Device Type	Sink (end node), not Repeater	—

**Notes:**

1. The receiver assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with a range of 0–255.
2. BT.601 is selected, but no color space conversion is enabled by default.
3. Each color field (R, G, B, Y, Cb, Cr) is decoded as an 8-bit value. 12-bit YCbCr 4:2:2 is programmable.
4. The receiver must be powered up by a write through I<sup>2</sup>C after hardware reset.

## Color Space Conversion

**RGB to YCbCr** The RGB→YCbCr color space converter (CSC) can convert from RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video. If no AVI packets are received, then the default conversion listed by video format in [Table 4](#) should be enabled in the receiver. If a received AVI packet specifies a different conversion, then that specification takes precedence. Note the difference between the RGB range for CE modes and PC modes. For PC mode RGB, color range scaling must also be enabled to create conformant YCbCr output values.

**Table 4. Color Space versus Video Format**

Video Format	Conversion	Formulas	
		CE Mode 16-235 RGB	PC Mode 0-255 RGB
640 x 480	ITU-R BT.601	$Y = 0.299R' + 0.587G' + 0.114B'$	$Y = 0.257R' + 0.504G' + 0.098B' + 16$
480i	ITU-R BT.601	$Cb = -0.172R' - 0.339G' + 0.511B' + 128$	$Cb = -0.148R' - 0.291G' + 0.439B' + 128$
576i	ITU-R BT.601	$Cr = 0.511R' - 0.428G' - 0.083B' + 128$	$Cr = 0.439R' - 0.368G' - 0.071B' + 128$
480p	ITU-R BT.601		
576p	ITU-R BT.601		
240p	ITU-R BT.601		
288p	ITU-R BT.601		
720p	ITU-R BT.709	$Y = 0.213R' + 0.715G' + 0.072B'$	$Y = 0.183R' + 0.614G' + 0.062B' + 16$
1080i	ITU-R BT.709	$Cb = -0.117R' - 0.394G' + 0.511B' + 128$	$Cb = -0.101R' - 0.338G' + 0.439B' + 128$
1080p	ITU-R BT.709	$Cr = 0.511R' - 0.464G' - 0.047B' + 128$	$Cr = 0.439R' - 0.399G' - 0.040B' + 128$

**YCbCr to RGB** The YCbCr→RGB color space converter can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to the detailed formulas in [Table 5](#). Note the difference between the RGB range for CE modes and PC modes.

**Table 5. YCbCr-to-RGB Color Space Conversion Formulas**

Video Formats	Conversion	YCbCr Input Color Range
<b>YCbCr 16-235 Input to RGB 16-235 Output</b>	<b>601</b>	$R' = Y + 1.371(Cr - 128)$ $G' = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$ $B' = Y + 1.732(Cb - 128)$
	<b>709</b>	$R' = Y + 1.540(Cr - 128)$ $G' = Y - 0.459(Cr - 128) - 0.183(Cb - 128)$ $B' = Y + 1.816(Cb - 128)$
<b>YCbCr 16-235 Input to RGB 0-255 Output</b>	<b>601</b>	$R' = 1.164(Y - 16) + 1.596(Cr - 128)$ $G' = 1.164(Y - 16) - 0.813(Cr - 128) - 0.391(Cb - 128)$ $B' = 1.164(Y - 16) + 2.018(Cb - 128)$
	<b>709</b>	$R' = 1.164(Y - 16) + 1.793(Cr - 128)$ $G' = 1.164(Y - 16) - 0.534(Cr - 128) - 0.213(Cb - 128)$ $B' = 1.164(Y - 16) + 2.115(Cb - 128)$

**Note:** Video specifications such as SMPTE-296M (Section 7.7-7.8) limit the range of R'G'B' or YCbCr results to 16–235 (for 8-bit luma and RGB) and 16–240 (for 8-bit chroma). When values outside this range are received into the SiI9013 HDMI Receiver, and no internal color space conversion or up/down-sampling is performed, the output color values will also be outside this range. PC mode video in the RGB space uses the entire 0–255 range. Compression may be enabled in the SiI9013 HDMI Receiver using the VID\_MODE register. When enabled, compression will constrain the luma output to 16–235 and the chroma output to 16–240. CE mode video in the RGB space is limited to 0–235/240.

## Automatic Video Configuration

The SiI9013 HDMI Receiver, like the SiI9025 and SiI9033 receivers, includes logic to support auto video mode detection. In this manner, the output video bus can be locked to one format for all possible incoming video formats. This simplifies the firmware overhead as well as the amount of microcontroller intervention. The video output mode is set using the OUTMODE register. Supported output video modes are shown in [Table 6](#). The SiI9013 HDMI Receiver uses bits in the AVI InfoFrame, as shown in [Table 7](#), to enable these modes.

**Table 6. OutMode Programming**

OUTMODE[7:0]	Color	Format	Width	MUX	Sync
0b00000000	RGB	4:4:4	24	N	Sep.
0b10000000	YCbCr	4:4:4	24	N	Sep.
0b11000000	YCbCr	4:2:2	16	N	Sep.
0b11001000	YCbCr	4:2:2	20	N	Sep.
0b11010000	YCbCr	4:2:2	8	N	Emb.
0b11011000	YCbCr	4:2:2	10	N	Emb.
0b11100000	YCbCr	4:2:2	8	Y	Sep.
0b11101000	YCbCr	4:2:2	10	Y	Sep.
0b11110000	YCbCr	4:2:2	8	Y	Emb.
0b11111000	YCbCr	4:2:2	10	Y	Emb.

### Notes:

1. Multiplexed 4:2:2 YCbCr output allowed only in 24-bit interface mode.
2. All other values for OUTMODE are reserved.

**Table 7. AVI InfoFrame Video Path Details**

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	Color Space	C[1:0]	Colorimetric	PR[3:0]	Pixel Repetition
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:4:4	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:2:2	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Future	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

**Notes:**

1. The Auto Video Configuration requires that the AVI information is accurate. If the Video Identification Code in AVI Byte 4 is zero, then the AVC logic reverts to RGB 4:4:4 input.
2. If AVI InfoFrame packets do not arrive for 4 or more frames, then the AVI data registers are cleared, and the AVC logic will revert to RGB 4:4:4, with no pixel replication.
3. Refer to the EIA/CEA-861B Specification for more details on the AVI InfoFrame packet.
4. The SiI9013 HDMI Receiver can support only pixel replication modes 0b0000, 0b0001 and 0b0011. The other modes are unsupported and can result in unpredictable behavior.

**Audio Processing Logic**

The audio processing logic block receives the audio stream packets from the HDMI data bus and puts them into an audio FIFO. The audio sample clock is recovered using information in the N/CTS packets and uses that sample clock to pull the data out of the FIFO. The audio data can be output from the receiver as S/PDIF or I<sup>2</sup>S or both. Registers are provided to control the byte formatting of the I<sup>2</sup>S data to simplify direct connection to a variety of audio DACs.

Audio sample rates from 32 kHz to 192 kHz are supported by the I<sup>2</sup>S outputs and by the S/PDIF output. PCM data (IEC 60958) and compressed data (IEC 61937) can be output on the I<sup>2</sup>S and S/PDIF outputs. MCLK frequencies support various audio sample rates as shown in Table 8 (in MHz).

**Table 8. Supported MCLK Frequencies in MHz**

Multiple of Fs	Audio Sample Rate, Fs						
	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	11.290	12.288	22.579	24.576
256	8.192	11.290	12.288	22.579	24.576	45.158	49.152
384	12.288	16.934	18.432	33.869	36.864		
512	16.384	22.579	24.576	45.158	49.152		

**Auto Audio Configuration**

The SiI9013 HDMI Receiver can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame, and HDMI registers. Audio output will only be enabled when all necessary conditions are met. If any critical condition is missing, then the audio output is disabled automatically.

**Soft Mute**

On command from a register bit, the SiI9013 HDMI Receiver will progressively reduce the audio data amplitude to mute the sound in a controlled manner. This is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being heard from the audio DACs.

**I<sup>2</sup>S Channel Mapping**

Any of the four I<sup>2</sup>S channels carried on the HDMI link may be mapped to any of the four SD[0:3] outputs, using the channel mapping logic programmable with registers. This feature is useful as there is no standardized mapping of audio

channels to audio speaker output positions. A detailed explanation can be found in the *SiI9013 HDMI Receiver Programmer's Reference* (SiI-PR-1012).

## Control and Configuration

### Registers/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9013 HDMI Receiver. These registers are used to perform HDCP authentication, audio, video, and auxiliary format processing, CEA-861B info-packet format, and power-down control.

The registers are accessible from one of two I<sup>2</sup>C ports. The first port is the DDC port which is connected through the HDMI cable to the HDMI host. It is used by the host to control the SiI9013 HDMI Receiver for HDCP operation. The second port is the local I<sup>2</sup>C port which is used by the local display micro to control the SiI9013 HDMI Receiver. This is shown in Figure 6. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers.

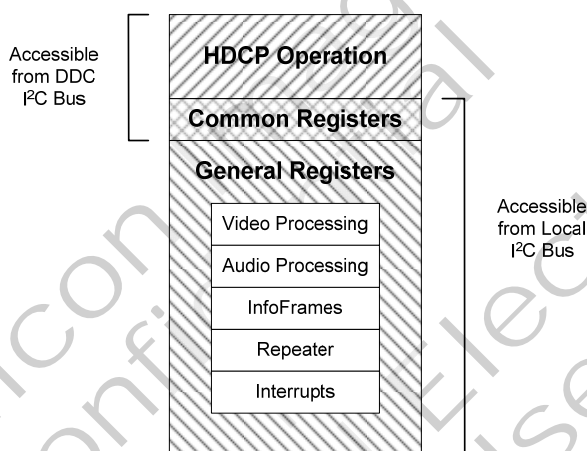


Figure 6. I<sup>2</sup>C Register Domains

### I<sup>2</sup>C Ports

The SiI9013 HDMI Receiver provides two I<sup>2</sup>C interfaces, one to communicate back to the HDMI or DVI host across the DDC channel and another for initialization and control by a microcontroller in the display. Both I<sup>2</sup>C interfaces are 5 V tolerant.

#### E-DDC Bus Interface to HDMI Host

The E-DDC I<sup>2</sup>C interface (DSDA, DSCL) on the SiI9013 HDMI Receiver is a slave interface capable of running up to 100 kHz and is used for HDCP operations.

The SiI9013 HDMI Receiver is accessible on the E-DDC bus at device address 0x74. This complies with the HDCP 1.1 Specification.

#### I<sup>2</sup>C Interface to Display Controller

The Controller I<sup>2</sup>C interface (CSDA, CSCL) on the SiI9013 HDMI Receiver is a slave interface capable of running up to 400 kHz. This bus is used to configure the SiI9013 HDMI Receiver by reading and writing to the appropriate registers. The SiI9013 HDMI Receiver is accessible on the local I<sup>2</sup>C bus at two device addresses. The logic state of the CI2CA pin is latched on the rising edge of RESET#, providing a choice of two pairs of device addresses.

Table 9. Control of Local I<sup>2</sup>C Address with CI2CA Pin

	CI2CA = Pull Down	CI2CA = Pull Up
First Device Addr	0x60	0x62
Second Device Addr	0x68	0x6A

# Electrical Specifications

## Absolute Maximum Conditions

Table 10. Absolute Maximum Conditions<sup>1</sup>

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC	I/O Pin Supply Voltage	-0.3	—	4.0	V	2, 3
PVCC	TMDS PLL Supply Voltage	-0.3	—	4.0	V	2
AVCC	TMDS Analog Supply Voltage	-0.3	—	4.0	V	2
AUDPVCC18	Audio PLL Supply Voltage	-0.3	—	2.5	V	2, 3, 4
CVCC18	Digital Core Supply Voltage	-0.3	—	2.5	V	2, 3
DVCC18	TMDS Digital Logic Supply Voltage	-0.3	—	2.5	V	2
XTALVCC	ACR PLL Crystal Oscillator Supply Voltage	-0.3	—	4.0	V	2
REGVCC	ACR PLL Regulator Supply Voltage	-0.3	—	4.0	V	2, 4
V <sub>I</sub>	Input Voltage	-0.3	—	IOV <sub>CC</sub> + 0.3	V	2
V <sub>I2C</sub>	Input Voltage on I <sup>2</sup> C Pins	-0.3	—	6.0	V	—
V <sub>IPWR5V</sub>	Input Voltage on PWR5V pin	-0.3	—	6.0	V	—
T <sub>J</sub>	Junction Temperature	—	—	125	°C	—
T <sub>STG</sub>	Storage Temperature	-65	—	150	°C	—
DIFF33	Difference between two 3.3 V Power Pins	—	—	1.0	V	5
DIFF18	Difference between two 1.8 V Power Pins	—	—	1.0	V	5
DIFF3318	Difference between any 3.3 V and 1.8 V Pins	-1.0	—	2.0	V	5, 6

**Notes:**

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot may not exceed absolute maximum conditions.
4. REGVCC is internally regulated to 1.8 V and controls the audio PLL. AUDPVCC18 supplies the audio PLL logic.
5. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 11.
6. No 1.8 V pin may be more than DIFF3318[min] higher than any 3.3 V pin. No 3.3 V pin may be more than DIFF3318[max] higher than any 1.8 V pin.

## Normal Operating Conditions

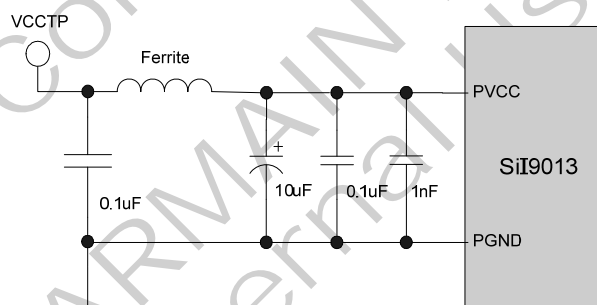
**Table 11. Normal Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC	I/O Pin Supply Voltage	3.0	3.3	3.6	V	1, 4
PVCC	TMDS PLL Supply Voltage	3.0	3.3	3.6	V	3, 4, 8
AVCC	TMDS Analog Supply Voltage	3.0	3.3	3.6	V	1, 3, 5, 8
AUDPVCC18	Audio PLL Supply Voltage	1.62	1.8	1.98	V	—
CVCC18	Digital Core Supply Voltage	1.62	1.8	1.98	V	2
DVCC18	TMDS Digital Logic Supply Voltage	1.62	1.8	1.98	V	2
XTALVCC	ACR PLL Crystal Oscillator Supply Voltage	3.0	3.3	3.6	V	4
REGVCC	ACR PLL Regulator Supply Voltage	3.0	3.3	3.6	V	4
V <sub>CCN</sub>	Supply Voltage Noise	—	—	100	mV <sub>P-P</sub>	6
T <sub>A</sub>	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ <sub>ja</sub>	Ambient Thermal Resistance (Exposed Pad Soldered)	—	—	29	°C/W	7
	Ambient Thermal Resistance (Exposed Pad Not Soldered)	—	—	48.1	°C/W	7

**Notes:**

1. IOVCC and AVCC pins should be controlled from one power source.
2. AUDPVCC18, CVCC18 and DVCC18 should be controlled from one power source.
3. A ferrite bead should be placed between PVCC and AVCC to limit the noise level on the PVCC pins. See Figure 37 for details.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 11.
5. The HDMI 1.1 specification requires termination voltage (AVCC) to be controlled to 3.3 V ±5%.
6. The supply voltage noise is measured at test point VCCTP shown in Figure 7. The ferrite bead provides filtering of power supply noise. The figure is representative.
7. Airflow at 0 m/s.
8. For applications above 135 MHz, use +3.3 V–5% / +10% power supply for these pins to guarantee reliable operation.

Schematics on page 45 show decoupling and power supply regulation.


**Figure 7. Test Point VCCTP for VCC Noise Tolerance Spec**

## DC Specifications

### Digital I/O Specifications

**Table 12. Digital I/O Specifications**

Symbol	Parameter	Pin Type <sup>3</sup>	Conditions <sup>2</sup>	Min	Typ	Max	Units	Note
V <sub>IH</sub>	High-level Input Voltage	LVTTL	—	2.0	—	—	V	—
V <sub>IL</sub>	Low-level Input Voltage	LVTTL	—	—	—	0.8	V	—
V <sub>TH+</sub>	LOW to HIGH Threshold	Schmitt	—	1.9	—	—	V	5
V <sub>TH-</sub>	HIGH to LOW Threshold	Schmitt	—	—	—	0.7	V	5
V <sub>OH</sub>	High-level Output Voltage	LVTTL	—	2.4	—	—	V	10
V <sub>OL</sub>	Low-level Output Voltage	LVTTL	—	—	—	0.4	V	10
I <sub>OL</sub>	Output Leakage Current	—	High Impedance	-10	—	10	μA	—
V <sub>ID</sub>	Differential Input Voltage	—	—	75	250	1000	mV	4
I <sub>OD4</sub>	4mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	6.2	12.4	19	mA	1, 6, 7
			V <sub>OUT</sub> = 0.4 V	4.5	6.6	7.6	mA	1, 6, 7
I <sub>OD8</sub>	8mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	12.3	24.8	38	mA	1, 6, 8
			V <sub>OUT</sub> = 0.4 V	8.9	13.2	15.2	mA	1, 6, 8
I <sub>OD12</sub>	12mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	18.5	37.1	56.9	mA	1, 6, 8
			V <sub>OUT</sub> = 0.4 V	1.0	19.7	22.7	mA	1, 6, 8
R <sub>PD</sub>	Internal Pull Down Resistor	Outputs	IOVCC = 3.3 V	—	58	—	kΩ	1, 11
I <sub>OPD</sub>	Output Pull Down Current	Outputs	IOVCC = 3.6 V	—	60	90	μA	1, 11
I <sub>IPD</sub>	Input Pull Down Current	Input	IOVCC = 3.6 V	—	60	90	μA	1, 12
R <sub>TERM</sub>	Termination Resistance	Inputs	Single-ended	45	—	55	Ω	13

**Notes:**

- These limits are guaranteed by design.
- Under normal operating conditions unless otherwise specified, including output pin loading C<sub>L</sub> = 10 pF.
- Refer to the [Pin Descriptions](#) section (beginning on page 25) for pin type designations for all package pins.
- Differential input voltage is a single-ended measurement, according to DVI Specification.
- Schmitt trigger input pin thresholds V<sub>TH+</sub> and V<sub>TH-</sub> correspond to V<sub>IH</sub> and V<sub>IL</sub>, respectively.
- Minimum output drive specified at ambient = 7 °C and IOVCC = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC = 3.6 V.
- I<sub>OD4</sub> Output applies to pins QO[23:0], SPDIF, SCK, WS, SD[3:0], INT, and MUTEOUT.
- I<sub>OD8</sub> Output applies to pins QE[23:0], DE, HSYNC, VSYNC, and MCLK.
- I<sub>OD12</sub> Output applies to pins SCDT and ODCK.
- Note that the SPDIF output pin drives LVTTL levels, not the low-swing levels defined by IEC958.
- The chip includes an internal pull-down resistor on many of the output pins. Refer to pages 25–26. When floating, these pins draw a pull down current according to this specification when the signal is driven HIGH by another source device.
- The MCLK pin is an I/O pin with an internal pull down resistor. The pin draws a pull down current according to this specification.
- Previous Panellink parts required an external resistor, R<sub>EXT</sub>, to match the receiver to the interface impedance. The termination is now controlled internally by the SiI9013 HDMI Receiver and no external resistor is required.

## DC Power Supply Specifications

### Total Power versus Power-Down Modes

**Table 13. Total Power versus Power-Down Modes**

Symbol	Parameter	Mode	Frequency (MHz)	Typ <sup>1</sup>		Max <sup>2</sup>		Units	Note
				3.3 V	1.8 V	3.3 V	1.8 V		
I <sub>PDQ3</sub>	Complete Power-Down Current	A	—			18	0	mA	3, 6
I <sub>PDS</sub>	Sleep Power-down Current	B	27			111	3	mA	4, 7
			74.25			123	14	mA	
			108			131	21	mA	
			150			143	30	mA	
			162			146	35	mA	
I <sub>STBY</sub>	Standby Current	C	27			119	41	mA	4, 8
			74.25			131	109	mA	
			108			139	157	mA	
			150			152	217	mA	
			162			154	227	mA	
I <sub>UNS</sub>	Unselected Current	D	27	151	51	146	48	mA	4, 9
			74.25	166	128	166	131	mA	
			108	176	178	176	179	mA	
			150	187	244	188	248	mA	
			162	190	259	193	261	mA	
I <sub>CCT</sub>	Normal Operating Current	E	27	158	51	173	51	mA	4
			74.25	184	130	222	127	mA	
			108	202	179	261	182	mA	
			150	217	244	314	250	mA	
			162	223	259	310	263	mA	

#### Notes:

- Typical Power Conditions measured under the following conditions:
  - Typical Process silicon, nominal VCC operating at T = 25 °C.
  - Video: 24-bit RGB, SMPTE-133 color video test pattern.
  - Audio: 8-channel I<sup>2</sup>S audio with MCLK = 256 x Fs, Fs = 48 kHz (480p) and Fs = 96 kHz (all other modes).
- Maximum Power Conditions measured under the following conditions:
  - Fast-Fast Process silicon, VCC + 10% operating at T = 0 °C.
  - Video: 24-bit RGB, Fine Dot Moire (1 pixel on/off) video test pattern.
  - Audio: 8-channel I<sup>2</sup>S audio with MCLK = 512 x Fs, Fs = 48 kHz (480p) and Fs = 96 kHz (all other modes).
- Power is not related to input pixel clock (RxC) frequency because the TMDS port is powered down.
- Power is related to input clock (RxC) frequency.
- Registers are always accessible on local I<sup>2</sup>C (CSDA/CSCL) without an active link clock.
- Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals at either TMDS port. I<sup>2</sup>C access is still available.
- Power Down Mode B: Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
- Power Down Mode C: Powers down core logic, ACR PLL, and output pins. HDCP does not continue. Interrupts disabled. INT pin show state of SCDT for the selected TMDS port.
- Power Down Mode D: Monitor SCDT on selected TMDS port with outputs floating. HDCP continues, but the output of the receiver can be connected to a shared bus.

**Power Down Mode Definitions****Table 14. Power Down Mode Definitions**

Mode		Bit States					Description
		PDTOT#	PD_12CH#	PD Clks <sup>1</sup>	PD Outs <sup>2</sup>	PD#	
A	Power Down	0	X	X	X	X	Minimum power. Everything is powered off. Host sees no termination of TMDS signals at either TMDS port. I <sup>2</sup> C access is still available.
B	Sleep Mode Power	1	0	0	X	0	Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
C	Standby Power	1	1	1	1	0	Powers down core logic, ACR PLL, and output pins. HDCP does not continue. Interrupts disabled. INT pin show state of SCDT for the selected TMDS port.
D	Unselected Power	1	1	1	0	1	Monitor SCDT on selected TMDS port with outputs floating. HDCP continues, but the output of the receiver can be connected to a shared bus.
E	Full Power	1	1	1	1	1	Normal Operating Condition.

**Notes:**

1. PD Clks includes PD\_MCLK#, PD\_XTAL#, and PD\_PCLK#, which are all set to zero.
2. PD Outs includes PD\_AO# and PD\_VO#, which are all set to zero.

**AC Specifications****Video AC Timing Specifications****Table 15. Output Rise and Fall Times (All Output Modes)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
D <sub>LHT</sub>	LOW-to-HIGH Transition VSYNC, HSYNC, ODCK, DE, QE[23:0], and QO[23:0]	C <sub>L</sub> = 10 pF	—	—	3	ns	Figure 13	2
D <sub>HLT</sub>	HIGH-to-LOW Transition VSYNC, HSYNC, ODCK, DE, QE[23:0], and QO[23:0]	C <sub>L</sub> = 10 pF	—	—	3	ns	Figure 13	2

**Table 16. 12-Bit DDR Output Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
R <sub>CIP</sub>	ODCK Cycle Time	1X Clock	12.1	—	40	ns	Figure 14	2, 10
F <sub>CIP</sub>	ODCK Frequency	1X Clock	25	—	81	MHz	—	2, 10
T <sub>DUTY</sub>	ODCK Duty Cycle	C <sub>L</sub> = 10 pF	45%	—	55%	R <sub>CIP</sub>	Figure 14	2, 5, 9
T <sub>CK2OUT</sub>	Clock-to-Output Delay	C <sub>L</sub> = 10 pF	1.0	—	3.5	ns	Figure 14	2, 9

**Table 17. 8/10/12/16/20/24-Bit SDR Output Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
R <sub>CIP</sub>	ODCK Cycle Time	1X Clock	6	—	40	ns	Figure 14	2, 10
F <sub>CIP</sub>	ODCK Frequency	1X Clock	25	—	162	MHz	—	2, 10
T <sub>DUTY</sub>	ODCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	R <sub>CIP</sub>	Figure 14	2, 5, 9
T <sub>CK2OUT</sub>	Clock-to-Output Delay	C <sub>L</sub> = 10 pF	1.0	—	3.5	ns	Figure 14	2, 9

**Table 18. 48-Bit SDR Output Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
R <sub>CIP</sub>	ODCK Cycle Time	1X Clock	12.1	—	40	ns	Figure 14	2, 10
F <sub>CIP</sub>	ODCK Frequency	1X Clock	25	—	81	MHz	—	2, 10
T <sub>DUTY</sub>	ODCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	R <sub>CIP</sub>	Figure 14	2, 5, 9
T <sub>CK2OUT</sub>	Clock-to-Output Delay	C <sub>L</sub> = 10 pF	1.0	—	4.0	ns	Figure 14	2, 9

**Note:** Unless otherwise noted, the threshold levels for clock and data measurements are measured at 1.65 V.

**Table 19. TMDS Input Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
F <sub>RXC</sub>	Differential Input Clock Frequency	—	25	—	162	MHz	—	—
T <sub>DPS</sub>	Intra-Pair (+ to –) Differential Input Skew	—	—	—	TBIT	ps	—	2, 7
T <sub>CCS</sub>	Channel to Channel Differential Input Skew	—	—	—	T <sub>CIP</sub>	ns	Figure 10	2, 6
T <sub>JIT</sub>	Differential Input Clock Jitter tolerance	74.25 MHz	—	—	400	ps	—	2, 3, 4
		162 MHz	—	—	182	ps		

**Notes:**

- Under normal operating conditions unless otherwise specified, including output pin loading of C<sub>L</sub> = 10 pF.
- Guaranteed by design.
- Jitter defined per DVI 1.0 Specification, Section 4.6 *Jitter Specification*, as 0.30 Unit Interval. A Unit Interval (UI) is the bit time on the TMDS link, or one-tenth of the link clock period.
- Jitter measured with Clock Recovery Unit per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*. Actual jitter tolerance may be higher depending on the frequency of the jitter.
- Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
- Period in time consisting of 6 serial UI, whereby each UI is equivalent to 1/10 of the F<sub>RXC</sub> Period. For example, if F<sub>RXC</sub> = 165 MHz, then each UI will have a period of TBIT = 606 ps; therefore, T<sub>CIP</sub> = 6xTBIT = 3.6 ns. (See also the applicable Silicon Image HDMI Transmitter Data Sheets).
- 1/10 of the Link Clock Period (see the applicable Silicon Image HDMI Transmitter Data Sheets).
- All output timings are defined at the maximum operating ODCK frequency, F<sub>CIP</sub>, unless otherwise specified.
- See Table 25 and Table 26 on page 22 and 22, respectively, for calculation of worst case output setup and hold times.
- F<sub>CIP</sub> may be the same as F<sub>RXC</sub> or one-half of F<sub>RXC</sub>, depending on OCLKDIV setting.
- R<sub>CIP</sub> is the inverse of F<sub>CIP</sub> and is not a controlling specification.
- Output skew specified when ODCK is programmed to divide-by-two mode.
- Glitches or extra edges in VSYNC may cause HDCP decryption on the receiver side to fail. Disable active video whenever changing from one video mode to another, as such changes may create extra VSYNC edges.

Refer to the *SiI9013 HDMI Receiver Programmer's Guide* (SiI-PR-1012) for more details on controlling timing modes.

## Interrupt Timings

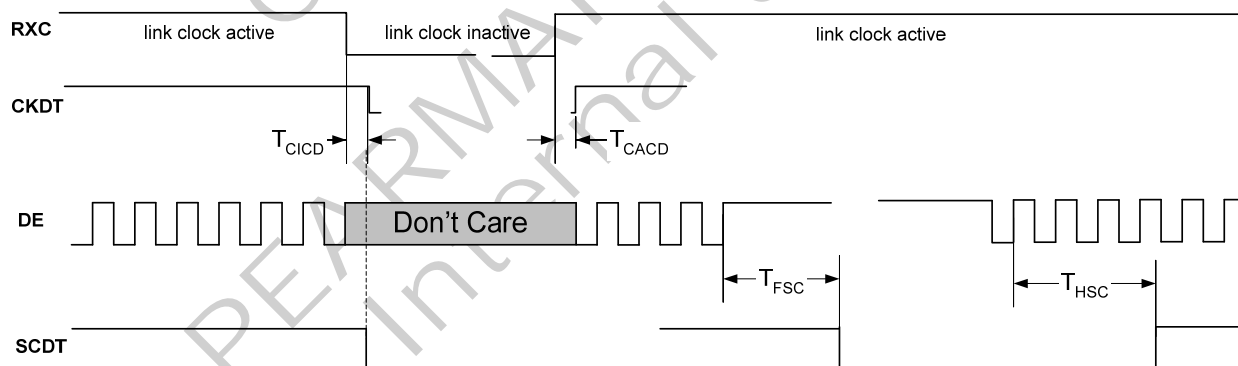
**Table 20. Interrupt Output Pin Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T <sub>FSC</sub>	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 8	1, 2, 3, 8
T <sub>HSC</sub>	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 8	1, 2, 4, 8
T <sub>CICD</sub>	RXC inactive to CKDT LOW	—	—	—	100	μs	Figure 8	1, 2, 8
T <sub>CACD</sub>	RXC active to CKDT HIGH	—	—	—	10	μs	Figure 8	1, 2, 8
T <sub>INT</sub>	Response Time for INT from Input Change	—	—	—	100	μs	—	1, 5, 8
T <sub>CIOD</sub>	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
T <sub>CAOD</sub>	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
T <sub>SRRF</sub>	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	—	7

**Notes:**

- Guaranteed by design.
- SCDT and CKDT are register bits in this device.
- SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150 μs, and the delay for DE LOW is approximately 40 ms.
- SCDT changes to HIGH when clock is active (T<sub>CACD</sub>) and at least 4 DE edges have been recognized. At 720p, the DE period is 22 μs, so SCDT will respond approximately 50 μs after T<sub>CACD</sub>.
- The INT pin will change state after a change in input condition when the corresponding interrupt is enabled.
- Output clock (ODCK) will become active before it becomes stable. Use the SCDT signal as the indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see T<sub>FSC</sub>).
- Software Reset must be asserted and then de-asserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT may be limited by the speed of the I<sup>2</sup>C connection.
- SCDT is HIGH only when CKDT is also HIGH. When the receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a power-down receiver signals a microprocessor connected to the INT pin whenever SCDT changes from LOW to HIGH or from HIGH to LOW.

**Important:** Silicon Image recommends that firmware for the SiI9013 receiver enable automatic software reset (SWRST\_AUTO at 0x60:0x05[4]). SWRST\_AUTO causes SWRST to be asserted whenever the HDMI receiver detects a loss of the TMDS clock (CKDT) or loss of video signals (SCDT). Failure to do so can cause the FIFO\_UNDERRUN interrupt to be incorrectly set, and not able to be cleared except by hardware reset.


**Figure 8. SCDT and CKDT Timing from DE or RXC Inactive/Active**
**Notes:**

- The SCDT shown in Figure 8 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT will change to LOW if DE is stuck HIGH while RXC remains active.
- The CKDT shown in Figure 8 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
- SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T<sub>HSC</sub> after CKDT changes to HIGH.
- The INT output pin will change state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the *SiI9013 HDMI Receiver Programmer's Guide* (SiI-PR-1012) for more details on controlling timing modes.

## Audio AC Timing Specifications

**Table 21. I<sup>2</sup>S Output Port Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T <sub>tr</sub>	SCK Clock Period (TX)	C <sub>L</sub> = 10 pF	1.00	—	—	T <sub>tr</sub>	Figure 17	1, 2
T <sub>HC</sub>	SCK Clock HIGH Time	C <sub>L</sub> = 10 pF	0.35	—	—	T <sub>tr</sub>		1, 2
T <sub>LC</sub>	SCK Clock LOW Time	C <sub>L</sub> = 10 pF	0.35	—	—	T <sub>tr</sub>		1, 2
T <sub>dtr</sub>	SCK to SD and WS	C <sub>L</sub> = 10 pF	—	—	0.8	T <sub>tr</sub>		1, 2
T <sub>htr</sub>	Hold Time SCK to SD and WS	C <sub>L</sub> = 10 pF	0	—	—	—		1, 2
T <sub>SCKDUTY</sub>	SCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	T <sub>tr</sub>		1, 2
T <sub>SCK2SD</sub>	SCK-to-SD Delay	C <sub>L</sub> = 10 pF	–5	—	+5	ns		1, 3
T <sub>AUDDLY</sub>	Audio Pipeline Delay	—	—	40	80	μs	—	1, 4

**Notes:**

- Guaranteed by design.
- Refer to [Figure 17](#). Meets timings in Philips I<sup>2</sup>S Specification.
- Applies also to SCK-to-WS delay.
- Audio delay is the pipeline delay for audio relative to its arrival time at the receiver input. HDMI specifies a maximum delay of 2 ms (Section 7.5). The video delay is insignificant. It is specified in DVI 1.0 to be a maximum of 64 pixel clocks (Table 3-2). At 27 MHz this video delay is less than 3 μs.

**Table 22. S/PDIF Output Port Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T <sub>SPCYC</sub>	SPDIF Cycle Time	C <sub>L</sub> = 10 pF	—	1.0	—	UI	Figure 18	1, 2
F <sub>SPDIF</sub>	SPDIF Frequency	—	4	—	24	MHz		4
T <sub>SPDUTY</sub>	SPDIF Duty Cycle	C <sub>L</sub> = 10 pF	90%	—	110%	UI		2
T <sub>MCLKCYC</sub>	MCLK Cycle Time	C <sub>L</sub> = 10 pF	20	—	250	ns	Figure 19	1, 2
F <sub>MCLK</sub>	MCLK Frequency	C <sub>L</sub> = 10 pF	4	—	50	MHz		1, 2
T <sub>MCLKDUTY</sub>	MCLK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	T <sub>MCLKCYC</sub>		2
T <sub>AUDDLY</sub>	Audio Pipeline Delay	—	—	40	80	μs	—	3

**Notes:**

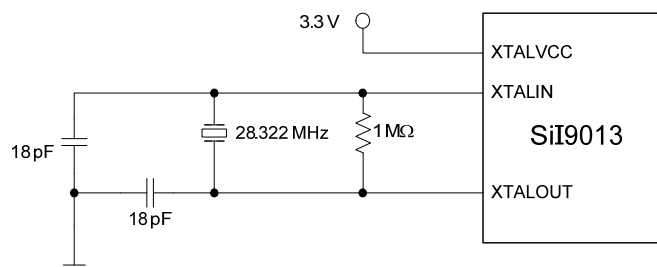
- Guaranteed by design.
- Proportional to unit time (UI), according to sample rate.
- Audio delay is the pipeline delay for audio relative to its arrival time at the receiver input. HDMI specifies a maximum delay of 2 ms (Section 7.5). The video delay is insignificant. It is specified in DVI 1.0 to be a maximum of 64 pixel clocks (Table 3-2). At 27 MHz this video delay is less than 3 μs.
- The SPDIF signal is not a true clock, but is generated from the internal 128Fs clock, for Fs from 32 kHz to 192 kHz.
- S/PDIF is not supported if MCLK = 512 • Fs rate.

**Table 23. Audio Crystal Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
F <sub>XTAL</sub>	External Crystal Freq.	—	26	27	28.5	MHz	<a href="#">Figure 9</a>	1

**Notes:**

- The receiver has been fully characterized for optimum audio quality using 28.322 MHz. A crystal clock with a 100-ppm accuracy is recommended. A less expensive, but not fully characterized circuit, may use 27 MHz.
- When XTALIN is driven by an external clock source, the XTALOUT pin should be left unconnected. Refer to [Figure 41](#) on page 48.


**Figure 9. Audio Crystal Schematic**

**Table 24. Miscellaneous Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T <sub>I2CDVD</sub>	SDA Data Valid delay from SCL falling edge	C <sub>L</sub> = 400 pF	—	—	700	ns	—	—
F <sub>DDC</sub>	Speed on TMDS DDC Ports	C <sub>L</sub> = 400 pF	—	—	100	kHz	—	—
F <sub>I2C</sub>	Speed on Local I <sup>2</sup> C Port	C <sub>L</sub> = 400 pF	—	—	400	kHz	—	—
T <sub>RESET</sub>	RESET# Signal LOW Time for valid reset	—	50	—	—	μs	Figure 20	—
T <sub>BKSVINIT</sub>	BKSV load time	—	42	—	325	ns	—	4

**Notes:**

1. Under normal operating conditions unless otherwise specified, including output pin loading of C<sub>L</sub> = 10 pF.
2. Guaranteed by design.
3. All standard mode (100 kHz) I<sup>2</sup>C timing requirements are guaranteed by design.
4. BKSV load time is the amount of time required to load the KSV value internal to the receiver. An attached HDCP host device should not read the BKSV until after this time. This value is a function of reference crystal frequency input (28.332 MHz) and the pixel clock period. The Min and Max values are based on 165 MHz and 27 MHz pixel clock, respectively. The loading of the BKSV event values is triggered by either an HDCP reset, or by a hardware reset followed by a valid XCLK and pixel clock.

## Timing Diagrams

### TMDS Input Timing Diagrams

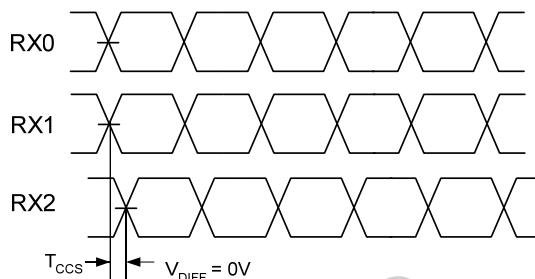


Figure 10. TMDS Channel-to-Channel Skew Timing

### Power Supply Control Timings

#### Power Supply Sequencing

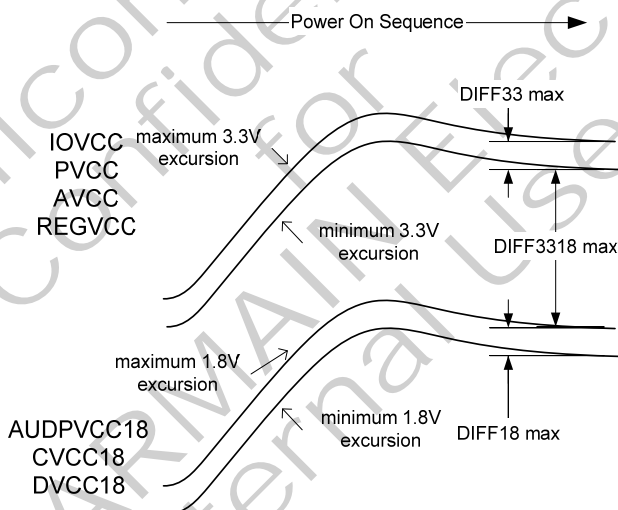


Figure 11. Power Supply Sequencing

#### Configuring Standby Power Mode

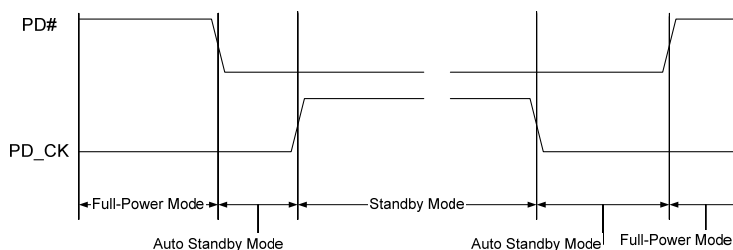


Figure 12. Configuring Standby Power Mode

## Digital Video Output Timing Diagrams

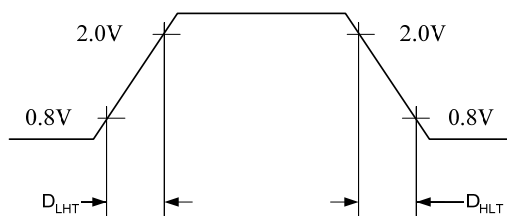


Figure 13. Video Digital Output Transition Times

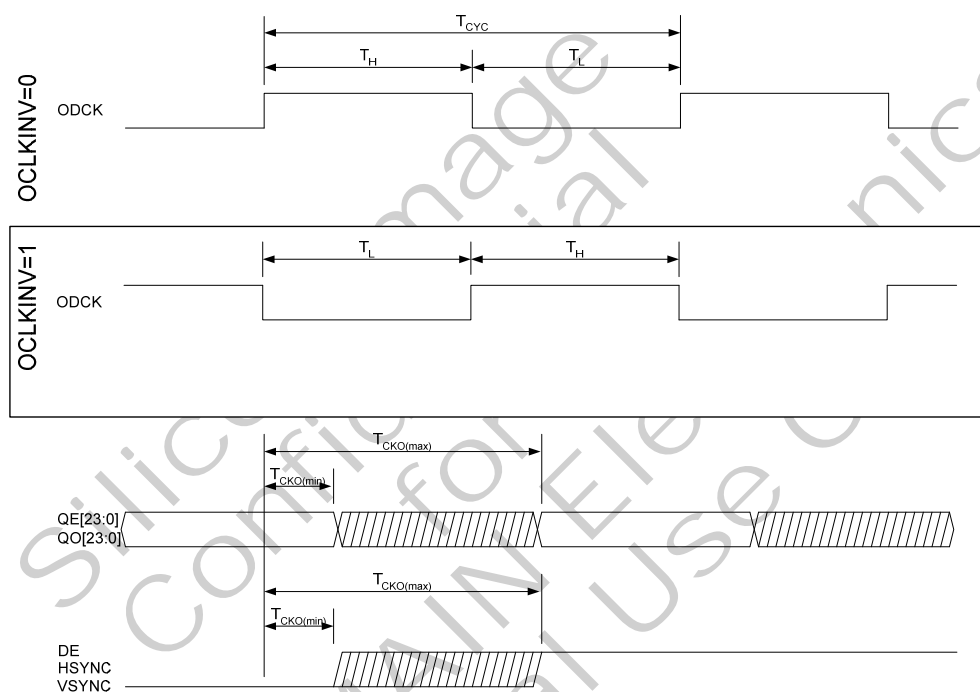


Figure 14. Receiver Clock-to-Output Delay and Duty Cycle Limits

## Calculating Setup and Hold Times

### 24-Bit SDR Mode

Output data is clocked out on one rising (or falling) edge of ODCK, and would then be captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay. This is shown in Figure 15. The falling active ODCK edge is shown with an arrowhead. For OCK\_INV = 1, reverse the logic.

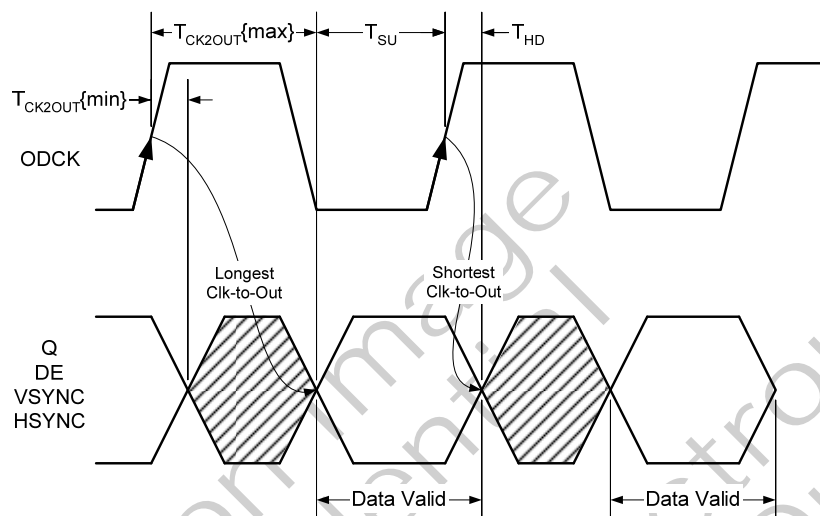


Figure 15. 24-Bit SDR Mode Receiver Output Setup and Hold Times

Table 25 shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 25. Calculation of 24-Bit SDR Output Setup and Hold Times

Mode	Symbol	Parameter	T <sub>ODCK</sub>		Min
24-bit SDR Mode	T <sub>SU24</sub>	Setup Time to ODCK = T <sub>ODCK</sub> - T <sub>CK2OUT</sub> {max}	27 MHz	37.0 ns	33.5
			74.25 MHz	13.5 ns	10.0
			108 MHz	9.3 ns	5.8
			165 MHz	6.1 ns	2.6
	T <sub>HD24</sub>	Hold Time from ODCK = T <sub>CK2OUT</sub> {min}	27 MHz	37.0 ns	1.0

### 12-Bit DDR Mode

Output data is clocked out on both rising and falling edges of ODCK, and would then be captured downstream using the opposite ODCK edge. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle (since every edge is used), and is a function only of the longest ODCK to output delay.

Table 26 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 26. Calculation of 12-Bit DDR Output Setup and Hold Times

Mode	Symbol	Parameter	T <sub>ODCK</sub>		Min
12-bit DDR Mode	T <sub>SU12</sub>	Setup Time to ODCK = T <sub>ODCK</sub> • T <sub>DUTY</sub> {min} - T <sub>CK2OUT</sub> {max}	27 MHz	37.0 ns	13.2
			74.25 MHz	13.5 ns	2.6
	T <sub>HD12</sub>	Hold Time from ODCK = T <sub>CK2OUT</sub> {min}	27 MHz	37.0 ns	1.0

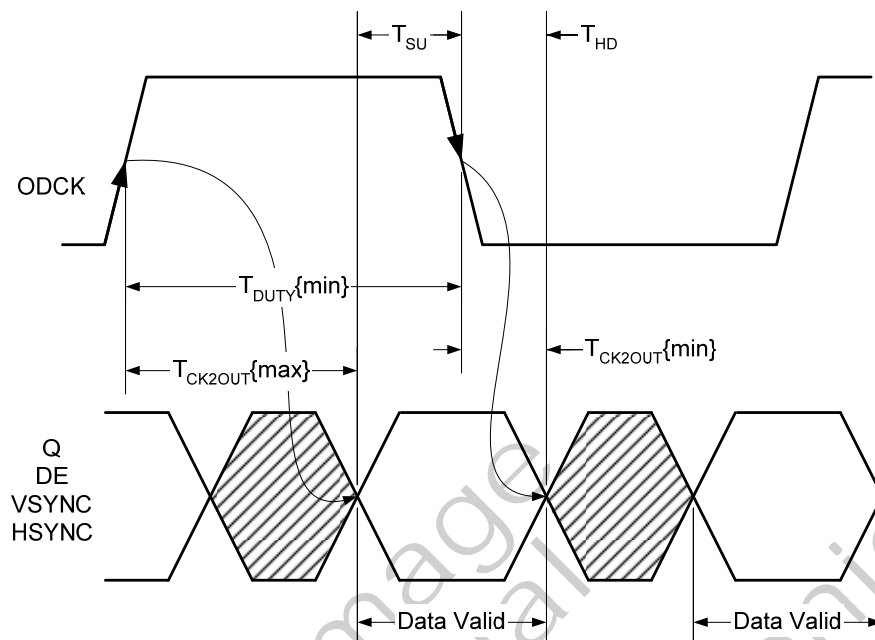


Figure 16. 12-Bit DDR Mode Receiver Output Setup and Hold Times

## Audio Output Timings

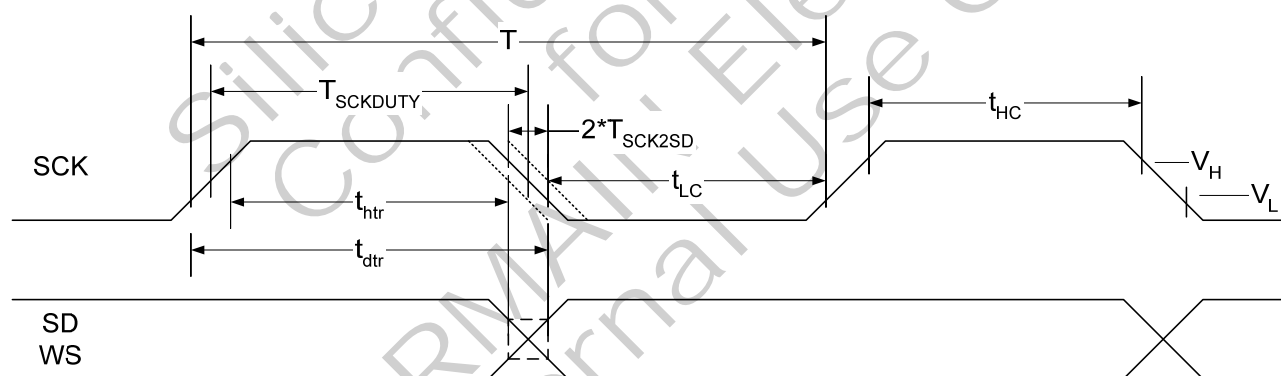


Figure 17. I<sup>2</sup>S Output Timings

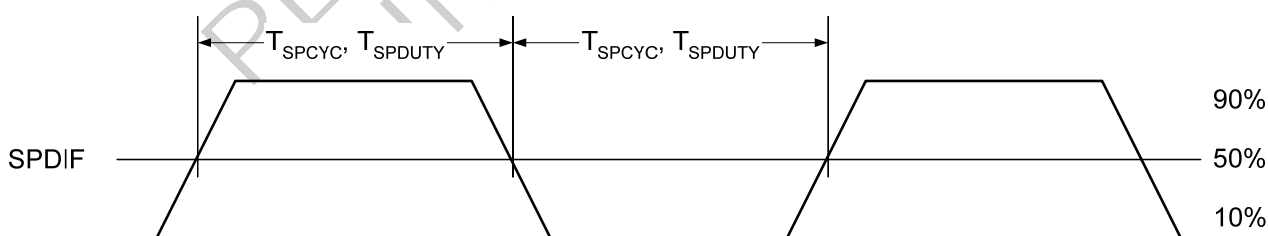


Figure 18. S/PDIF Output Timings

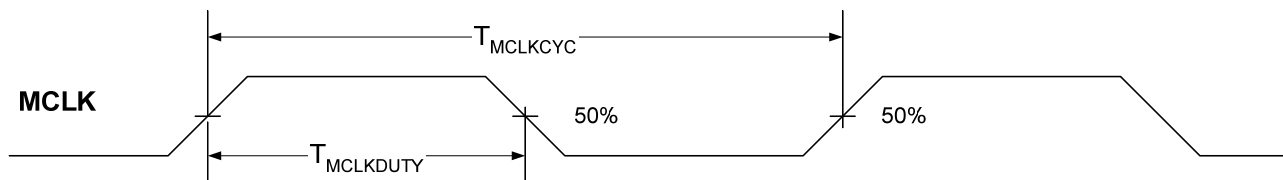
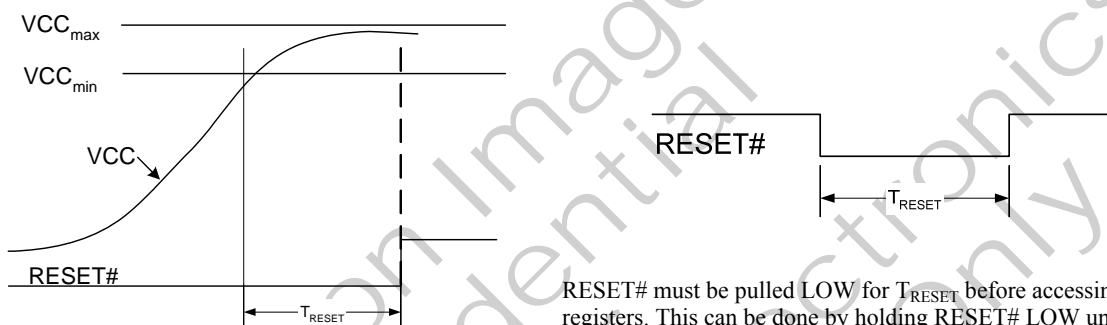


Figure 19. MCLK Timings

## Control Timings

### Reset Timings



Note that VCC must be stable between its limits for Normal Operating Conditions for  $T_{\text{RESET}}$  before RESET# is HIGH.

RESET# must be pulled LOW for  $T_{\text{RESET}}$  before accessing registers. This can be done by holding RESET# LOW until  $T_{\text{RESET}}$  after stable power (shown at the left in Figure 20); OR by pulling RESET# LOW from a HIGH state (shown at the right) for at least  $T_{\text{RESET}}$ .

Figure 20. RESET# Minimum Timings

## Pin Descriptions

### Digital Video Output Pins

Pin Name	Pin #	Description
QE0	124	24-Bit Even Pixel
QE1	123	
QE2	122	
QE3	121	
QE4	117	
QE5	116	
QE6	115	
QE7	114	
QE8	111	
QE9	110	
QE10	109	
QE11	108	
QE12	105	
QE13	104	
QE14	103	
QE15	102	
QE16	101	
QE17	100	
QE18	99	
QE19	96	
QE20	95	
QE21	94	
QE22	93	
QE23	92	

Pin Name	Pin #	Description
QO0	35	24-Bit Odd Pixel
QO1	34	
QO2	33	
QO3	32	
QO4	29	
QO5	28	
QO6	27	
QO7	26	
QO8	23	
QO9	22	
QO10	21	
QO11	20	
QO12	17	
QO13	16	
QO14	15	
QO15	14	
QO16	11	
QO17	10	
QO18	9	
QO19	8	
QO20	5	
QO21	4	
QO22	3	
QO23	2	
DE	127	Data enable.
HSYNC	128	Horizontal Sync.
VSNC	1	Vertical Sync.
ODCK	119	Output Data Clock.

#### Notes:

1. QE[23:0], DE, HSYNC, and VSYNC are 8 mA LVTTTL outputs.
2. QO[23:0] are 4 mA LVTTTL outputs.
3. ODCK is a 12 mA LVTTTL output.
4. HSYNC and VSYNC outputs carry sync signals for both embedded and explicit sync configurations.
5. When transporting video data which uses fewer than 24 bits, the unused bits on the Q[] bus may still carry switching pixel data signals. Unused Q[] bus pins should be unconnected, masked, or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 34), the bits QE[0] through QE[7] will output switching signals.
6. The output data bus, QE[] and QO[], may be wire-ORed to another device such that one device is always floating. However, the QE[] and QO[] pins do not have bus-hold internal pull-ups or pull-downs and cannot pull the bus when all connected devices are floating.

## Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	85	—	LVTTL	In	Crystal Clock Input.
XTALOUT	84	—	LVTTL	Out	Crystal Clock Output.
MCLK	79	—	LVTTL	Out	Audio Master Clock Output.
SCK	76	4 mA	LVTTL	Out	I <sup>2</sup> S Serial Clock Output.
WS	75	4 mA	LVTTL	Out	I <sup>2</sup> S Word Select Output.
SD0	74	4 mA	LVTTL	Out	I <sup>2</sup> S Serial Data Output.
SD1	73	4 mA	LVTTL	Out	I <sup>2</sup> S Serial Data Output.
SD2	72	4 mA	LVTTL	Out	I <sup>2</sup> S Serial Data Output.
SD3	71	4 mA	LVTTL	Out	I <sup>2</sup> S Serial Data Output.
SPDIF	70	4 mA	LVTTL	Out	S/PDIF Audio Output.
MUTE	67	4 mA	LVTTL	Out	Mute Audio Output. <sup>1</sup>

### Notes:

1. The MUTE pin is asserted when there is no active incoming video. This pin is controlled by the internal AUDM register bit. Refer to the *SiI9013 HDMI Receiver Programmer's Reference* (SiI-PR-1012).
2. When XTALIN is driven by an oscillator, the XTALOUT pin should be left unconnected.

## Configuration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	91	4 mA	LVTTL <sup>1</sup>	Out	Interrupt Output
RESET#	89	—	Schmitt	In	Reset Pin. Active LOW. Note that this pin must be dynamically controlled as part of normal operation. This is typically done by the host processor.
DSCL	42	—	Schmitt	In	DDC I <sup>2</sup> C Clock for DDC (5 V tolerant) <sup>2</sup>
DSDA	41	4 mA	Schmitt	Bi-Di	DDC I <sup>2</sup> C Data for DDC (5 V tolerant) <sup>2</sup>
CSCL	40	—	Schmitt	In	Configuration I <sup>2</sup> C Clock (5 V tolerant) <sup>2</sup>
CSDA	39	4 mA	Schmitt	Bi-Di	Configuration I <sup>2</sup> C Data (5 V tolerant) <sup>2</sup>
SCDT	90	12 mA	LVTTL	Out	Indicates active video at HDMI input port.
CI2CA	38	—	LVTTL	In	I <sup>2</sup> C Device Address Select.
PWR5V	44	—	LVTTL	In	TMDS Port Transmitter Detect (5 V tolerant) <sup>3</sup>
RSVDL	88	—	—	In	Reserved, must be tied LOW.
RSVD	48	—	—	—	Reserved Pin, leave unconnected.
NC	43	—	—	—	No connect.

### Notes:

1. The INT pin is programmable as either a push-pull LVTTL output, or as an open-drain output.
2. Level-shifting FETs between these pins and the connector are recommended to prevent any leakage path through these pins whenever the +5 V from the connector is on while the chip power is off. Refer to the [Design Recommendations](#) section on page 42 for details.

## Differential Signal Data Pins

Pin Name	Pin #	Type	Description
RXC+	51	Analog	TMDS input clock pair.
RXC-	50	Analog	
RX0+	55	Analog	TMDS input data pair.
RX0-	54	Analog	
RX1+	59	Analog	TMDS input data pair.
RX1-	58	Analog	
RX2+	63	Analog	TMDS input data pair.
RX2-	62	Analog	

## Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC18	12, 24, 36, 45, 81, 112, 125	Power	Digital Logic VCC	1.8 V
CGND	13, 25, 37, 80, 113, 126	Ground	Digital Logic GND	
IOVCC	7, 19, 31, 68, 77, 98, 107, 120	Power	Input/Output Pin VCC	3.3 V
IOGND	6, 18, 30, 69, 78, 97, 106, 118	Ground	Input/Output Pin GND	
AVCC	49, 53, 57, 61	Power	TMDS Analog VCC	3.3 V
AGND	52, 56, 60, 64	Ground	TMDS Analog GND	
PVCC	47	Power	TMDS PLL VCC	3.3 V
PGND	46	Ground	TMDS PLL GND	
AUDPVCC18	82	Power	ACR PLL VCC	1.8 V
AUDPGND	83	Ground	ACR PLL GND	
DVCC18	66	Power	ACR PLL Digital VCC	1.8 V
DGND	65	Ground	ACR PLL GND	
XTALVCC	86	Power	ACR PLL Crystal Input VCC	3.3 V
REGVCC	87	Power	ACR PLL Regulator VCC	3.3 V

# Video Path

The SiI9013 HDMI Receiver accepts all valid HDMI input formats, and can transform these formats into a variety of video output formats. The following pages describe how to control the video path formatting, and how to assign output pins for each video output format.

## HDMI Input Modes to SiI9013 HDMI Receiver Output Modes

The HDMI link supports transport of video in any of three modes: RGB 4:4:4, YCbCr 4:4:4, or YCbCr 4:2:2. The flexible video path in the SiI9013 HDMI Receiver allows reformatting of video data to a variety of output modes. Table 27 lists the supported transformations and points to the figure for each. In every case, the HDMI link itself carries separate syncs.

Table 27. Translating HDMI Formats to Output Formats

HDMI Input Format	Output Format					
	RGB 4:4:4, Separate Sync	YCbCr 4:4:4, Separate Sync	YCbCr 4:2:2, Separate Sync	YCbCr 4:2:2, Embedded Sync	YC Mux 4:2:2, Separate Sync	YC Mux 4:2:2, Embedded Sync
RGB 4:4:4	Figure 22A	Figure 22B	Figure 22C	Figure 22D	Figure 22E	Figure 22F
YCbCr 4:4:4	Figure 23A	Figure 23B	Figure 23C	Figure 23D	Figure 23E	Figure 23F
YCbCr 4:2:2	Figure 24A	Figure 24B	Figure 24C	Figure 24D	Figure 24E	Figure 24F

Figure 21 is copied from the *SiI9013 HDMI Receiver Programmers' Reference* (SiI-PR-1012). The processing blocks correspond to those shown in Figure 22 through Figure 24.

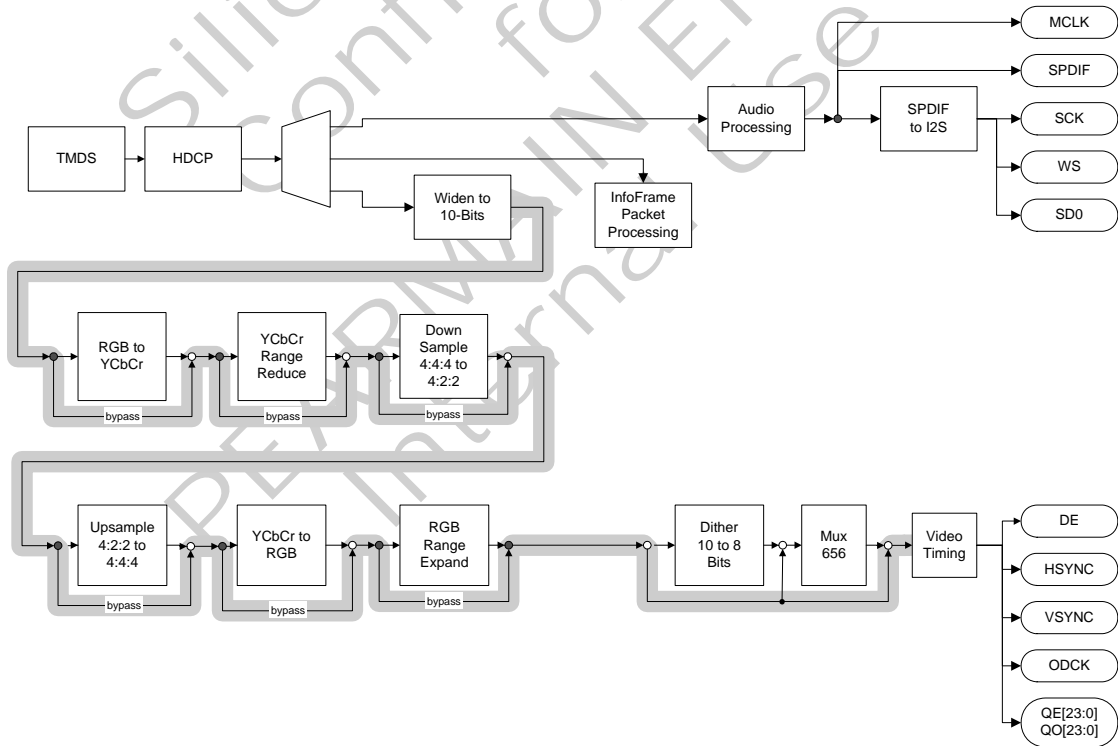


Figure 21. Receiver Video and Audio Data Processing Paths

## HDMI RGB 4:4:4 Input Processing

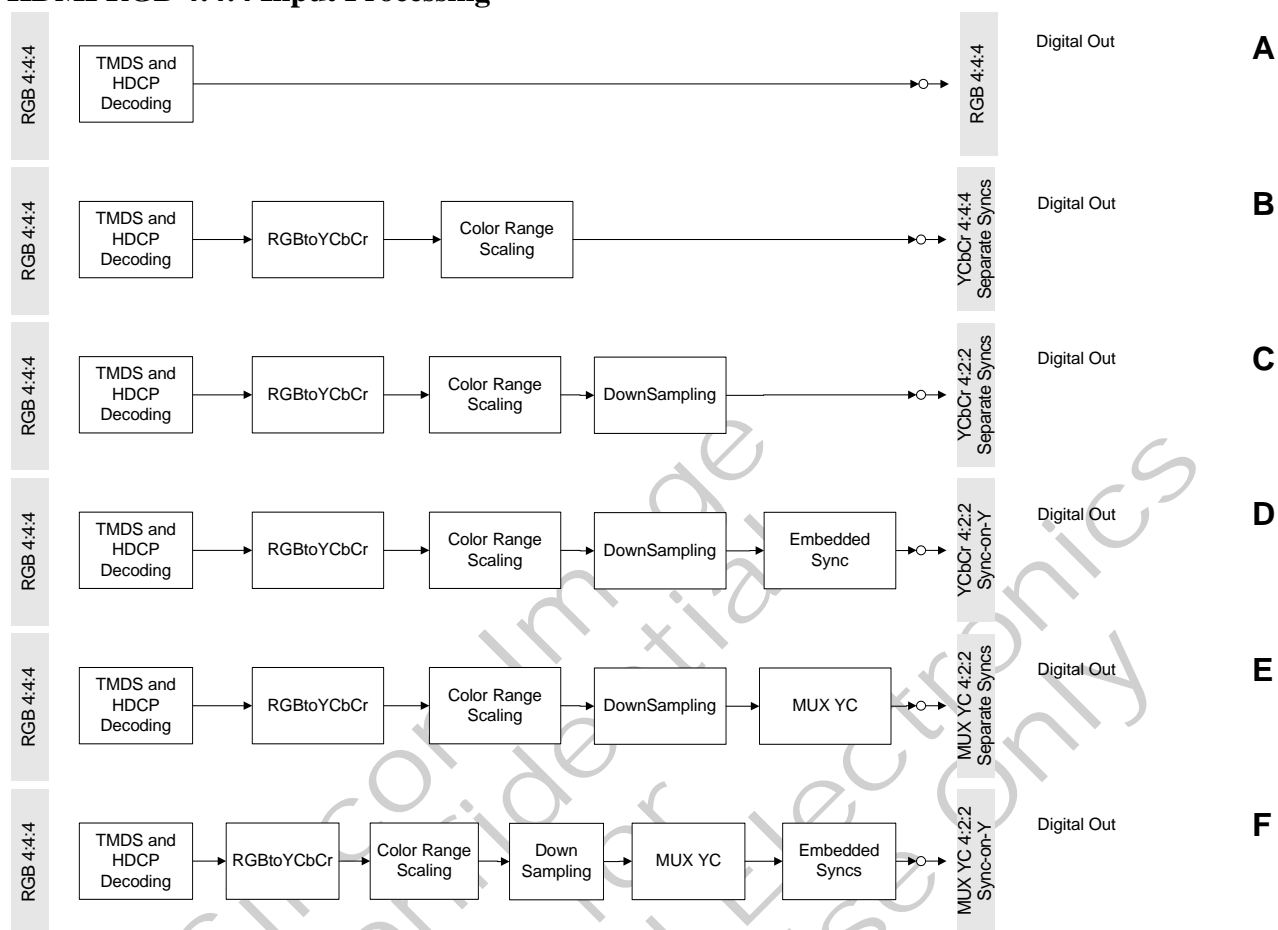


Figure 22. HDMI RGB 4:4:4 Input to Video Output Transformations

## HDMI YCbCr 4:4:4 Input Processing

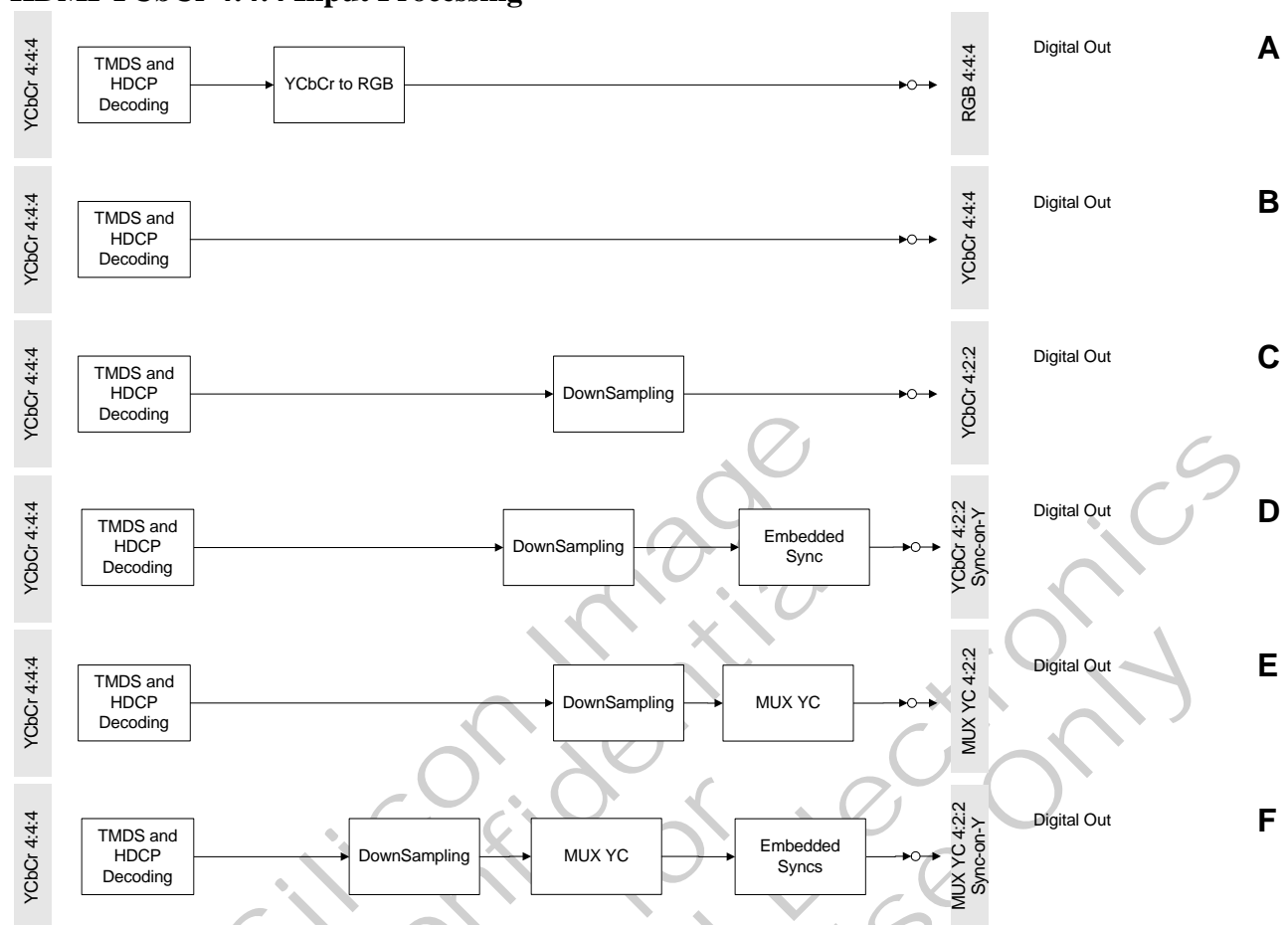
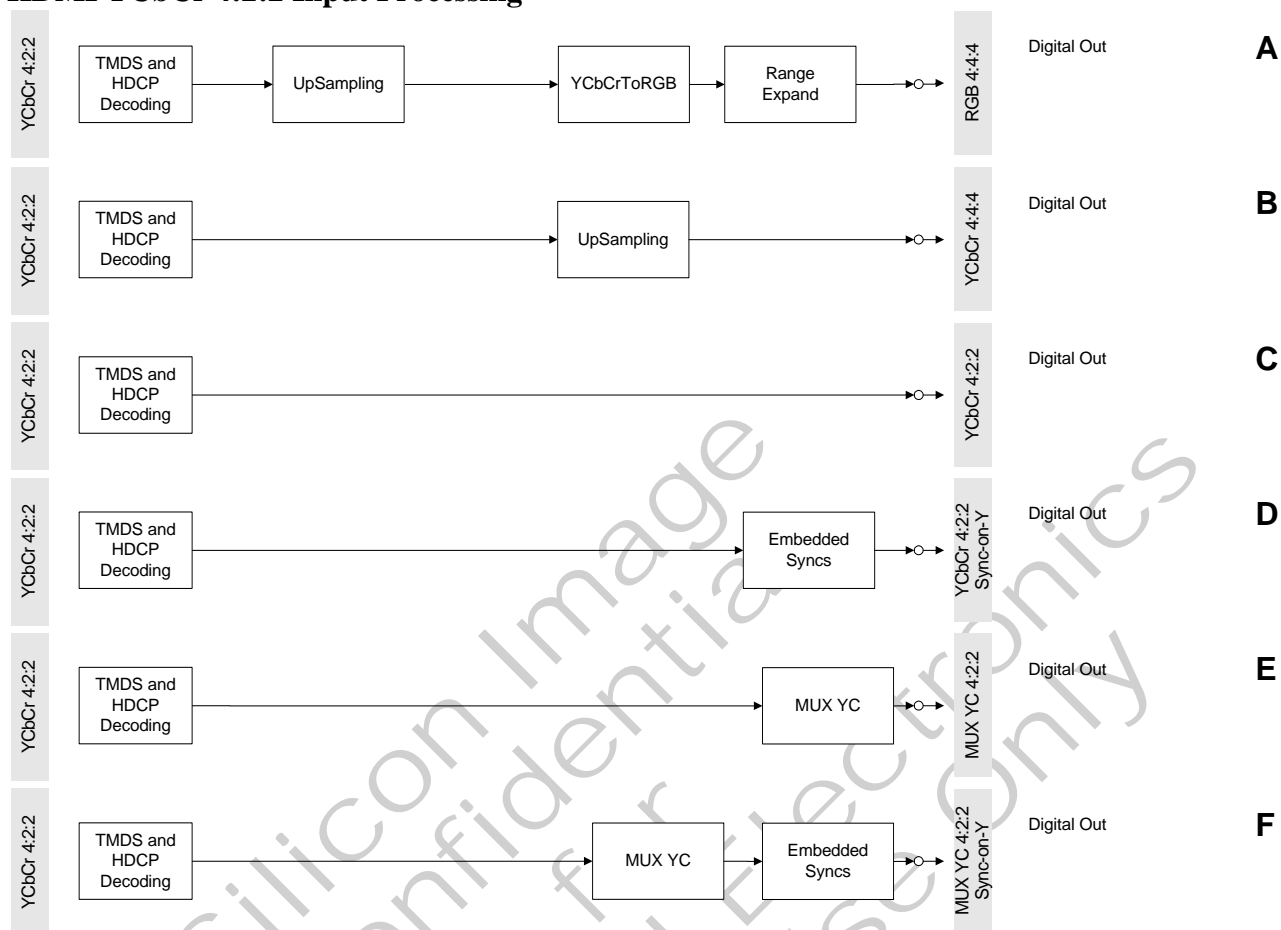


Figure 23. HDMI YCbCr 4:4:4 Input to Video Output Transformations

## HDMI YCbCr 4:2:2 Input Processing



**Figure 24. HDMI YCbCr 4:2:2 Input to Video Output Transformations**

Note that Range Expansion should be enabled only when the output video is a PC mode with a range of 0–255.

## SiI9013 HDMI Receiver Output Mode Configuration

The SiI9013 HDMI Receiver supports multiple output data mappings. Some have explicit control signals while some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings. Refer to the *SiI9013 HDMI Receiver Programmer's Reference* (SiI-PR-1012) for more details.

**Table 28. Output Video Formats**

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Note
RGB 4:4:4	24	1x	Explicit	33	3, 8
YCbCr 4:4:4	24	1x	Explicit	33	1, 3, 8
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Explicit	34	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Explicit	34	2, 3, 9
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	35	2, 5, 6
YC MUX	8, 10, 12	2x	Explicit	36	4, 6, 9
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	37	2, 7, 9, 10
RGB 4:4:4 Sep. Syncs	48	1x	Explicit	38	—
YCbCr 4:4:4 Sep. Syncs	48	1x	Explicit	38	11
RGB or YCbCr 4:4:4 DMO	12	Dual-Edge	Explicit	39	12

**Notes:**

1. 4:4:4 data contains one Cb, one Cr, and one Y value for every pixel.
2. 4:2:2 data contains one Cb and one Cr value for every two pixels, and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to the HDMI Specification 1.0, Section 6.2.3. The link clock must be within the specified range of the SiI9013 HDMI Receiver.
4. In YC MUX mode, data is output on one or two 8-bit channels. A 2x input clock is required.
5. YC MUX mode can embed the syncs using a preamble.
6. YCbCr data can be output on 12 bits (as part of a 24-bit mode or as a 12-bit mode), but the two least-significant bits will be zero since the internal data path is 10 bits wide, unless the data is received across the link as YC MUX 4:2:2 data.
7. SAV/EAV encoding embeds the syncs. A 2x input clock is required.
8. A 2x clock can also be sent with 4:4:4 data. This is necessary for the receiver to reformat such a stream into 4:2:2 data or into a multiplexed YC MUX output format.
9. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to the HDMI Specification 1.0, Section 6.4.
10. 2x clocking does not support YC 4:2:2 Embedded Sync timings for 720p or 1080i, as the output clock frequency would exceed the range allowed for the SiI9013 HDMI Receiver.
11. 48-bit output configuration can also support YCbCr 4:2:2, although 2 pixel/clock 4:2:2 is not useful downstream.
12. DMO YCbCr modes do not output a complete chroma value on one edge, followed by a complete luma value on the opposite edge.
13. Direct 12-bit YCbCr modes output a complete chroma value on one edge, followed by a complete luma value on the opposite edge. Channel swapping is required to perform this data bit mapping to the output pins. Refer to the Programmer's Reference.

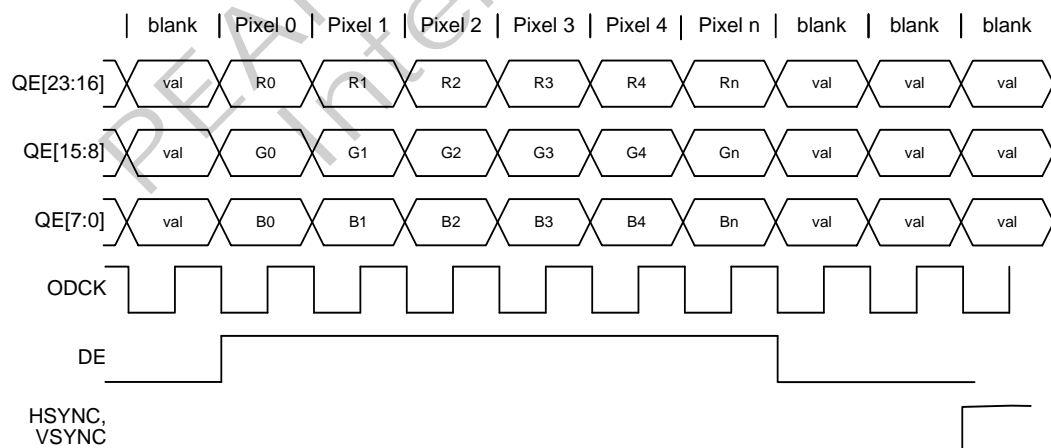
Note: In the figures in this section, the *val* data is defined in various specifications to specific values. These are controlled by setting the appropriate registers in the SiI9013 HDMI Receiver, since no pixel data is carried on HDMI during blanking.

## RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is output on each clock. Figure 22 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 29. When PIXS = 1 (48-bit mode), the even pixels are output on QE[0:23] and the odd pixels are output on QO[23:0].

**Table 29. 4:4:4 Mappings**

Pin Name	Pixel Bit	
	RGB	YCbCr
QE0	B0	Cb0
QE1	B1	Cb1
QE2	B2	Cb2
QE3	B3	Cb3
QE4	B4	Cb4
QE5	B5	Cb5
QE6	B6	Cb6
QE7	B7	Cb7
QE8	G0	Y0
QE9	G1	Y1
QE10	G2	Y2
QE11	G3	Y3
QE12	G4	Y4
QE13	G5	Y5
QE14	G6	Y6
QE15	G7	Y7
QE16	R0	Cr0
QE17	R1	Cr1
QE18	R2	Cr2
QE19	R3	Cr3
QE20	R4	Cr4
QE21	R5	Cr5
QE22	R6	Cr6
QE23	R7	Cr7
HSYNC		
VSYNC		
DE		



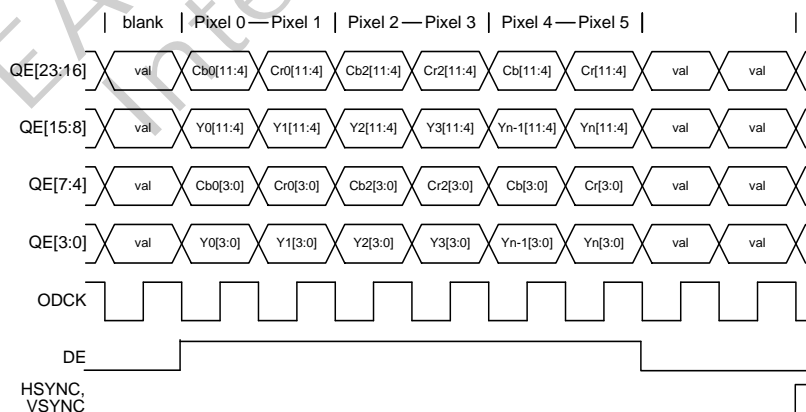
**Figure 25. 4:4:4 Timing Diagram**

## YC 4:2:2 Formats with Separate Syncs

The YC 4:2:2 formats output one pixel for every pixel clock period. A luma (Y) value is output for every pixel, but the chroma values (Cb and Cr) are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output explicitly on their own pins. The DE HIGH time must contain an even number of pixel clocks. Figure 26 shows timings with OCLKDIV = 0 and OCKINV = 1.

**Table 30. YC 4:2:2 non-Encoded-Sync Pin Mappings**

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
QE0	NC	NC	NC	NC	Y0	Y0
QE1	NC	NC	NC	NC	Y1	Y1
QE2	NC	NC	Y0	Y0	Y2	Y2
QE3	NC	NC	Y1	Y1	Y3	Y3
QE4	NC	NC	NC	NC	Cb0	Cr0
QE5	NC	NC	NC	NC	Cb1	Cr1
QE6	NC	NC	Cb0	Cr0	Cb2	Cr2
QE7	NC	NC	Cb1	Cr1	Cb3	Cr3
QE8	Y0	Y0	Y2	Y2	Y4	Y4
QE9	Y1	Y1	Y3	Y3	Y5	Y5
QE10	Y2	Y2	Y4	Y4	Y6	Y6
QE11	Y3	Y3	Y5	Y5	Y7	Y7
QE12	Y4	Y4	Y6	Y6	Y8	Y8
QE13	Y5	Y5	Y7	Y7	Y9	Y9
QE14	Y6	Y6	Y8	Y8	Y10	Y10
QE15	Y7	Y7	Y9	Y9	Y11	Y11
QE16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
QE17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
QE18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
QE19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
QE20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
QE21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
QE22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
QE23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE



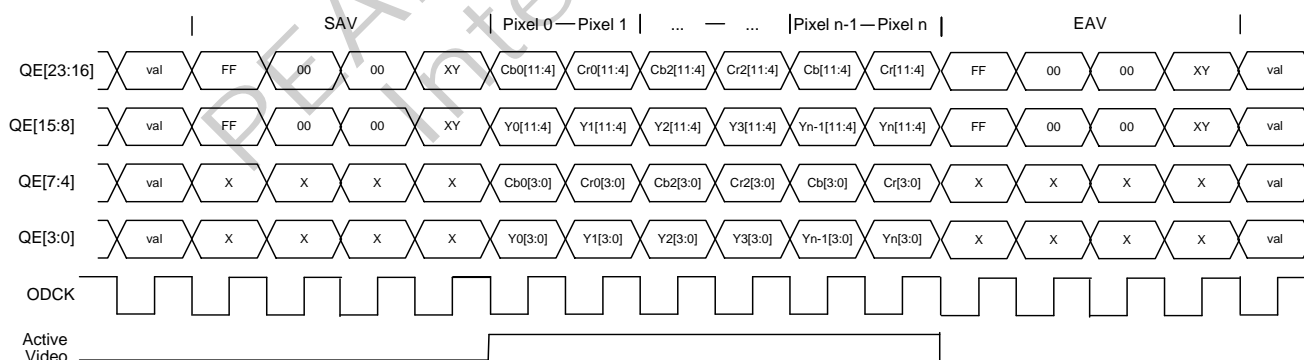
**Figure 26. YC Timing Diagram**

## YC 4:2:2 Formats with Embedded Syncs

The YC 4:2:2 embedded sync format is identical to the previous format (YC 4:2:2), except that the syncs are embedded and not explicit. Pixel data can be 24-bit, 20-bit or 16-bit. DE is always output. Figure 27 shows the start of active video (SAV) preamble, the end of active video (EAV) suffix, and shows timings with OCLKDIV = 0 and OCKINV = 1.

**Table 31. YC 4:2:2 Embedded Sync Pin Mappings**

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
QE0	NC	NC	NC	NC	Y0	Y0
QE1	NC	NC	NC	NC	Y1	Y1
QE2	NC	NC	Y0	Y0	Y2	Y2
QE3	NC	NC	Y1	Y1	Y3	Y3
QE4	NC	NC	NC	NC	Cb0	Cr0
QE5	NC	NC	NC	NC	Cb1	Cr1
QE6	NC	NC	Cb0	Cr0	Cb2	Cr2
QE7	NC	NC	Cb1	Cr1	Cb3	Cr3
QE8	Y0	Y0	Y2	Y2	Y4	Y4
QE9	Y1	Y1	Y3	Y3	Y5	Y5
QE10	Y2	Y2	Y4	Y4	Y6	Y6
QE11	Y3	Y3	Y5	Y5	Y7	Y7
QE12	Y4	Y4	Y6	Y6	Y8	Y8
QE13	Y5	Y5	Y7	Y7	Y9	Y9
QE14	Y6	Y6	Y8	Y8	Y10	Y10
QE15	Y7	Y7	Y9	Y9	Y11	Y11
QE16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
QE17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
QE18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
QE19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
QE20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
QE21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
QE22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
QE23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	NC	NC	NC	NC	NC	NC
VSYNC	NC	NC	NC	NC	NC	NC
DE	NC	NC	NC	NC	NC	NC



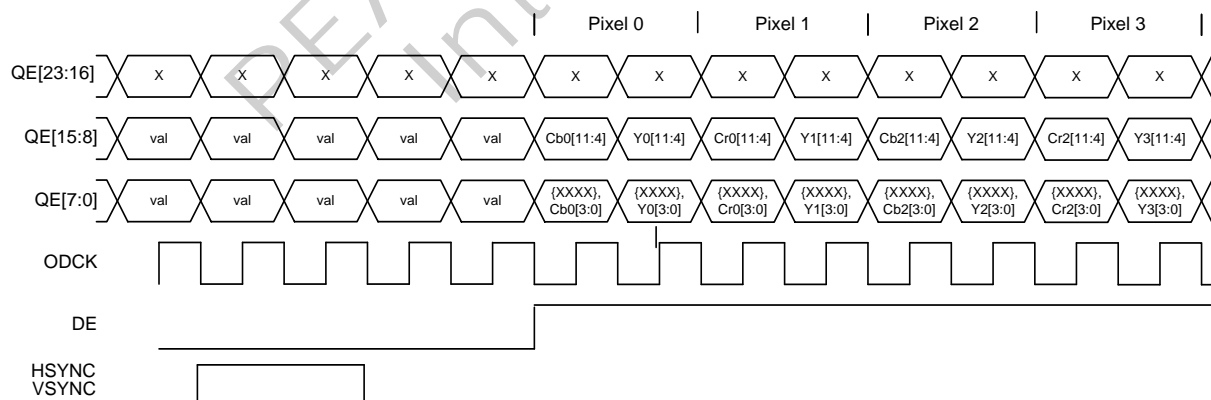
**Figure 27. YC 4:2:2 Embedded Sync Timing Diagram**

## YC Mux (4:2:2) Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping shown in Table 32, but complete luma (Y) and chroma (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. *This mode is only allowed when the differential clock frequency received over the HDMI link is twice the pixel rate.* Figure 28 shows the 24-bit mode. The 16- and 20-bit mappings use fewer output pins for the pixel data. Note the explicit syncs. Figure 28 shows OCLKDIV = 0 and OCKINV = 1.

**Table 32. YC Mux 4:2:2 Mappings**

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
QE0	NC	NC	D0
QE1	NC	NC	D1
QE2	NC	D0	D2
QE3	NC	D1	D3
QE4	NC	NC	NC
QE5	NC	NC	NC
QE6	NC	NC	NC
QE7	NC	NC	NC
QE8	D0	D2	D4
QE9	D1	D3	D5
QE10	D2	D4	D6
QE11	D3	D5	D7
QE12	D4	D6	D8
QE13	D5	D7	D9
QE14	D6	D8	D10
QE15	D7	D9	D11
QE16	NC	NC	NC
QE17	NC	NC	NC
QE18	NC	NC	NC
QE19	NC	NC	NC
QE20	NC	NC	NC
QE21	NC	NC	NC
QE22	NC	NC	NC
QE23	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE



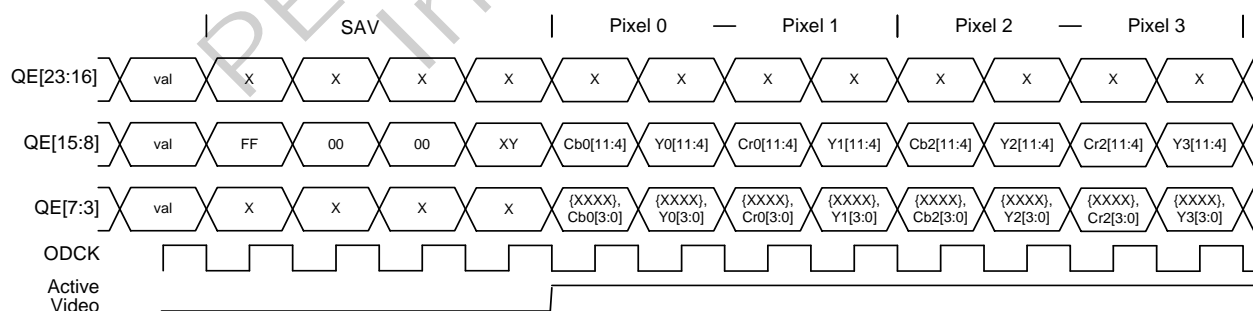
**Figure 28. YC Mux 4:2:2 Timing Diagram**

## YC Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to that on page 36, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luma (Y) and chroma (Cb and Cr) onto the same pins on alternating pixel clock cycles. *This mode is valid only when 2x pixel replication is active as indicated in the AVI packet.* Normally this mode is used only for 480i, 480p, 576i, and 576p modes. The output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows fall of DE. See the ITU-R BT656 Specification. 480p, 54 MHz output can be achieved if the input differential clock is 54 MHz. Figure 29 shows OCLKDIV = 0 and OCKINV = 1.

**Table 33. YC Mux 4:2:2 Embedded Sync Pin Mapping**

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
QE0	NC	D0	D0
QE1	NC	D1	D1
QE2	NC	NC	D2
QE3	NC	NC	D3
QE4	NC	NC	NC
QE5	NC	NC	NC
QE6	NC	NC	NC
QE7	NC	NC	NC
QE8	D0	D2	D4
QE9	D1	D3	D5
QE10	D2	D4	D6
QE11	D3	D5	D7
QE12	D4	D6	D8
QE13	D5	D7	D9
QE14	D6	D8	D10
QE15	D7	D9	D11
QE16	NC	NC	NC
QE17	NC	NC	NC
QE18	NC	NC	NC
QE19	NC	NC	NC
QE20	NC	NC	NC
QE21	NC	NC	NC
QE22	NC	NC	NC
QE23	NC	NC	NC
HSYNC	NC	NC	NC
VSYNC	NC	NC	NC
DE	NC	NC	NC



**Figure 29. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram**

## 48-Bit Output Mode

In 48-bit SDR output mode (PIXS = 1), the first active (even) pixel on each line is output on QE[23:0] and the second (odd pixel) is output on QO[23:0]. Figure 30 shows an example of the timing diagram for RGB 4:4:4 in 48-bit mode. The same timing format will be true with YCbCr 4:4:4 mode, with the even pixel output on QE[23:0] while the odd pixels output on QO[23:0]. When outputting fewer than 8 bits per channel, the unused bits are as shown on pages 33–34. 48-bit mode is not useful when outputting embedded syncs or in YC Mux mode.

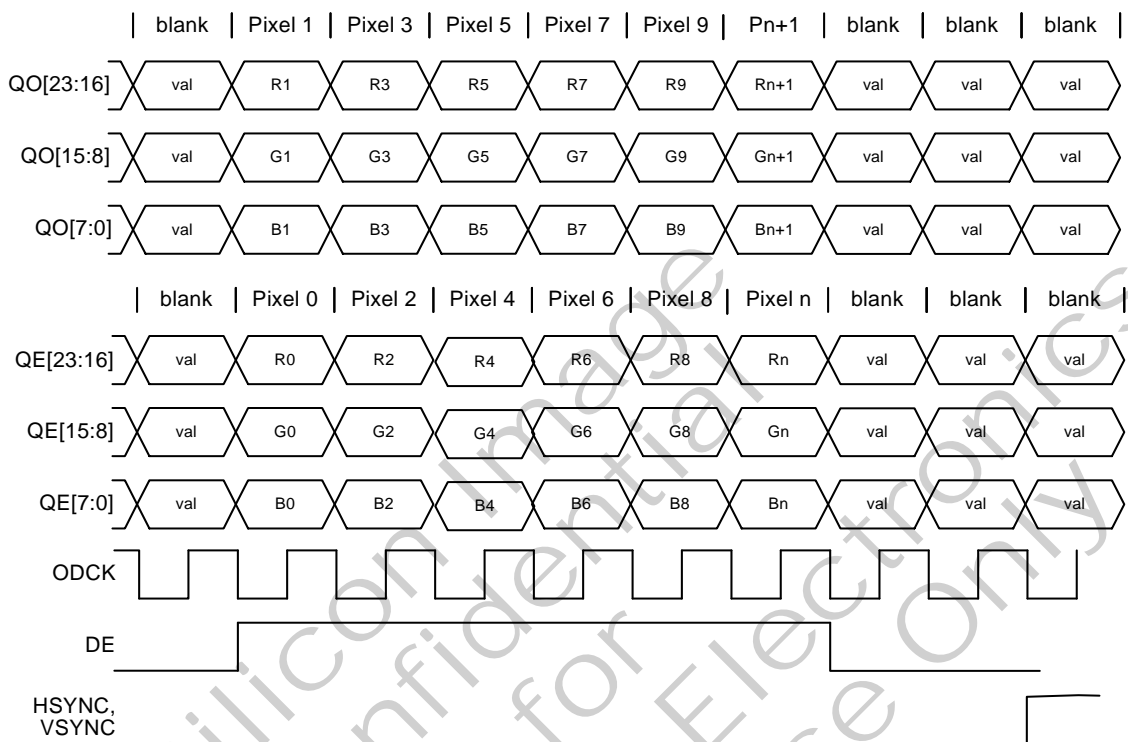


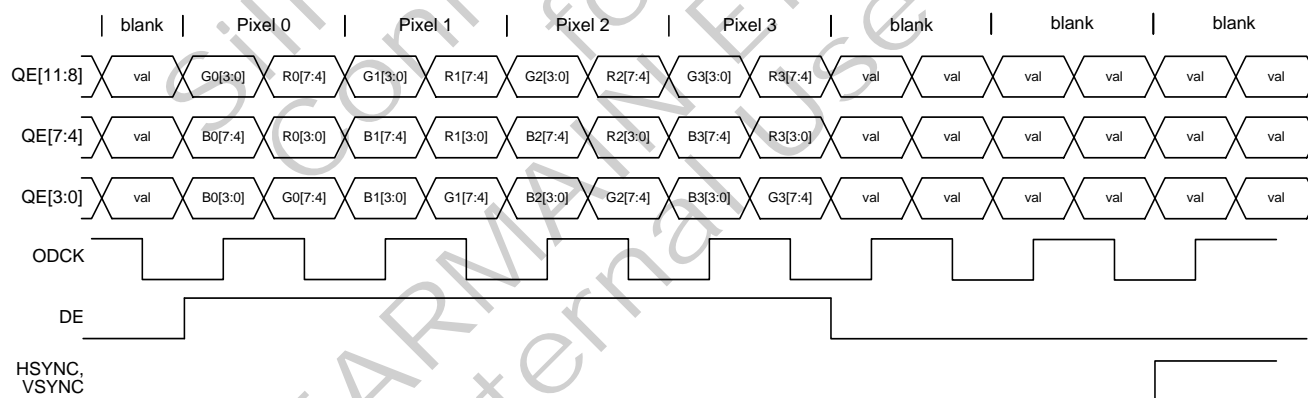
Figure 30. 48-Bit 4:4:4 Timing Diagram

## 12-Bit DDR RGB 4:4:4 and YCbCr 4:4:4 Formats with Separate Syncs

The output clock runs at the pixel rate and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12 pins. Figure 31 shows RGB data. The same timing format is used for YCbCr 4:4:4, as listed in columns four and five of Table 34. Control signals (DE, HSYNC, and VSYNC) change state with respect to the *first* edge of ODCK.

**Table 34. 12-Bit DDR Output 4:4:4 Mappings**

Pin Name	24-bit RGB		24-bit YCbCr	
	First Edge	Second Edge	First Edge	Second Edge
QE0	B0	G4	Cb0	Y4
QE1	B1	G5	Cb1	Y5
QE2	B2	G6	Cb2	Y6
QE3	B3	G7	Cb3	Y7
QE4	B4	R0	Cb4	Cr0
QE5	B5	R1	Cb5	Cr1
QE6	B6	R2	Cb6	Cr2
QE7	B7	R3	Cb7	Cr3
QE8	G0	R4	Y0	Cr4
QE9	G1	R5	Y1	Cr5
QE10	G2	R6	Y2	Cr6
QE11	G3	R7	Y3	Cr7
HSYNC	HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC	
DE	DE		DE	



**Figure 31. 12-Bit DDR Output 4:4:4 Timing Diagram**

## I<sup>2</sup>C Interfaces

### HDCP E-DDC / I<sup>2</sup>C Interface

The HDCP protocol requires values to be exchanged between the video transmitter and video receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I<sup>2</sup>C serial protocol. In an SiI9013 HDMI Receiver design, the SiI9013 HDMI Receiver is the video receiver and will have a connection to the E-DDC bus with a slave address of 0x74. The I<sup>2</sup>C read operation is shown in Figure 32, and the write operation in Figure 33.

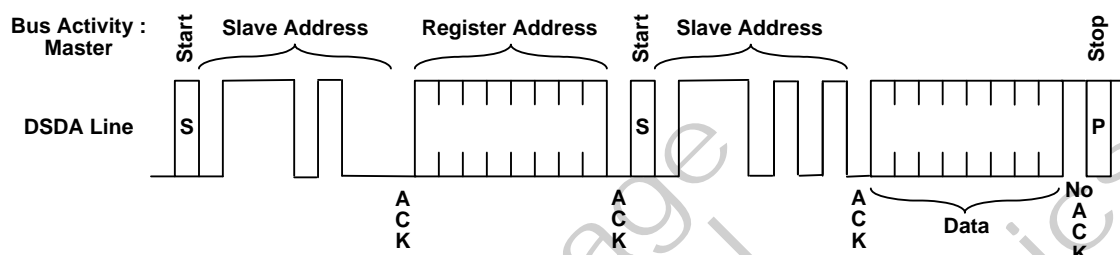


Figure 32. I<sup>2</sup>C Byte Read

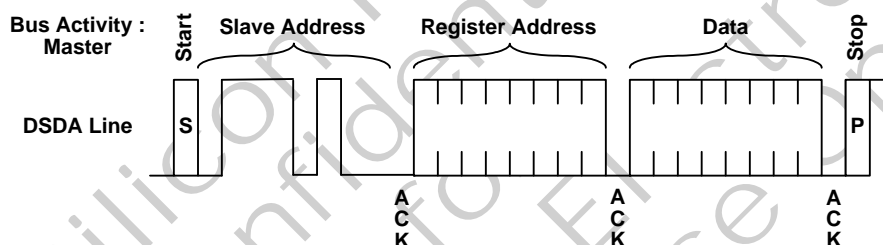


Figure 33. I<sup>2</sup>C Byte Write

Multiple bytes may be transferred in each transaction, regardless of whether a read or a write. The operations will be similar to those in Figure 32 and Figure 33 except that there will be more than one data phase. An ACK follows each byte, except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I<sup>2</sup>C specification for more information.

There is also a Short Read format, designed to improve the efficiency of R<sub>i</sub> register reads (which must be done every two seconds while encryption is enabled). This transaction is shown in Figure 34. Note that there is no register address phase (only the slave address phase), since the register address is reset to 0x08 (R<sub>i</sub>) after a hardware or software reset, and after the STOP condition on any preceding I<sup>2</sup>C transaction.

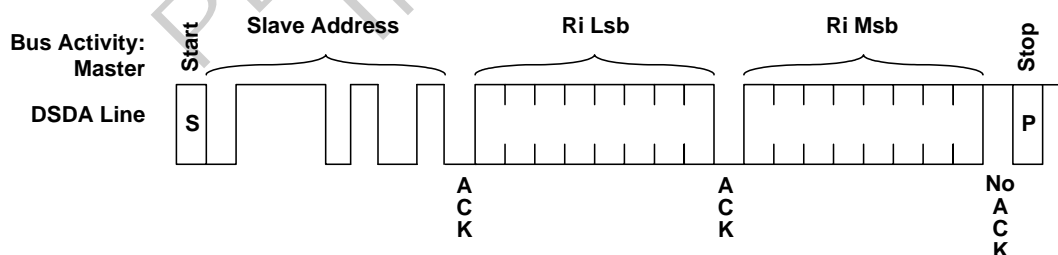


Figure 34. Short Read Sequence

## Local I<sup>2</sup>C Interface

The SiI9013 HDMI Receiver has a second I<sup>2</sup>C port accessible only to the controller in the display device. It is separate from the E-DDC bus. The receiver is a slave device which responds to two seven-bit binary I<sup>2</sup>C device addresses, which are selected with the CI2CA pin (see page 10). Two device addresses are used to accommodate the long list of registers in the SiI9013 HDMI Receiver, since I<sup>2</sup>C can access only 256 registers at any one device address. This I<sup>2</sup>C interface only supports the read operation in Figure 32 and the write operation in Figure 33. It does not support the short read operation shown in Figure 34.

**Note:** The Slave Address fields shown in Figure 32 through Figure 34 are shown for the DDC port (address 0x74) and will be different on the local I<sup>2</sup>C port. Also, the I<sup>2</sup>C data pin for the local I<sup>2</sup>C bus is CSDA, instead of the DSDA pin shown in these figures.

## Video Requirement for I<sup>2</sup>C Access

The SiI9013 HDMI Receiver does not require an active video clock to access its registers from either the E-DDC port or the local I<sup>2</sup>C port. Read-Write registers may be written and then read back. Read-only registers, which provide values for an active video or audio stream, will return indeterminate values if there is no video clock and no active syncs.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

## HDCP Registers

The register values which are exchanged over the DVI DDC I<sup>2</sup>C serial interface with the SiI9013 HDMI Receiver for HDCP are described in the HDCP 1.1 Specification in Section 2.6 – HDCP Port. Refer to the *SiI9013 HDMI Receiver Programmer's Reference* (SiI-PR-1012) for details on these and all other SiI9013 HDMI Receiver registers.

## Design Recommendations

The following information is provided as recommendations. If you choose to deviate from these recommendations for a particular application, Silicon Image recommends that you contact your Silicon Image technical representative for an evaluation of the change.

## Power Control

The low-power standby state feature of the SiI9013 HDMI Receiver provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD# register bit to put it in a lower power state may result in faster system response time, depending on the system Vcc supply ramp-up delay.

## Power Pin Current Demands

The limits shown in Table 35 indicate the current demanded by each group of power pins on the SiI9013 HDMI Receiver. These limits were characterized at VCC +10%, room temperature, and for Fast-Fast silicon. Actual application current demands will be lower than these figures, and will vary with video resolution and audio clock frequency.

Table 35. Maximum Power Domain Currents versus Video Mode

Mode	IDCK (MHz)	3.3V Power Domain Currents (mA)					1.8V Power Domain Currents (mA)		
		AVCC	IOVCC	PVCC	REGVCC	XTALVCC	CVCC18	DVCC18	AUDPVCC18
480p	27.0	141	17	1	6	8	57	8	0.1
1080i	74.25	156	56	2	6	8	141	20	0.1
SXGA	108.0	168	66	2	6	8	193	28	0.1
1080p	148.5	182	112	3	6	8	259	39	0.1
UXGA60	162	187	105	3	6	8	272	40	0.1

### Notes:

1. Measured with 192 kHz, 8-channel audio, and MCLK = 49.152 MHz. 480p mode measured with 48 kHz, 8-channel audio, and MCLK = 24.576 MHz.
2. Measured with 24-bit SDR RGB input and 24-bit SDR RGB output, Fine Dot Moire (1 pixel on/off) pattern.

## Crystal Clock Source Requirement

Whether through an external crystal or a LVTTTL clock, a clock source must always be available to drive the SiI9013 receiver. For typical applications, a 28.332 MHz crystal should be connected between the XTALIN and XTALOUT pins to provide the reference clock for the audio PLL and the clock to control of the internal audio pipeline. This reference clock is also used for the internal reading of the HDCP keys. Therefore, for designs not supporting audio, a clock must always be present to support the non-audio functions.

For designs which do not otherwise support audio, the XTALIN pin can be connected to an ordinary LVTTTL clock source at 27 MHz, commonly available on HDMI sink designs. There is no requirement that this clock source be low jitter. The XTALOUT pin should be left unconnected when XTALIN is driven with a LVTTTL clock. Figure 41 shows the recommended connections.

## Receiver DDC Bus Protection

VESA DDC Specification (available at <http://www.vesa.org>) defines the DDC interconnect bus to be a 5 V signaling path. The I<sup>2</sup>C pins on the SiI9013 chip are 5 V tolerant, but they are not true open-drain I/O. If IOVCC is removed from the device, there will be a leakage path through the I<sup>2</sup>C pins. Therefore, board designers should use a power isolation circuit between the DDC pins in the connector and the DDC pin on the SiI9013 receiver. The pull-up resistors on the DDC bus should be pulled up using the 5 V supply from the HDMI connector. Figure 38 on page 46 shows this circuit.

## PWR5V Input

Although the PWR5V pin of the SiI9013 receiver is 5 V tolerant, power isolation circuitry similar to the one described above is recommended for the PWR5V pin as well. Adding this circuit between the HDMI connector +5 V pin and the PWR5V pin is primarily to prevent any leakage path whenever the power to the device is off while the +5 V power from the connector is on. Refer to [Figure 38](#) on page 46 for an example.

## Voltage Ripple Regulation

Excessive noise on PVCC can cause problems for the PLL as it tries to stay locked on the incoming video clock. To ensure error-free operation, the voltage level on the PVCC pins must not exceed the voltage level on the AVCC pins by more than 50 mV. [Figure 37](#) on page 45 shows a schematic with the recommendation on how to connect and filter the PVCC pins from the AVCC pins.

For applications above 135 MHz, a tighter tolerance (+3.3 V –5%/+10%) is recommended for both AVCC and PVCC power supplies to ensure optimum performance at the higher-speed modes.

## Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in [Figure 37](#). Place these components as close as possible to the SiI9013 device pins, and avoid routing traces through vias, as shown in [Figure 35](#), which is representative of the various types of power pins on the receiver.

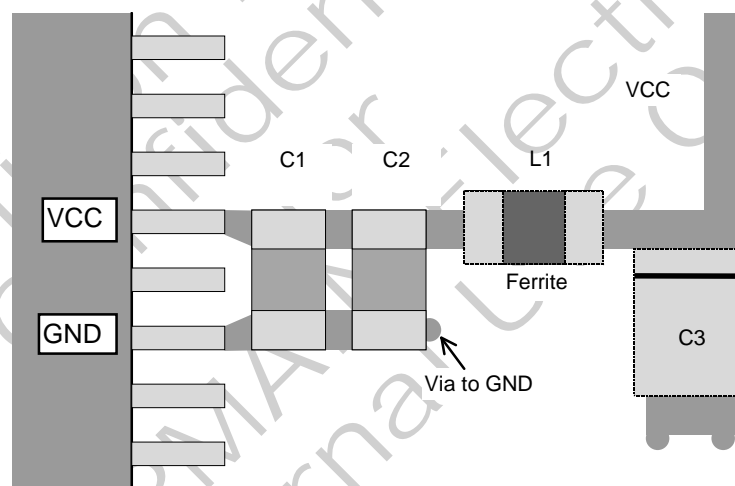
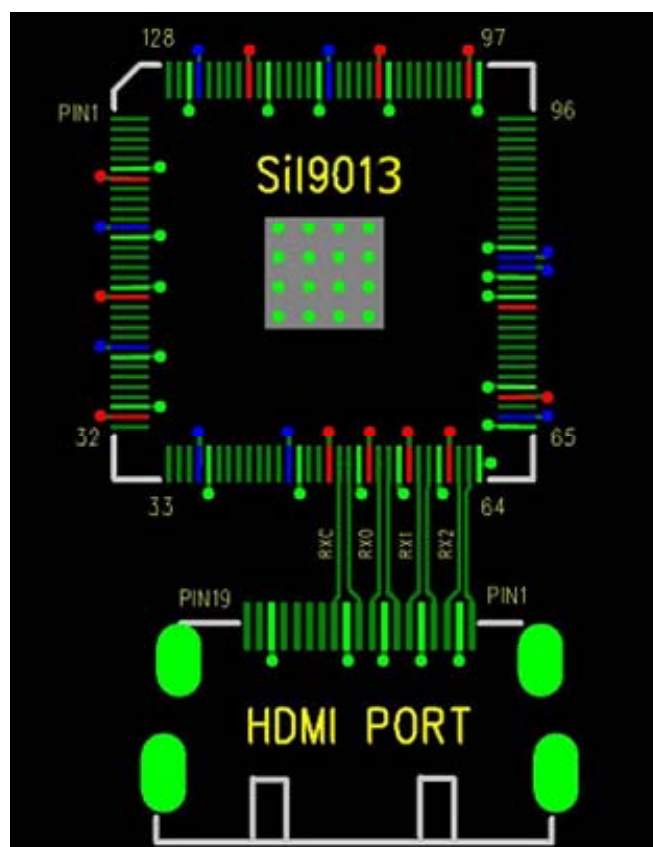


Figure 35. Decoupling and Bypass Capacitor Placement

## Receiver Layout

The receiver chip should be placed as closely as possible to the input connectors that carry the TMDS signals. The differential lines should be routed as directly as possible from connector to receiver. The SiI9013 device is tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, and the number of vias through which the signal lines are routed should be minimized. The distance separating the two traces of the differential pair should be kept to a minimum.



**Figure 36. HDMI to Receiver Routing – Top View**

Note the eight TMDS traces connected directly from the HDMI connectors (bottom) to the pins on the SiI9013 HDMI Receiver (top). Trace impedance should be 100 ohms differential in each pair, and 50 ohm single-ended if possible. Trace width and pitch will depend on the PCB construction. Not all connections are shown; the figure demonstrates routing of TMDS lines without crossovers, vias, EMI, or ESD protection. See also [Figure 43](#) and [Figure 44](#).

## ESD Protection

The receiver chip is designed to withstand electrostatic discharge to 2 kV. In applications where higher protection levels are required, ESD limiting components can be placed on the differential lines coming into the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use of the lowest capacitance devices is suggested, and in no case should the capacitance value exceed 5 pF.

The components on the TMDS lines shown in [Figure 38](#) on page 46 were qualified for the HDMI compliance test. However, no ESD testing was conducted to characterize the performance of these components. These components may be considered as a starting point in the system design, but characterization for ESD performance of these components is recommended and must be evaluated on a system-by-system basis prior to finalizing the design.

## EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines (aside from any essential ESD protection as described earlier). The differential signaling used in HDMI is inherently low in EMI as long as the routing recommendations noted in the [Receiver Layout](#) section are followed.

The PCB ground plane should extend unbroken under as much of the receiver chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

## Thermal and Electrical Benefits of Exposed Pads

The SiI9013 receiver is available in a 128-pin LQFP thermally enhanced package. The package comes with an ExposedPad™ at the bottom, providing the primary heat removal path in addition to excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional LQFP package, but the exposed pad must be attached to the PCB ground to remove the maximum amount of heat from the package, as well as to ensure the best electrical performance. Whenever possible, therefore, Silicon Image recommends using the exposed pad in all SiI9013 designs, particularly in applications with video modes operating above 74.25 MHz.

For guidelines in designing with exposed pads, please refer to the Silicon Image application note *Designing with Exposed Pads* (SiI-AN-0129) for more information.

## Typical Circuits

Representative circuits for application of the SiI9013 receiver chip are shown in Figure 37 through Figure 42. For a detailed review of your intended circuit implementation, contact your Silicon Image representative.

### Power Supply Decoupling

The ferrite on PVCC should have an impedance of 10 ohms or more in the frequency range 1–2 MHz. An example device (surface mount, 0805 package) is part number MLF2012A4R7K from TDK. A data sheet is available at [http://www.tdk.co.jp/tefe02/e511\\_MLF2012.pdf](http://www.tdk.co.jp/tefe02/e511_MLF2012.pdf)

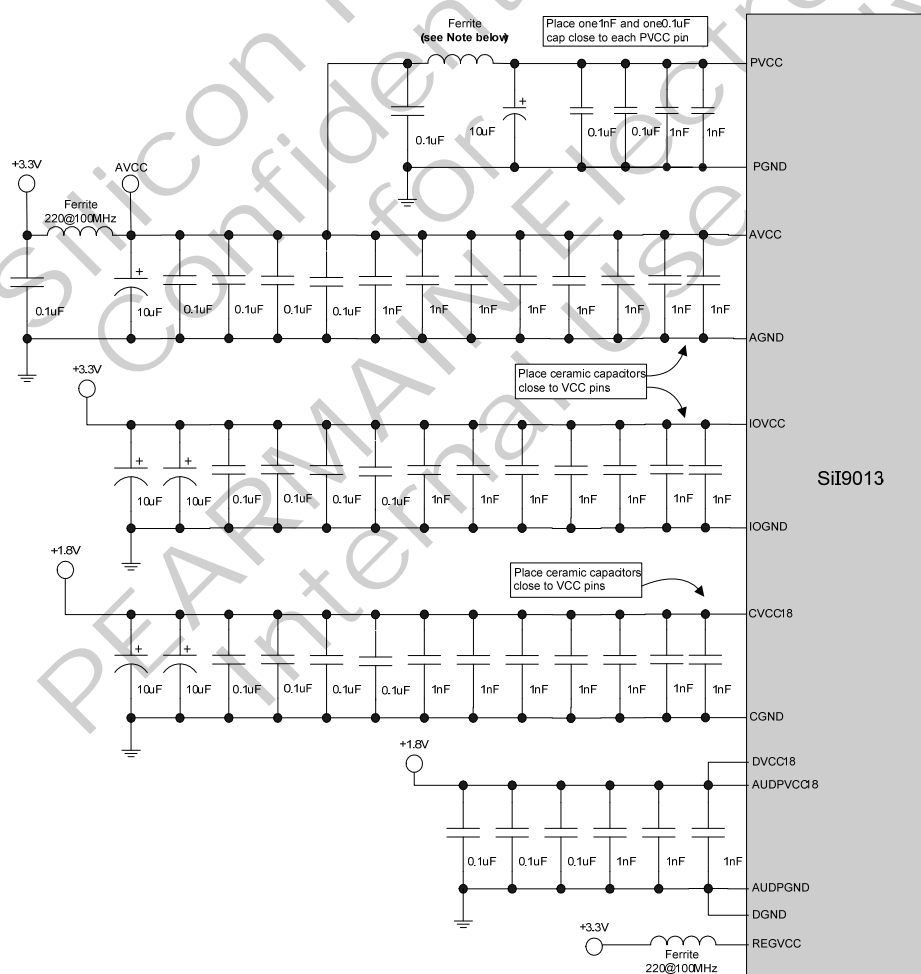


Figure 37. Power Supply Decoupling and PLL Filtering Schematic

## HDMI Port TMDs Connections

Common mode chokes combined with ESD protection components can be used to improve the ESD protection and EMI performance of the HDMI interface. Varistors from vendors such as TDK, CMD, and Semtech can be used in place of the ESD protection. When designing with these components, considerations must be taken to make sure the input impedance of the HDMI receiver is maintained and kept well within the compliant limits. The performance of these components must also be characterized and evaluated on a system-by-system basis.

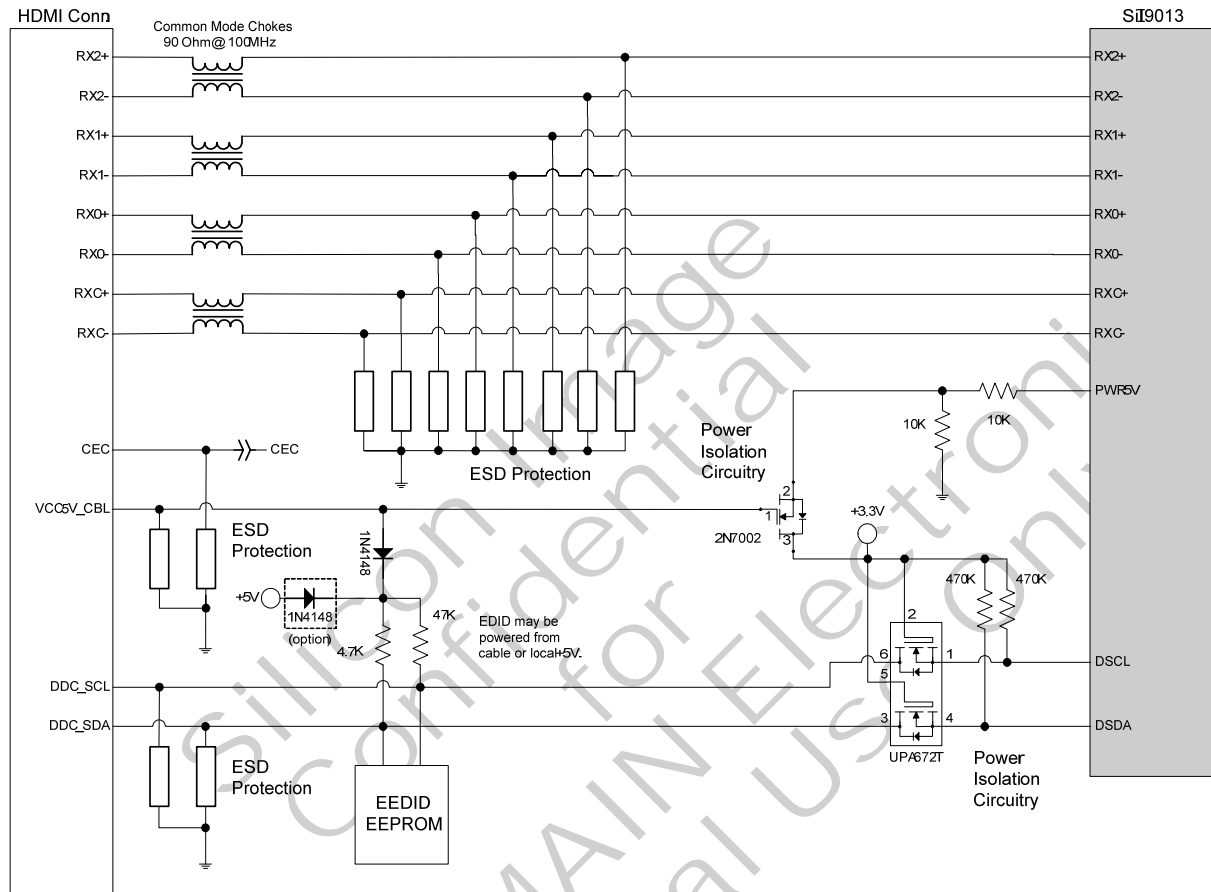


Figure 38. HDMI Port Connections Schematic

## Digital Video Output Connections

The series termination shown for QE[23:0] should be repeated for QO[23:0] if QO[23:0] are used. These resistors should be placed close to the chip.

The receiver INT output may be connected as an interrupt to the microcontroller, or the microcontroller can poll register 0x70 (INTR\_STATE) to determine if any of the enabled interrupts have occurred. Refer to the *SiI9013 HDMI Receiver Programmers' Reference* (SiI-PR-1012) for details. The receiver VSYNC output may be connected to the microcontroller if it is necessary to monitor the vertical refresh rate of the incoming video.

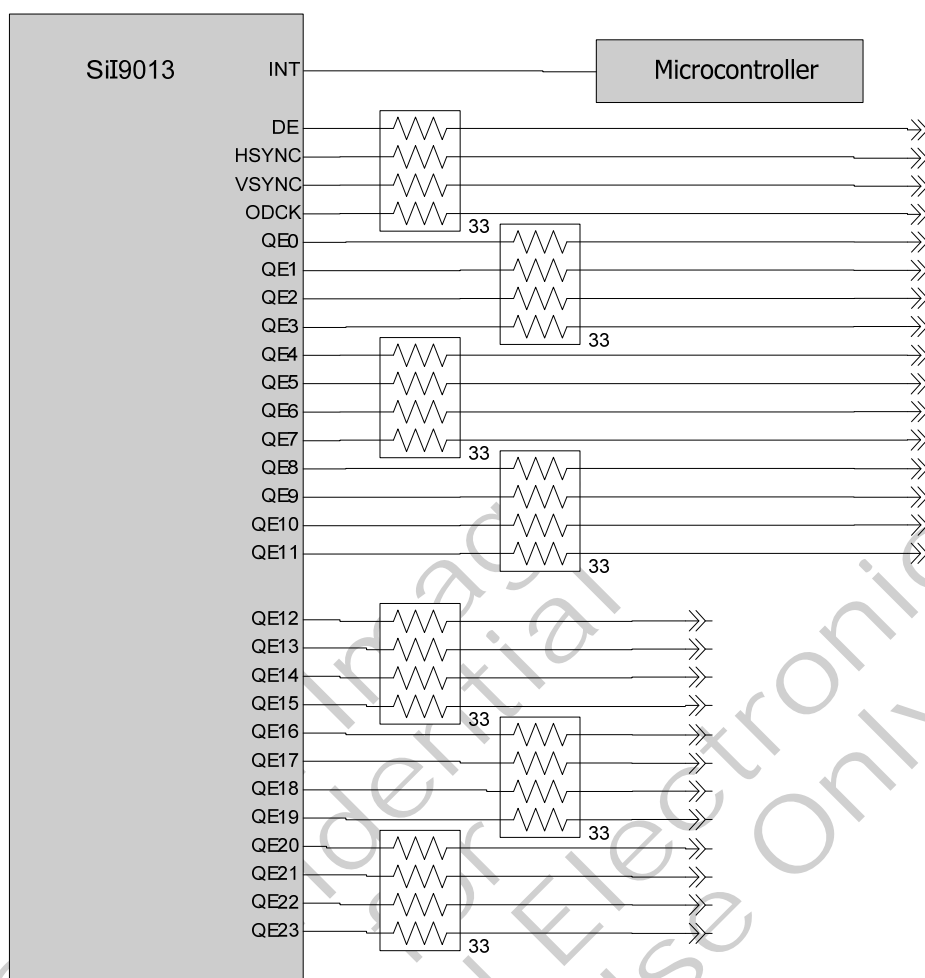


Figure 39. Digital Display Schematic

## Digital Audio Output Connections

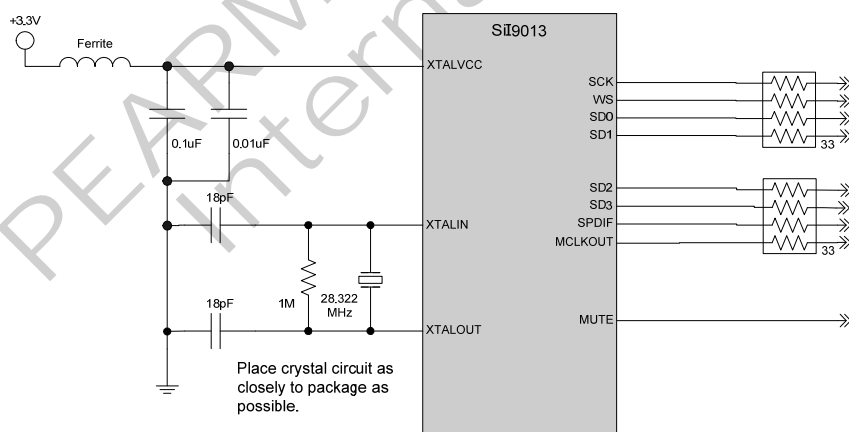


Figure 40. Audio Output Schematic

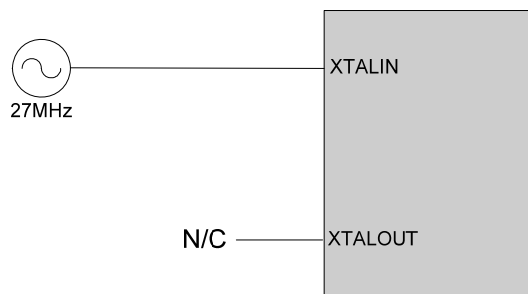


Figure 41. XTALIN Connection with External Clock Source

## Control Signal Connections

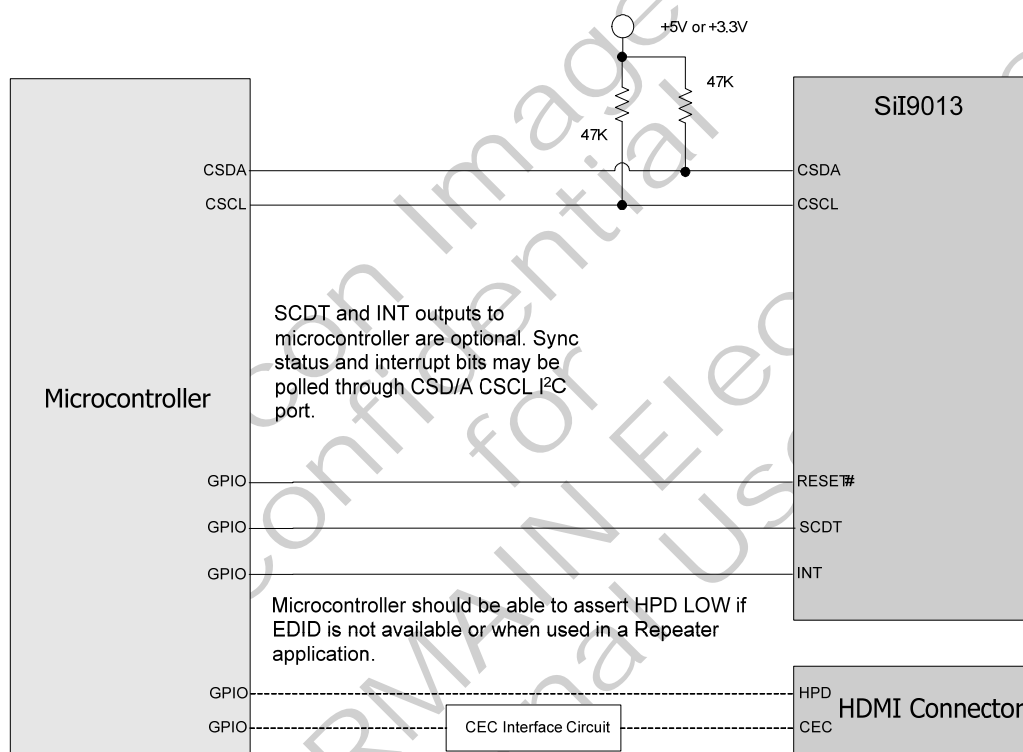


Figure 42. Controller Connections Schematic

## Layout

Figure 43 and Figure 44 on the next page show examples of routing TMDS lines between the SiI9013 HDMI Receiver and the HDMI connector.

## TMDS Input Port Connections

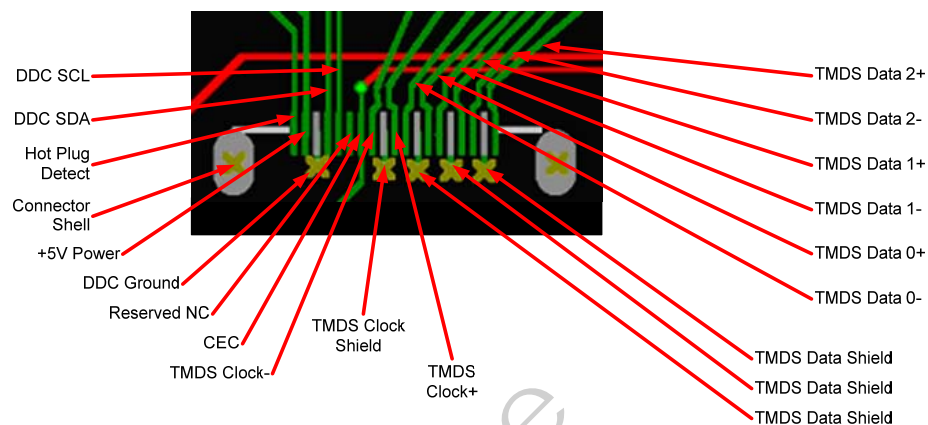


Figure 43. TMDS Input Signal Assignments

## Routing with ESD Devices

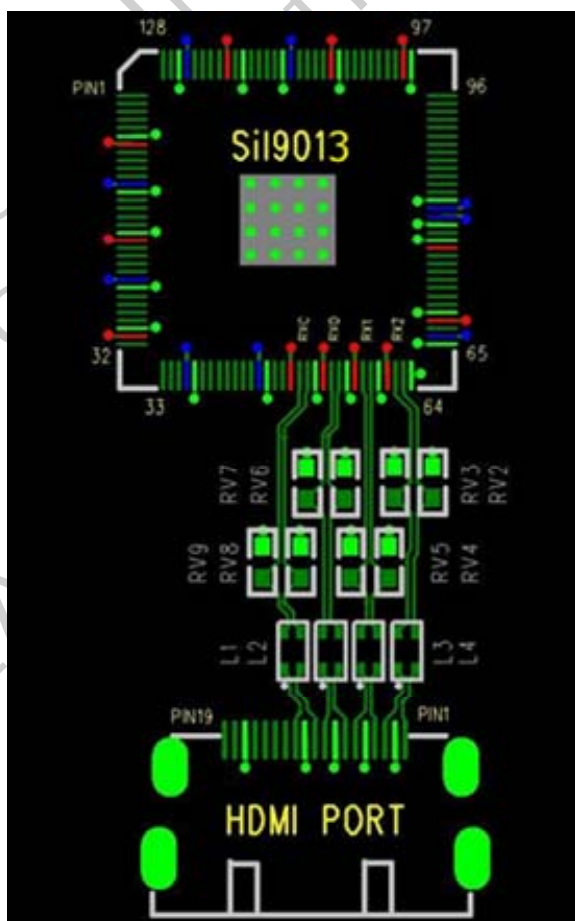


Figure 44. TMDS Input Layout through ESD Devices

# Packaging

## Package Dimensions

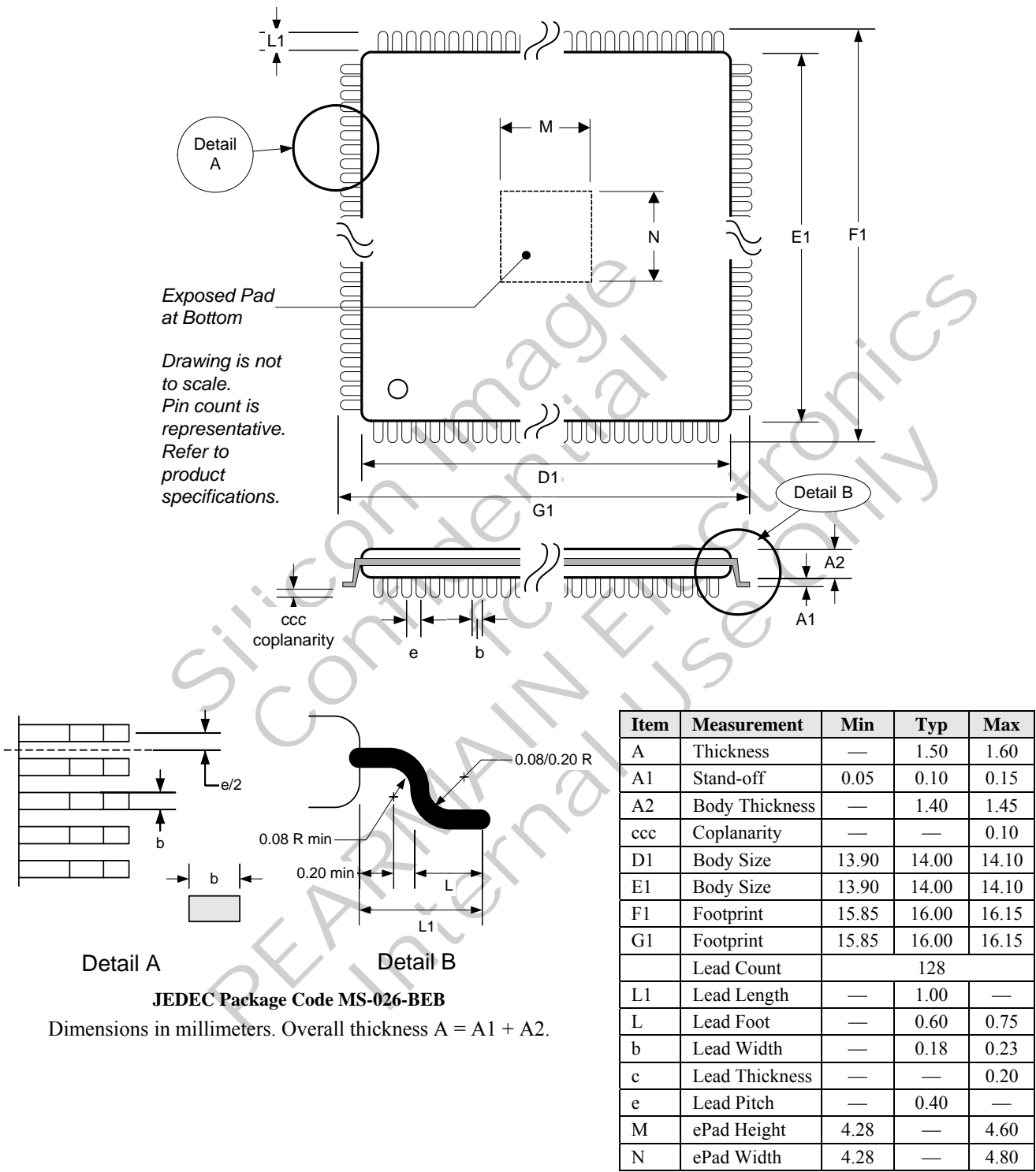
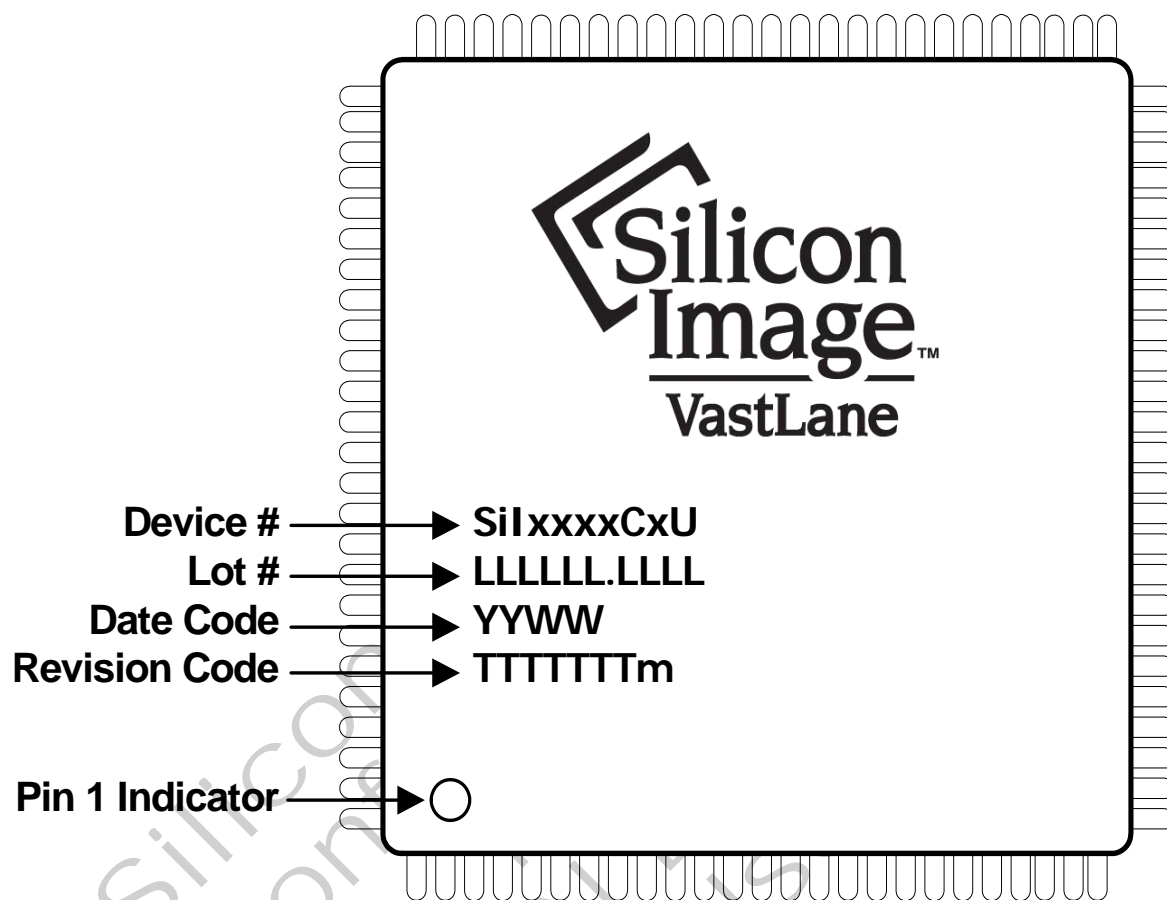


Figure 45. Package Diagram

## Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to specifics in [Figure 45](#) on page 50.



### Notes:

1. The universal package may be used in lead-free and standard reflow process lines.
2. Only production HDCP key versions are available.

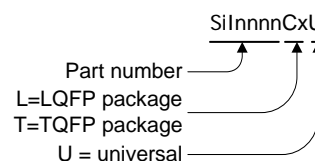


Figure 46. Marking Diagram

## Ordering Information

Production Part Numbers: SiI9013CLU

LQFP-128 Package

## References

### Standards Documents

Table 36 lists the abbreviations used in this document. Contact the responsible standards groups listed in Table 37 for more information on these specifications.

**Table 36. Referenced Documents**

Abbreviation	Standards publication, organization, and date
HDMI	<i>High Definition Multimedia Interface, Revision 1.1</i> , HDMI Consortium, May 2004
HCTS	<i>HDMI Compliance Test Specification, Revision 1.0</i> , HDMI Consortium, July 2003
HDCP	<i>High-bandwidth Digital Content Protection, Revision 1.1</i> , Digital Content Protection, LLC, June 2003
E-EDID	<i>Enhanced Extended Display Identification Data Standard</i> , Release A Revision 1, VESA, Feb. 2000
CEA-861	<i>A DTV Profile for Uncompressed High Speed Digital Interfaces</i> , EIA/CEA, January 2001
CEA-861-B	<i>A DTV Profile for Uncompressed High Speed Digital Interfaces</i> , Draft 020328, EIA/CEA, March 2002
EIAWG7	<i>Recommended Practice for Use of EDID with EIA/CEA-861 et al</i> , EIA Working Group 7, May 2002
EDDC	<i>Enhanced Display Data Channel Standard, Version 1</i> , VESA, September 1999

**Table 37. Standards Groups Contact Information**

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	<a href="http://global.ihs.com">http://global.ihs.com</a>	<a href="mailto:global@ihs.com">global@ihs.com</a>	800-854-7179
VESA	<a href="http://www.vesa.org">http://www.vesa.org</a>	—	408-957-9270
HDCP	<a href="http://www.digital-cp.com">http://www.digital-cp.com</a>	<a href="mailto:info@digital-cp.com">info@digital-cp.com</a>	—
DVI	<a href="http://www.ddwg.org">http://www.ddwg.org</a>	<a href="mailto:ddwg.if@intel.com">ddwg.if@intel.com</a>	—
HDMI	<a href="http://www.hdmi.org">http://www.hdmi.org</a>	<a href="mailto:admin@hdmi.org">admin@hdmi.org</a>	—

### Silicon Image Documents

Table 38 lists Silicon Image documents that are available from your Silicon Image sales representative.

**Table 38. Silicon Image Publications**

Document	Title
SiI-AN-0118	<i>SiI9011/9021/9031 HDMI PanelLink Receivers Application Note</i>
SiI-AN-0129	<i>PCB Layout Guidelines: Designing with Exposed Pads</i>
SiI-PR-1012	<i>SiI9013 HDMI Receiver HDMI Receiver Programmers' Reference</i>

**Disclaimers**

These materials are provided on an “AS IS” basis. Silicon Image, Inc. and its affiliates disclaim all representations and warranties (express, implied, statutory or otherwise), including but not limited to: (i) all implied warranties of merchantability, fitness for a particular purpose, and/or non-infringement of third party rights; (ii) all warranties arising out of course-of-dealing, usage, and/or trade; and (iii) all warranties that the information or results provided in, or that may be obtained from use of, the materials are accurate, reliable, complete, up-to-date, or produce specific outcomes. Silicon Image, Inc. and its affiliates assume no liability or responsibility for any errors or omissions in these materials, makes no commitment or warranty to correct any such errors or omissions or update or keep current the information contained in these materials, and expressly disclaims all direct, indirect, special, incidental, consequential, reliance and punitive damages, including WITHOUT LIMITATION any loss of profits arising out of your access to, use or interpretation of, or actions taken or not taken based on the content of these materials.

Silicon Image, Inc. and its affiliates reserve the right, without notice, to periodically modify the information in these materials, and to add to, delete, and/or change any of this information.

Notwithstanding the foregoing, these materials shall not, in the absence of authorization under U.S. and local law and regulations, as required, be used by or exported or re-exported to (i) any U.S. sanctioned or embargoed country, or to nationals or residents of such countries; or (ii) any person, entity, organization or other party identified on the U.S. Department of Commerce's Denied Persons or Entity List, the U.S. Department of Treasury's Specially Designated Nationals or Blocked Persons List, or the Department of State's Debarred Parties List, as published and revised from time to time; (iii) any party engaged in nuclear, chemical/biological weapons or missile proliferation activities; or (iv) any party for use in the design, development, or production of rocket systems or unmanned air vehicles.

**Products and Services**

The products and services described in these materials, and any other information, services, designs, know-how and/or products provided by Silicon Image, Inc. and/or its affiliates are provided on an “AS IS” basis, except to the extent that Silicon Image, Inc. and/or its affiliates provides an applicable written limited warranty in its standard form license agreements, standard Terms and Conditions of Sale and Service or its other applicable standard form agreements, in which case such limited warranty shall apply and shall govern in lieu of all other warranties (express, statutory, or implied). EXCEPT FOR SUCH LIMITED WARRANTY, SILICON IMAGE, INC. AND ITS AFFILIATES DISCLAIM ALL REPRESENTATIONS AND WARRANTIES (EXPRESS, IMPLIED, STATUTORY OR OTHERWISE), REGARDING THE INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS PROVIDED BY SILICON IMAGE, INC. AND/OR ITS AFFILIATES, INCLUDING BUT NOT LIMITED TO, ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND/OR NON-INFRINGEMENT OF THIRD PARTY RIGHTS. YOU ACKNOWLEDGE AND AGREE THAT SUCH INFORMATION, SERVICES, DESIGNS, KNOW-HOW AND PRODUCTS HAVE NOT BEEN DESIGNED, TESTED, OR MANUFACTURED FOR USE OR RESALE IN SYSTEMS WHERE THE FAILURE, MALFUNCTION, OR ANY INACCURACY OF THESE ITEMS CARRIES A RISK OF DEATH OR SERIOUS BODILY INJURY, INCLUDING, BUT NOT LIMITED TO, USE IN NUCLEAR FACILITIES, AIRCRAFT NAVIGATION OR COMMUNICATION, EMERGENCY SYSTEMS, OR OTHER SYSTEMS WITH A SIMILAR DEGREE OF POTENTIAL HAZARD. NO PERSON IS AUTHORIZED TO MAKE ANY OTHER WARRANTY OR REPRESENTATION CONCERNING THE PERFORMANCE OF THE INFORMATION, PRODUCTS, KNOW-HOW, DESIGNS OR SERVICES OTHER THAN AS PROVIDED IN THESE TERMS AND CONDITIONS.



1060 E. Arques Avenue  
Sunnyvale, CA 94085  
T 408.616.4000 F 408.830.9530  
[www.siliconimage.com/](http://www.siliconimage.com/)

Silicon Image  
Confidential  
PEARMAIN for  
Internal Use Only



1060 E. Arques Avenue  
Sunnyvale, CA 94085  
T 408.616.4000 F 408.830.9530  
[www.siliconimage.com/](http://www.siliconimage.com/)