

January 2004

## Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST™ CPLD solution. The ispMACH 4000 family includes 3.3V, 2.5V and 1.8V power supply versions, designated the ispMACH 4000V, 4000B, 4000C and 4000Z (1.8V, zero power) devices, respectively. The ispMACH 4000C is the industry's first 1.8V In-System Programmable (ISP™) CPLD family. The ispMACH 4000 devices couple industry leading speed performance with the lowest static and dynamic power consumption available, while supporting I/O standards between 3.3 and 1.8 volts.

The ispMACH 4000 family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with zero/low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch BGA (fpBGA) packages ranging from 44 to 256 pins/balls. Tables 1 and 2 show the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C and 4000Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment.

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E<sup>2</sup> low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any "turbo bits" or other power management schemes associated with a traditional sense-amplifier approach. The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry's lowest static power.

The ispMACH 4000V and 4000Z families supports the full automotive temperature range of -40 to 125°C Ambient (Specified as a junction temperature range of -40 to 130°C). The 3.3V ispMACH 4000V supports a wide range of 3.3V, 2.5V and 1.8V I/O standards and features 5V tolerant I/Os when using the LVCMOS 3.3, LVTTTL and PCI interfaces. This high-performance family is well suited for the full range of automotive applications including "in-cabin" electronics and telematics (cell phones, navigation, radio, networking and PC) as well as harsher "under-the-hood" applications such as engine and power train control systems management. The ispMACH 4000V automotive temperature grade family provides logic density solutions from 32 to 256 macrocells, the broadest automotive CPLD product offering in the industry. Lattice supports multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 176 pins.

## Features

### ■ High Performance

- $f_{MAX}$  = 400MHz maximum operating frequency
- $t_{PD}$  = 2.5ns propagation delay
- Up to four global clock pins with programmable clock polarity control
- Up to 80 PTs per output

### ■ Ease of Design

- Superior solution for power sensitive consumer applications
- Enhanced macrocells with individual clock, reset, preset and clock enable controls
- Up to four global OE controls
- Individual local OE control per I/O pin
- Excellent First-Time-Fit™ and refit
- Fast path, SpeedLocking™ Path, and wide-PT path
- Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders

### ■ Zero Power (ispMACH 4000Z) and Low Power (ispMACH 4000V/B/C)

- Typical static current 10 $\mu$ A (4032Z)
- Typical static current 1.8mA (4000C)
- 1.8V core low dynamic power
- ispMACH 4000Z operational down to 1.6V  $V_{CC}$

### ■ Broad Device Offering

- 32 to 512 macrocells
- 30 to 208 I/O pins
- 44 to 256 pins/balls in TQFP, csBGA or fpBGA packages
- Multiple temperature range support
  - Commercial: 0 to 90°C junction (Tj)
  - Industrial: -40 to 105°C junction (Tj)
  - Automotive: -40 to 130°C junction (Tj)

### ■ Easy System Integration

- Operation with 3.3V, 2.5V or 1.8V LVCMOS I/O
- Operation with 3.3V (4000V), 2.5V (4000B) or 1.8V (4000C/Z) supplies
- 5V tolerant I/O for LVCMOS 3.3, LVTTL and PCI interfaces
- Hot-socketing
- Open-drain capability
- Input pull-up, pull-down or bus-keeper
- Programmable output slew rate
- 3.3V PCI compatible
- IEEE 1149.1 boundary scan testable
- 3.3V/2.5V/1.8V In-System Programmable (ISP™) using IEEE 1532 compliant interface
- I/O pins with fast setup path
- Lead-free package option

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells.

The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to  $V_{CCO}$  of 3.0V for LVCMOS 3.3, LVTTL and PCI interfaces.

**Table 1. ispMACH 4000V/B/C Family Selection Guide**

	ispMACH 4032V/B/C	ispMACH 4064V/B/C	ispMACH 4128V/B/C	ispMACH 4256V/B/C	ispMACH 4384V/B/C	ispMACH 4512V/B/C
Macrocells	32	64	128	256	384	512
I/O + Dedicated Inputs	30+2/32+4	30+2/32+4/ 64+10	64+10/92+4/ 96+4	64+10/96+14/ 128+4/160+4	128+4/192+4	128+4/208+4
t <sub>PD</sub> (ns)	2.5	2.5	2.7	3.0	3.5	3.5
t <sub>S</sub> (ns)	1.8	1.8	1.8	2.0	2.0	2.0
t <sub>CO</sub> (ns)	2.2	2.2	2.7	2.7	2.7	2.7
f <sub>MAX</sub> (MHz)	400	400	333	322	322	322
Supply Voltages (V)	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V
Pins/Package	44 TQFP 48 TQFP	44 TQFP 48 TQFP 100 TQFP	100 TQFP 128 TQFP 144 TQFP <sup>1</sup>	100 TQFP  144 TQFP <sup>1</sup> 176 TQFP 256 fpBGA <sup>2</sup>	176 TQFP 256 fpBGA	176 TQFP 256 fpBGA

1. 3.3V (4000V) only.

2. 128-I/O and 160-I/O configurations.

**Table 2. ispMACH 4000Z Family Selection Guide**

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t <sub>PD</sub> (ns)	3.5	3.7	4.2	4.5
t <sub>S</sub> (ns)	2.2	2.5	2.7	2.9
t <sub>CO</sub> (ns)	3.0	3.2	3.5	3.8
f <sub>MAX</sub> (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I <sub>CC</sub> (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

**Figure 1. ispMACH 4000V/B/C/Z Family Packages**

