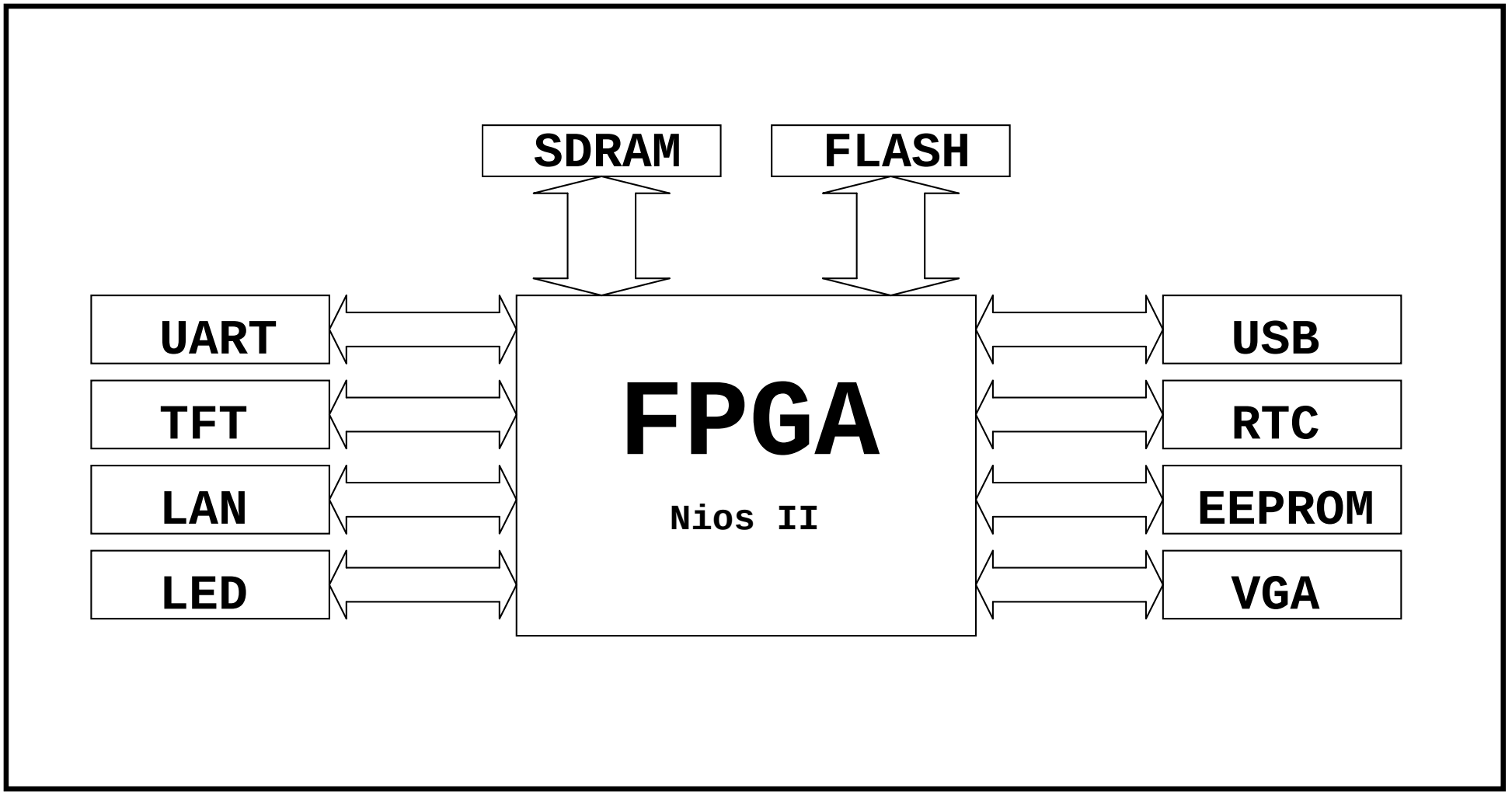

Num	Description	Num	Description
1	1_POWER	6	
2	2_INTERFACE	7	
3	3_FPGA	8	
4	4_FLASH_SDRAM	9	
5		10	

Niello Power
Model: DB2C8

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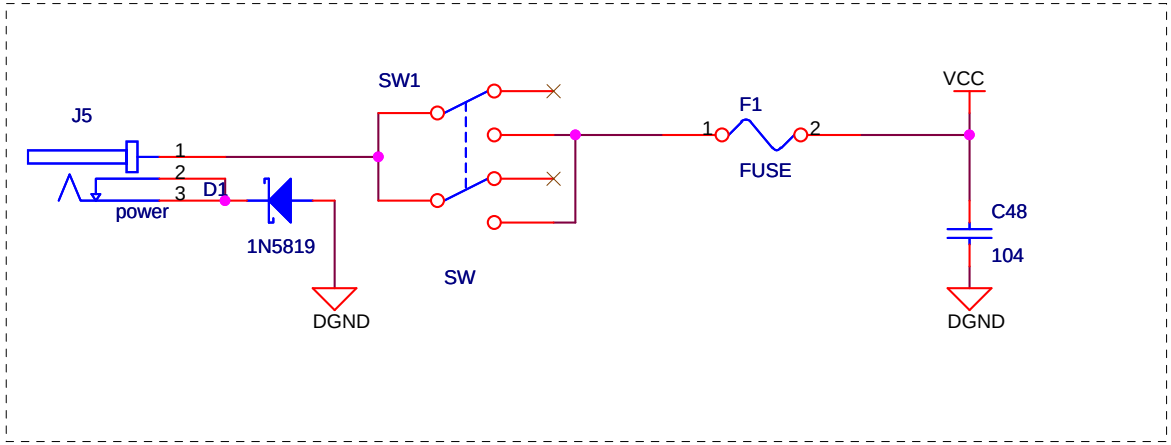
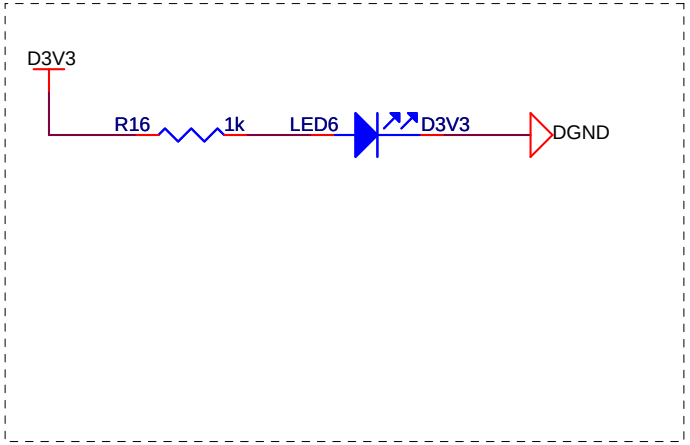
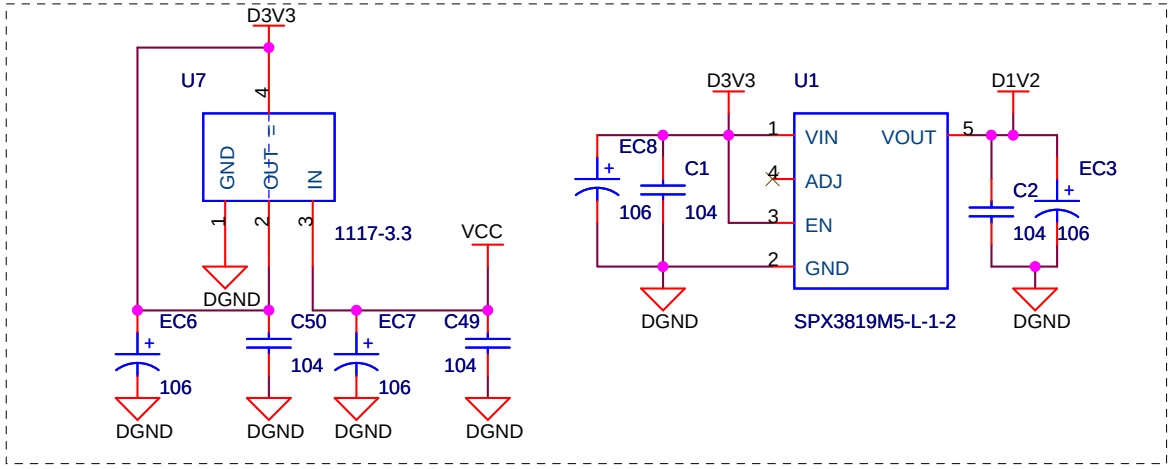
Date	2011.3.18	Verision	3.0

Power Input: 5V







Title: 1_Power		
Size: A	Document Number: *Http://www.heijin.org*	Rev: 3.0
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PIN[1..208] PIN[1..208]

F_DB[0..7] F_DB[0..7]

F_A[0..19] F_A[0..19]

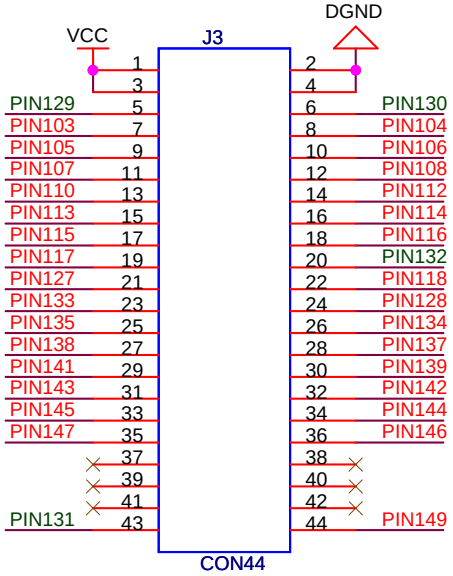
F_nCE F_nCE

F_nOE F_nOE

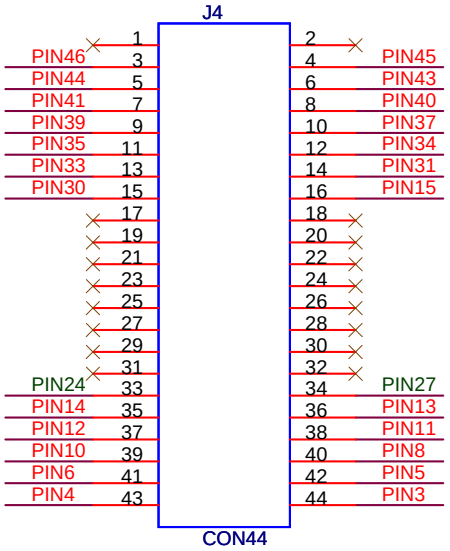
F_nWE F_nWE

F_ALSB F_ALSB

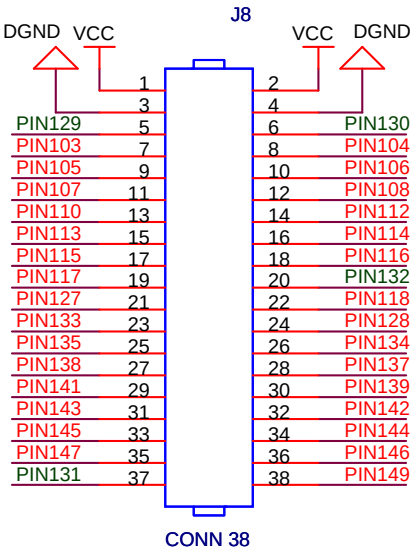
LED[0..3] LED[0..3]

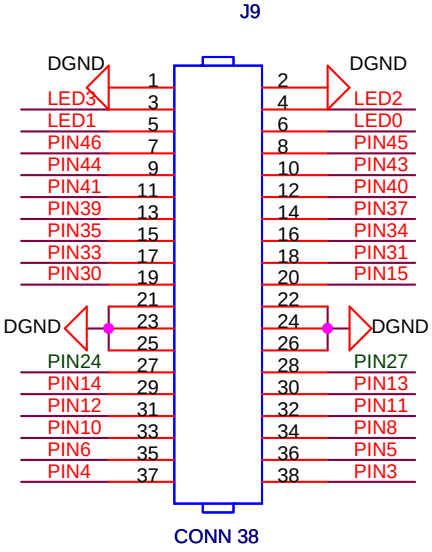


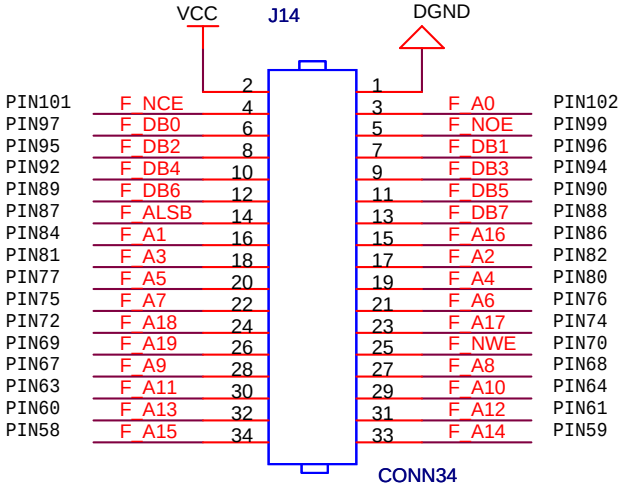
Correspond to the bottom board J7



Correspond to the bottom board J6







Title	2_INTERFACE	
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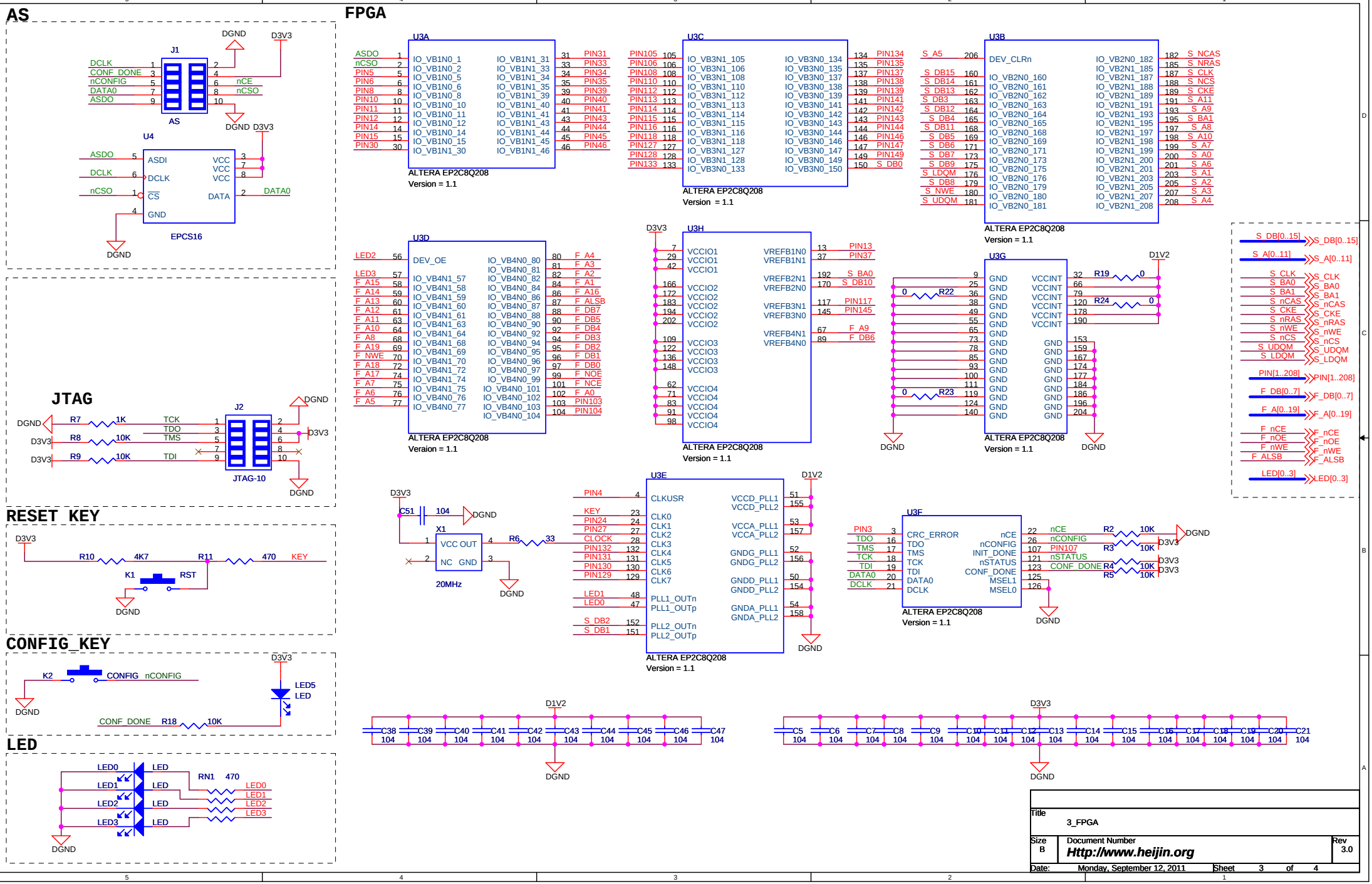

Title	3_FPGA
Size	B
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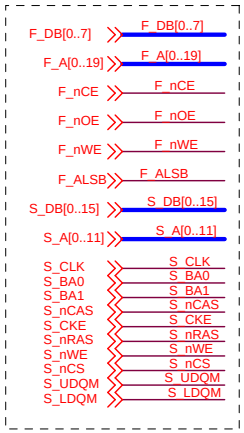
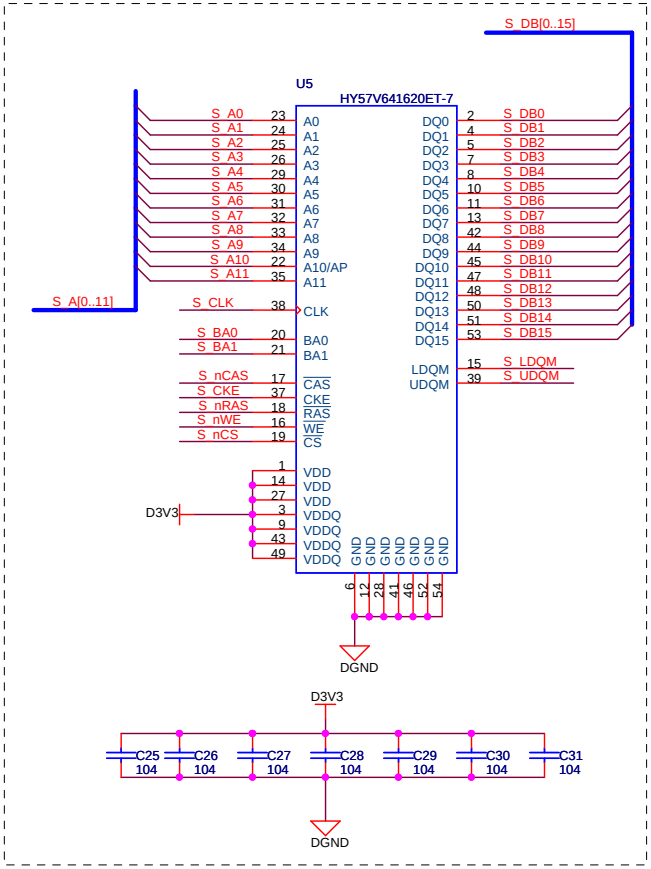
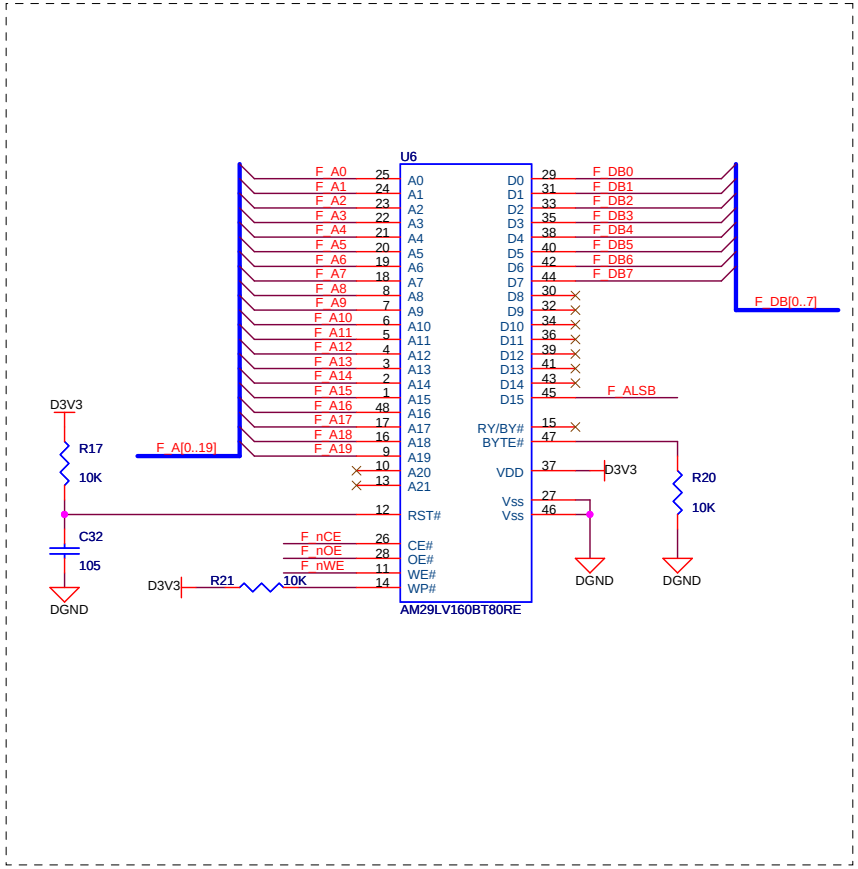


SDRAM



FLASH



Title	4_FLASH_SDRAM	
Size B	Document Number Http://www.heijin.org	Rev 3.0
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