1 AM3517/05 ARM Microprocessor

1.1 Features

- AM3517/05 ARM Microprocessor:
  - Software Compatible with OMAP™ 3 Processors**
  - MPU Subsystem
    - 500-MHz ARM Cortex-A8 Core
    - NEON SIMD Coprocessor and Vector floating point (FP) co-processor
  - Memory Interfaces:
    - 16/32- bit DDR2 Interface with 1 GByte total addressable space
    - General Purpose Memory Interface supporting 16-bit Wide Multiplexed Address/Data bus
    - 64 K-Byte shared SRAM
    - 3 Removable Removable Media Interfaces [MMC/SD/SDIO]
  - IO Voltage: DDR2 IOs: 1.8V; Other IOs: 1.8V and 3.3V,1.2V Core Voltage
  - Commerial and Industrial temperature grade*
  - 16-bit Video Input Port capable of capturing HD video
  - 491-pin sBGA package (17x17, .65 mm pitch)
  - HD resolution Display Subsystem
  - Serial Communication
    - High-End CAN Controller
    - 10/100 Mbit Ethernet MAC
    - USB OTG subsystem with standard DP/DM interface[HS/FS/LS]
    - Multiport USB Host Subsystem [HS/FS/LS]
      - 12-/8-Pin ULPI Interface or 6-/4-/3-Pin
    - Four Master/Slave Multichannel Serial Port Interface (McSPI) Ports
    - Five Multichannel Buffered Serial Ports
      - 512-Byte Transmit/Receive Buffer (McBSP1/3/4/5)
      - 5K-Byte Transmit/Receive Buffer (McBSP2)
      - SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
      - 128-Channel Transmit/Receive Mode
      - Direct Interface to I2S and PCM Device and TDM Buses
    - HDQ/1-Wire Interface
    - 4 UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
    - 3 Master/Slave High-Speed Inter-Integrated Circuit (I2C) Controllers
    - 12 32-bit General Purpose Timers
    - 1 32-bit Watchdog Timer
    - 1 32-bit 32-kHz Sync Timer
    - Up to 186 General-Purpose I/O (GPIO) Pins
- Display subsystem
  - Parallel Digital Output
  - Up to 24-Bit RGB
  - Supports Up to 2 LCD Panels
  - Support for Remote Frame Buffer Interface (RFBI) LCD Panels
  - Two 10-bit Digital-to-Analog Converters (DACs) Supporting
  - Composite NTSC/PAL Video
  - Luma/Chroma Separate Video (S-Video)
  - Serial Digital Output
  - Rotation 90-, 180-, and 270-degrees
  - Resize Images From 1/4x to 8x
  - Color Space Converter
  - 8-bit Alpha Blending
- Video Processing Front End (VPFE) 16-bit Video Input Port
  - RAW Data Interface
  - 75-MHz Maximum Pixel Clock
  - Supports REC656/CCIR656 Standard
  - Supports YCbCr422 Format (8-bit or 16-bit With Discrete Horizontal and Vertical Sync Signals)
  - Generates Optical Black Clamping Signals
  - Built-in Digital Clamping and Black Level Compensation
  - 10-bit to 8-bit A-law Compression Hardware
  - Supports up to 16K Pixels (Image Size) in Horizontal and Vertical Directions
- System Direct Memory Access (sDMA) Controller (32 Logical Channels With Configurable Priority)
- Comprehensive Power, Reset and Clock Management

PRODUCT PREVIEW

PRODUCT PREVIEW

- ARM Cortex™-A8 Memory Architecture
  - ARMv7 Architecture
    - Trust Zone
    - Thumb-2
    - MMU Enhancements
  - In-Order, Dual-Issue, Superscalar Microprocessor Core
  - NEON Multimedia Architecture
  - Over 2x Performance of ARMv6 SIMD
  - Supports Both Integer and Floating Point SIMD
  - JAZELLE RCT Execution Environment Architecture
  - Dynamic Branch Prediction with Branch Target Address Cache, Global history buffer and 8 entry return stack
  - Embedded Trace Macrocell [ETM] support for Non_invasive Debug
  - 16K-Byte instruction Cache (4-Way set-associative)
  - 16K-Byte Data Cache (4-Way Set-Associative)
  - 256K-Byte L2 Cache
- POWERVR SGX™ Graphics Accelerator
  - Tile Based Architecture Delivering up to 10 MPoly/sec
  - Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0
  - Fine Grained Task Switching, Load Balancing, and Power Management
  - Programmable, High-Quality Image Anti-Aliasing
- Endianess
  - ARM Instructions - Little Endian
  - ARM Data – Configurable
- SDRC Memory Controller
  - 16, 32-bit Memory Controller With 1G-Byte Total Address Space
  - Interfaces to Double Data Rate (DDR2) SRAM
  - SDRAM Memory Scheduler (SMS) and Rotation Engine
- General Purpose Memory Controller (GPMC)
  - 16-bit Wide Multiplexed Address/Data Bus
  - Up to 8 Chip Select Pins With 128M-Byte Address Space per Chip Select Pin
  - Glueless Interface to NOR Flash, NAND Flash (With ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
  - Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
  - Nonmultiplexed Address/Data Mode (Limited 2K-Byte Address Space)
- Test Interfaces
  - IEEE-1149.1 (JTAG) Boundary-Scan Compatible
  - Embedded Trace Macro Interface (ETM)
  - Serial Data Transport Interface (SDTI)
- 65-nm CMOS technology
- Applications:
  - Single Board Computers
  - Industrial and Home Automation
  - Digital Signage
  - Point-of-Sale Devices
  - Portable Media Player
  - Portable Industrial
  - Transportation
  - Navigation
  - Smart White Goods
  - Digital TV
  - Digital Video Camera
  - Gaming
  - Notes:
    *Operating condition restrictions apply.
    **Different memory controller to support DDR2. New IP support for VPFE, EMAC, and HECC.

1.2 Description

AM3517/05 high-performance, industrial applications processors with video, image, and graphics processing sufficient to support the following:

- Single Board Computers
- Home and Industrial automation
- Digital Signage

The device supports high-level operating systems (OSs), such as:

- Linux
- Windows CE

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor
- POWERVR SGX™ Graphics Accelerator (AM3517 Device only) Subsystem for 3D graphics acceleration to support display and gaming effects (3517 only)
- Display subsystem with several features for multiple concurrent image manipulation, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- High performance interconnects provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals. The device also offers a comprehensive clock-management scheme.

AM3517/05 devices are available in a 491-pin sBGA package.

This AM3517/05 data manual presents the electrical and mechanical specifications for the AM3517/05 ARM Microprocessor.

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the AM3517/05 ARM Microprocessor.

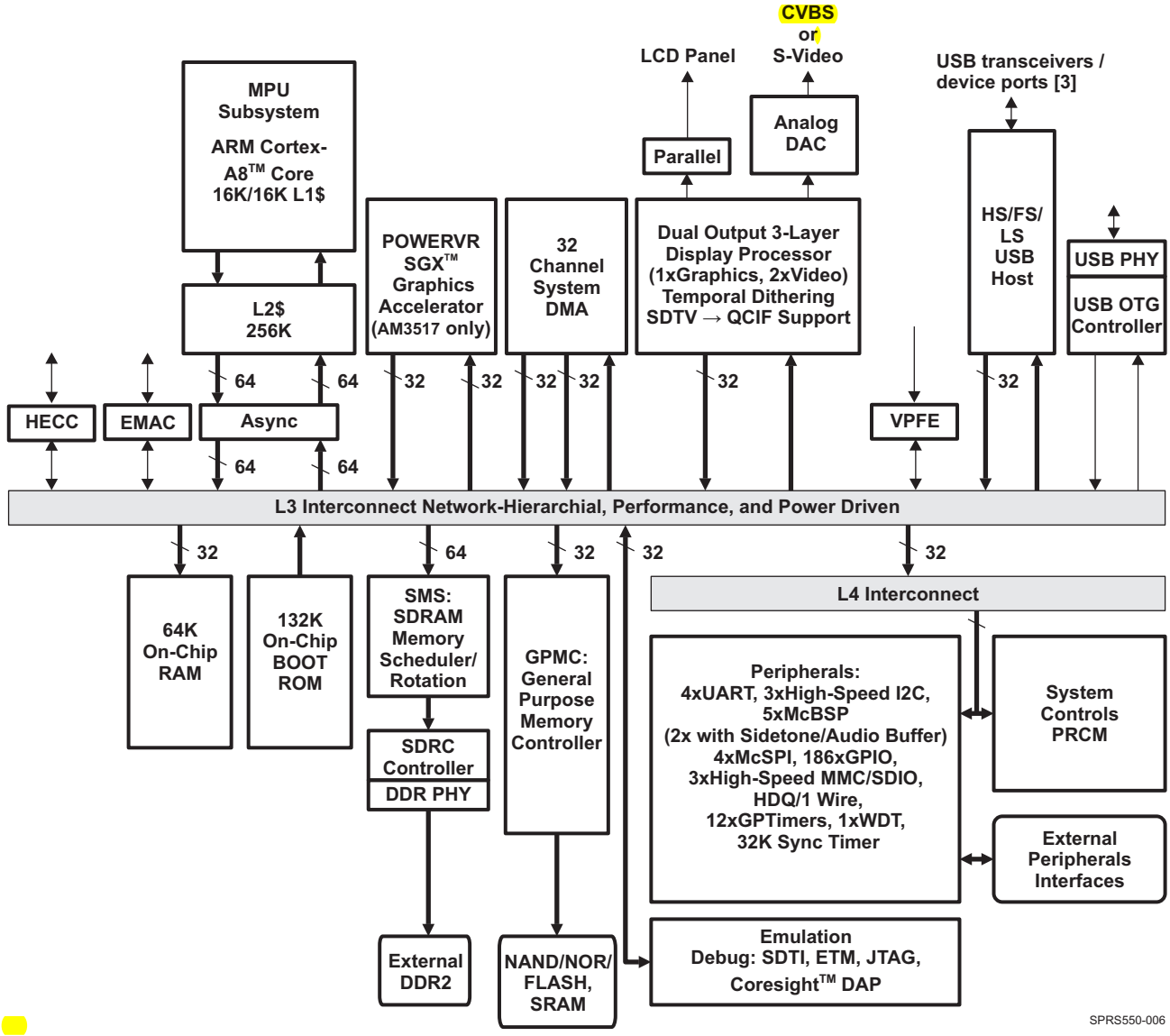

Figure 1-1. AM3517/05 Functional Block Diagram

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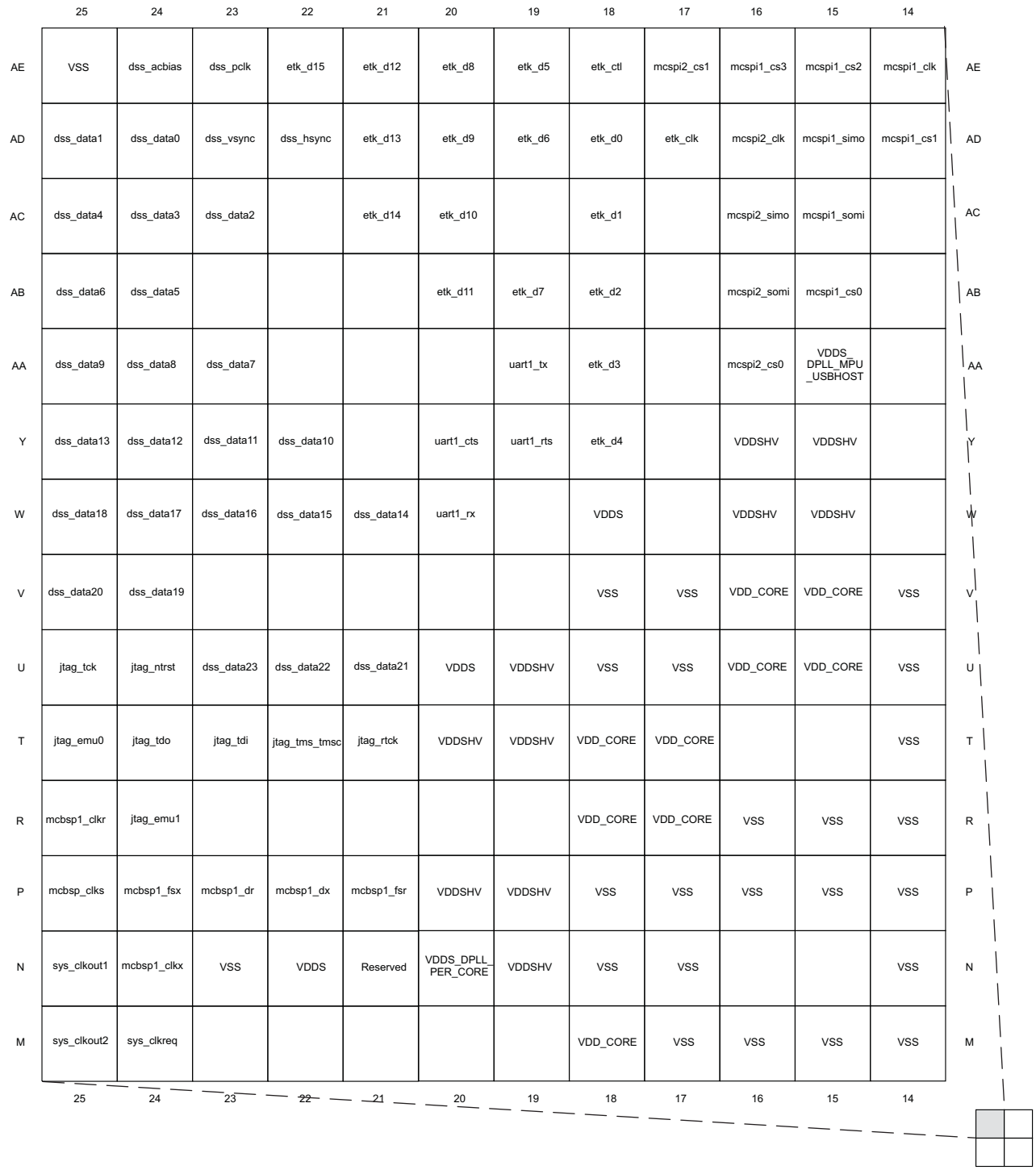
2 TERMINAL DESCRIPTION

2.1 Pin Assignments

2.1.1 Pin Map (Top View)

Figure 2-1 through Figure 2-4 show the top view of the 491-pin sPBGA package **[ZCN]** package pin assignments in four quadrants (A, B, C, and D).

Note: A pin with an "NC" designator indicates No Connection. For proper device operation, these pins must be left unconnected.

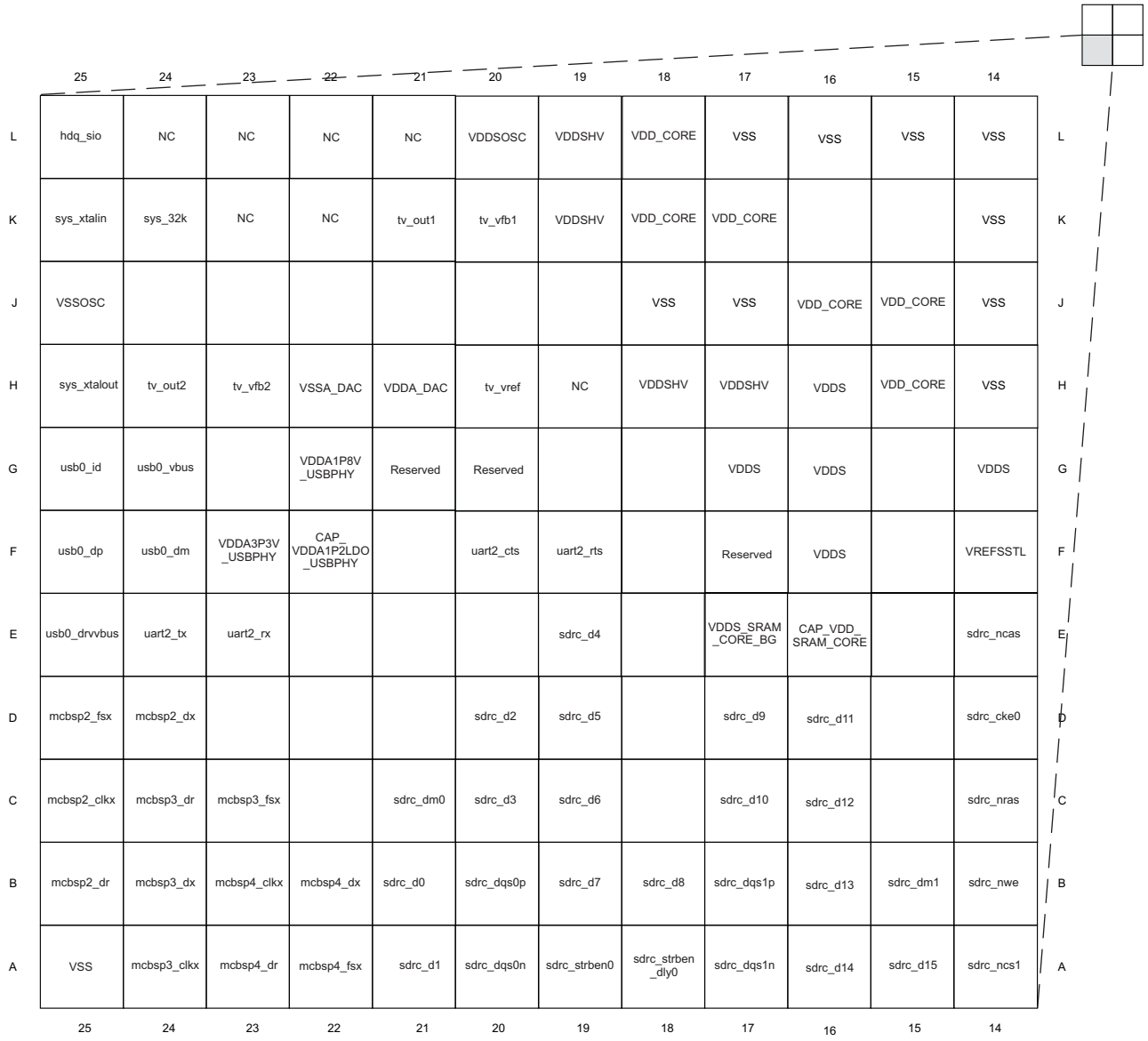


	25	24	23	22	21	20	19	18	17	16	15	14	
AE	VSS	dss_acbias	dss_pclk	etk_d15	etk_d12	etk_d8	etk_d5	etk_ctl	mcspi2_cs1	mcspi1_cs3	mcspi1_cs2	mcspi1_clk	AE
AD	dss_data1	dss_data0	dss_vsync	dss_hsync	etk_d13	etk_d9	etk_d6	etk_d0	etk_clk	mcspi2_clk	mcspi1_simo	mcspi1_cs1	AD
AC	dss_data4	dss_data3	dss_data2		etk_d14	etk_d10		etk_d1		mcspi2_simo	mcspi1_somi		AC
AB	dss_data6	dss_data5				etk_d11	etk_d7	etk_d2		mcspi2_somi	mcspi1_cs0		AB
AA	dss_data9	dss_data8	dss_data7				uart1_tx	etk_d3		mcspi2_cs0	VDDS_ DPLL_MPU _USBHOST		AA
Y	dss_data13	dss_data12	dss_data11	dss_data10		uart1_cts	uart1_rts	etk_d4		VDDSHV	VDDSHV		Y
W	dss_data18	dss_data17	dss_data16	dss_data15	dss_data14	uart1_rx		VDDS		VDDSHV	VDDSHV		W
V	dss_data20	dss_data19						VSS	VSS	VDD_CORE	VDD_CORE	VSS	V
U	jtag_tck	jtag_ntrst	dss_data23	dss_data22	dss_data21	VDDS	VDDSHV	VSS	VSS	VDD_CORE	VDD_CORE	VSS	U
T	jtag_emu0	jtag_tdo	jtag_tdi	jtag_tms_tmsc	jtag_rtck	VDDSHV	VDDSHV	VDD_CORE	VDD_CORE			VSS	T
R	mcbsp1_clkr	jtag_emu1						VDD_CORE	VDD_CORE	VSS	VSS	VSS	R
P	mcbsp_clks	mcbsp1_fsx	mcbsp1_dr	mcbsp1_dx	mcbsp1_fsr	VDDSHV	VDDSHV	VSS	VSS	VSS	VSS	VSS	P
N	sys_clkout1	mcbsp1_clkx	VSS	VDDS	Reserved	VDDS_DPLL_ PER_CORE	VDDSHV	VSS	VSS			VSS	N
M	sys_clkout2	sys_clkreq						VDD_CORE	VSS	VSS	VSS	VSS	M
	25	24	23	22	21	20	19	18	17	16	15	14	

Figure 2-1. ZCN Pin Map [Quadrant A]

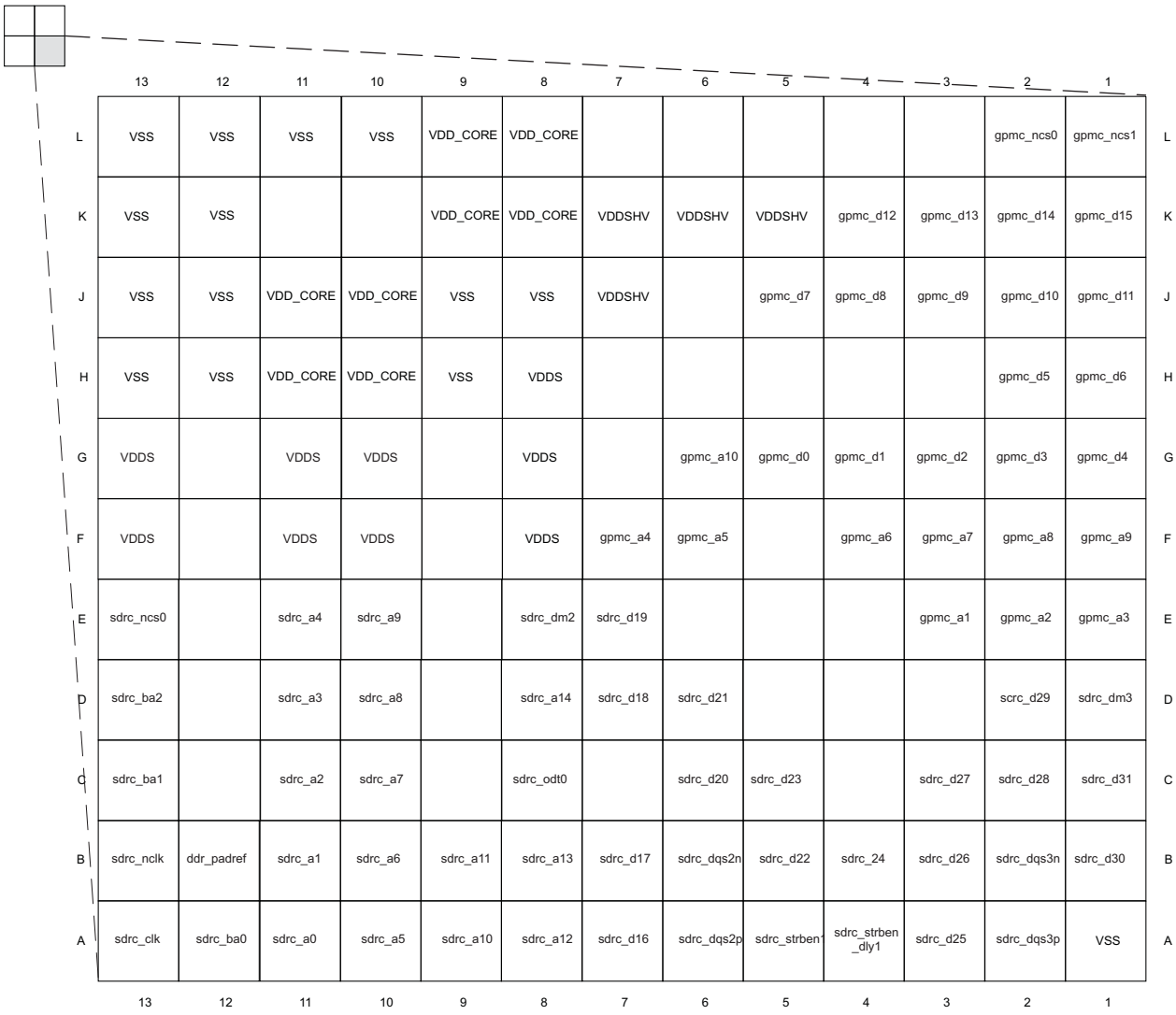
	13	12	11	10	9	8	7	6	5	4	3	2	1	
AE	mmc2_dat7	mmc2_dat3	mmc2_cmd	mmc1_dat7	mmc1_dat2	rmii_50mhz_clk	rmii_txd1	rmii_mdio_data	ccdc_data4	ccdc_data1	ccdc_wen	ccdc_hs	VSS	AE
AD	mmc2_dat6	mmc2_dat2	mmc2_clk	mmc1_dat6	mmc1_dat1	rmii_txen	rmii_txd0	rmii_mdio_clk	ccdc_data3	ccdc_data0	ccdc_vd	ccdc_pclk	ccdc_field	AD
AC	mmc2_dat5	mmc2_dat1		mmc1_dat5	mmc1_dat0		rmii_rxer	ccdc_data7	ccdc_data2		sys_boot8	sys_boot7	sys_boot6	AC
AB	mmc2_dat4	mmc2_dat0		mmc1_dat4	mmc1_cmd		rmii_crs_dv	ccdc_data6				sys_boot5	sys_boot4	AB
AA	VDDS_SRAM_MPU	CAP_VDD_SRAM_MPU		mmc1_dat3	mmc1_clk		rmii_rxd1				sys_boot3	sys_boot2	sys_boot1	AA
Y	VDDSHV	VDDSHV		VDDSHV	VDDS		rmii_rxd0	ccdc_data5		sys_boot0	sys_nreswarm	sys_nrespwron	sys_nirq	Y
W	VDDSHV	VDDSHV		VDDSHV	VDDSHV			VDDSHV	i2c3_sda	i2c3_scl		i2c2_sda	i2c2_scl	W
V	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS	VDDSHV	VDDSHV	i2c1_sda	i2c1_scl	hecc1_rxd	hecc1_txd	Reserved	V
U	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS						Reserved	gpmc_wait3	U
T	VSS	VSS			VDD_CORE	VDD_CORE	VDDSHV	VDDSHV	gpmc_wait2	gpmc_wait1	gpmc_wait0	gpmc_nwp	gpmc_nbe1	T
R	VSS	VSS	VSS	VSS	VDD_CORE	VDD_CORE	VDDSHV	VDDSHV	VDDS	gpmc_nbe0_cle	gpmc_nwe	gpmc_noe	gpmc_nadv_ale	R
P	VSS	VSS	VSS	VSS	VSS	VSS						uart3_tx_irtx	uart3_rx_irrx	P
N	VSS	VSS			VSS	VSS	VDDSHV	VDDSHV	gpmc_ncs6	gpmc_ncs7	uart3_cts_sd	uart3_cts_rctx	gpmc_clk	N
M	VSS	VSS	VSS	VSS	VSS	VSS	VDDSHV	VDDSHV	VDDSHV	gpmc_ncs2	gpmc_ncs3	gpmc_ncs4	gpmc_ncs5	M
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 2-2. ZCN Pin Map [Quadrant B]



	25	24	23	22	21	20	19	18	17	16	15	14	
L	hdq_sio	NC	NC	NC	NC	VDDSOSC	VDDSHV	VDD_CORE	VSS	VSS	VSS	VSS	L
K	sys_xtalin	sys_32k	NC	NC	tv_out1	tv_vfb1	VDDSHV	VDD_CORE	VDD_CORE			VSS	K
J	VSSOSC							VSS	VSS	VDD_CORE	VDD_CORE	VSS	J
H	sys_xtalout	tv_out2	tv_vfb2	VSSA_DAC	VDDA_DAC	tv_vref	NC	VDDSHV	VDDSHV	VDDS	VDD_CORE	VSS	H
G	usb0_id	usb0_vbus		VDDA1P8V _USBPHY	Reserved	Reserved			VDDS	VDDS		VDDS	G
F	usb0_dp	usb0_dm	VDDA3P3V _USBPHY	CAP_ VDDA1P2LDO _USBPHY		uart2_cts	uart2_rts		Reserved	VDDS		VREFSSTL	F
E	usb0_drvvbus	uart2_tx	uart2_rx				sdrc_d4		VDDS_SRAM _CORE_BG	CAP_VDD_ SRAM_CORE		sdrc_ncas	E
D	mcbsp2_fsx	mcbsp2_dx				sdrc_d2	sdrc_d5		sdrc_d9	sdrc_d11		sdrc_cke0	D
C	mcbsp2_clkx	mcbsp3_dr	mcbsp3_fsx		sdrc_dm0	sdrc_d3	sdrc_d6		sdrc_d10	sdrc_d12		sdrc_nras	C
B	mcbsp2_dr	mcbsp3_dx	mcbsp4_clkx	mcbsp4_dx	sdrc_d0	sdrc_dqs0p	sdrc_d7	sdrc_d8	sdrc_dqs1p	sdrc_d13	sdrc_dm1	sdrc_nwe	B
A	VSS	mcbsp3_clkx	mcbsp4_dr	mcbsp4_fsx	sdrc_d1	sdrc_dqs0n	sdrc_strben0	sdrc_strben _dly0	sdrc_dqs1n	sdrc_d14	sdrc_d15	sdrc_ncs1	A
	25	24	23	22	21	20	19	18	17	16	15	14	

Figure 2-3. ZCN Pin Map [Quadrant C]



	13	12	11	10	9	8	7	6	5	4	3	2	1	
L	VSS	VSS	VSS	VSS	VDD_CORE	VDD_CORE						gpmc_ncs0	gpmc_ncs1	L
K	VSS	VSS			VDD_CORE	VDD_CORE	VDDSHV	VDDSHV	VDDSHV	gpmc_d12	gpmc_d13	gpmc_d14	gpmc_d15	K
J	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS	VDDSHV		gpmc_d7	gpmc_d8	gpmc_d9	gpmc_d10	gpmc_d11	J
H	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VDDS						gpmc_d5	gpmc_d6	H
G	VDDS		VDDS	VDDS		VDDS		gpmc_a10	gpmc_d0	gpmc_d1	gpmc_d2	gpmc_d3	gpmc_d4	G
F	VDDS		VDDS	VDDS		VDDS	gpmc_a4	gpmc_a5		gpmc_a6	gpmc_a7	gpmc_a8	gpmc_a9	F
E	sdrc_ncs0		sdrc_a4	sdrc_a9		sdrc_dm2	sdrc_d19				gpmc_a1	gpmc_a2	gpmc_a3	E
D	sdrc_ba2		sdrc_a3	sdrc_a8		sdrc_a14	sdrc_d18	sdrc_d21				scrc_d29	sdrc_dm3	D
C	sdrc_ba1		sdrc_a2	sdrc_a7		sdrc_odt0		sdrc_d20	sdrc_d23		sdrc_d27	sdrc_d28	sdrc_d31	C
B	sdrc_nclk	ddr_padref	sdrc_a1	sdrc_a6	sdrc_a11	sdrc_a13	sdrc_d17	sdrc_dqs2n	sdrc_d22	sdrc_24	sdrc_d26	sdrc_dqs3n	sdrc_d30	B
A	sdrc_clk	sdrc_ba0	sdrc_a0	sdrc_a5	sdrc_a10	sdrc_a12	sdrc_d16	sdrc_dqs2p	sdrc_strben[1]	sdrc_strben_dly1	sdrc_d25	sdrc_dqs3p	VSS	A
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 2-4. ZCN Pin Map [Quadrant D]

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each pin for the ZCN package. The following list describes the table column headers.

1. **BALL LOCATION:** Ball number(s) on the bottom side associated with each signal(s) on the bottom.
2. **PIN NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).
   Note: Table 2-1 does not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 2.4, *Signal Descriptions.*
3. **MODE:** Multiplexing mode number.
   a. Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.

      Note: The default mode is the mode which is automatically configured on release of the internal GLOBAL_PWRON reset; also see the RESET REL. MODE column.
   b. Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
4. **TYPE:** Signal direction
   – I = Input
   – O = Output
   – I/O = Input/Output
   – D = Open drain
   – DS = Differential
   – A = Analog

   Note: In the safe_mode, the buffer is configured in high-impedance.
5. **BALL RESET STATE:** The state of the terminal at reset (power up).
   – 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   – 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
6. **BALL RESET REL. STATE:** The state of the terminal at reset release.
   – 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   – 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
7. **RESET REL. MODE:** This mode is automatically configured on release of the internal GLOBAL_PWRON reset.
8. **POWER:** The voltage supply that powers the terminal's I/O buffers.
9. **VOLTAGE**: Supply voltage for associated pin.
10. **HYS**: Indicates if the input buffer is with hysteresis.
11. **LOAD:** Load capacitance of the associated output buffer.
12. **PULL U/D - TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

13. **IO CELL:** IO cell information.

Note: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

Table 2-1. Ball Characteristics (ZCN Pkg.)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
B21	sdrc_d0	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A21	sdrc_d1	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D20	sdrc_d2	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C20	sdrc_d3	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
E19	sdrc_d4	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D19	sdrc_d5	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C19	sdrc_d6	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B19	sdrc_d7	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B18	sdrc_d8	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D17	sdrc_d9	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C17	sdrc_d10	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D16	sdrc_d11	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C16	sdrc_d12	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B16	sdrc_d13	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A16	sdrc_d14	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A15	sdrc_d15	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A7	sdrc_d16	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B7	sdrc_d17	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D7	sdrc_d18	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
E7	sdrc_d19	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C6	sdrc_d20	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D6	sdrc_d21	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B5	sdrc_d22	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C5	sdrc_d23	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B4	sdrc_d24	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A3	sdrc_d25	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B3	sdrc_d26	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C3	sdrc_d27	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C2	sdrc_d28	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
D2	sdrc_d29	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
B1	sdrc_d30	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
C1	sdrc_d31	0	IO	L	Z	0	VDDS	1.8V	Yes	4	PU/ PD	LVCMOS
A12	sdrc_ba0	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
C13	sdrc_ba1	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
D13	sdrc_ba2	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A11	sdrc_a0	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B11	sdrc_a1	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
C11	sdrc_a2	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
D11	sdrc_a3	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
E11	sdrc_a4	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A10	sdrc_a5	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B10	sdrc_a6	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
C10	sdrc_a7	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
D10	sdrc_a8	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
E10	sdrc_a9	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A9	sdrc_a10	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B9	sdrc_a11	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A8	sdrc_a12	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B8	sdrc_a13	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
D8	sdrc_a14	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
E13	sdrc_ncs0	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A14	sdrc_ncs1	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
A13	sdrc_clk	0	IO	L	Z	0	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
B13	sdrc_nclk	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
D14	sdrc_cke0	0	O	L	PD	7	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
	sdrc_cke0_safe	7		L								
C14	sdrc_nras	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
E14	sdrc_ncas	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B14	sdrc_nwe	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
C21	sdrc_dm0	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B15	sdrc_dm1	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
E8	sdrc_dm2	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
D1	sdrc_dm3	0	O	L	Z	0	VDDS	1.8V	No	8	PU/ PD	LVCMOS
B20	sdrc_dqs0p	0	IO	L	Z	0	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
B17	sdrc_dqs1p	0	IO	L	Z	0	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
A6	sdrc_dqs2p	0	IO	L	Z	0	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
A2	sdrc_dqs3p	0	IO	L	Z	0	VDDS	1.8V	Yes	8	PU/ PD	LVCMOS
A20	sdrc_dqs0n	0	IO	L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
A17	sdrc_dqs1n	0	IO	L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
B6	sdrc_dqs2n	0	IO	L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
B2	sdrc_dqs3n	0	IO	L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
C8	sdrc_odt0	0		L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
A19	sdrc_strben0	0		L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
A18	sdrc_strben_dly0	0		L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
A5	sdrc_strben1	0		L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
A4	sdrc_strben_dly1	0		L	Z	0	VDDS	1.8V		8	PU/ PD	LVCMOS
B12	ddr_padref	0	PWR				VDDS	1.8V				
E3	gpmc_a1	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_34	4	IO									
	safe_mode	7										
E2	gpmc_a2	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_35	4	IO									
	safe_mode	7										
E1	gpmc_a3	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_36	4	IO									
	safe_mode	7										
F7	gpmc_a4	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_37	4	IO									
	safe_mode	7										
F6	gpmc_a5	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_38	4	IO									
	safe_mode	7										
F4	gpmc_a6	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_39	4	IO									
	safe_mode	7										
F3	gpmc_a7	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_40	4	IO									
	safe_mode	7										
F2	gpmc_a8	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_41	4	IO									
	safe_mode	7										

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
F1	gpmc_a9	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq2	1	I									
	gpio_42	4	IO									
	safe_mode	7										
G6	gpmc_a10	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq3	1	I									
	gpio_43	4	IO									
	safe_mode	7										
G5	gpmc_d0	0	IO	H	PU	0	VDDSHV	1.8V/3.3V		30	PU/ PD	LVCMOS
G4	gpmc_d1	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
G3	gpmc_d2	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
G2	gpmc_d3	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
G1	gpmc_d4	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
H2	gpmc_d5	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
H1	gpmc_d6	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
J5	gpmc_d7	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
J4	gpmc_d8	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_44	4	IO									
J3	gpmc_d9	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_45	4	IO									
J2	gpmc_d10	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_46	4	IO									
J1	gpmc_d11	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_47	4	IO									
K4	gpmc_d12	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_48	4	IO									
K3	gpmc_d13	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_49	4	IO									
K2	gpmc_d14	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_50	4	IO									
K1	gpmc_d15	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_51	4	IO									
L2	gpmc_ncs0	0	O	H	Z	0	VDDSHV	1.8V/3.3V	No	30	NA	LVCMOS
L1	gpmc_ncs1	0	O	H	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_52	4	IO									
M4	gpmc_ncs2	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpt9_pwm_evt	2	IO									
	gpio_53	4	IO									
	safe_mode	7										
M3	gpmc_ncs3	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq0	1	I									
	gpt10_pwm_evt	2	IO									
	gpio_54	4	IO									
	safe_mode	7										
M2	gpmc_ncs4	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq1	1	I									
	gpt9_pwm_evt	3	IO									
	gpio_55	4	IO									
	safe_mode	7										
M1	gpmc_ncs5	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	sys_ ndmareq2	1	I									
	gpt10_pwm_ evt	3	IO									
	gpio_56	4	IO									
	safe_mode	7										
N5	gpmc_ncs6	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq3	1	I									
	gpt11_pwm_ evt	3	IO									
	gpio_57	4	IO									
	safe_mode	7										
N4	gpmc_ncs7	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpmc_io_dir	1	O									
	gpt8_pwm_e vt	3	IO									
	gpio_58	4	IO									
	safe_mode	7										
N1	gpmc_clk	0	O	L	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_59	4	IO									
R1	gpmc_nadv_ ale	0	O	L	Z	0	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
R2	gpmc_noe	0	O	H	Z	0	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
R3	gpmc_nwe	0	O	H	Z	0	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
R4	gpmc_nbe0_ cle	0	O	L	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_60	4	IO									
T1	gpmc_nbe1	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_61	4	IO									
	safe_mode	7										
T2	gpmc_nwp	0	O	L	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_62	4	IO									
T3	gpmc_wait0	0	I	H	PU	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
T4	gpmc_wait1	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart4_tx	1	O									
	gpio_63	4	IO									
	safe_mode	7										
T5	gpmc_wait2	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart4_rx	1	I									
	gpio_64	4	IO									
	safe_mode	7										
U1	gpmc_wait3	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	sys_ ndmareq1	1	I									
	uart3_cts_rct x	2	I									
	gpio_65	4	IO									
	safe_mode	7										
AE23	dss_pclk	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_66	4	IO									
	safe_mode	7										
AD22	dss_hsync	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_67	4	IO									
	safe_mode	7										
AD23	dss_vsync	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_68	4	IO									
	safe_mode	7										

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
AE24	dss_acbias	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_69	4	IO									
	safe_mode	7										
AD24	dss_data0	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart1_cts	2	I									
	dssvenc656_data0	3	I									
	gpio_70	4	IO									
	safe_mode	7										
AD25	dss_data1	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart1_rts	2	O									
	dssvenc656_data1	3	I									
	gpio_71	4	IO									
	safe_mode	7										
AC23	dss_data2	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	dssvenc656_data2	3	I									
	gpio_72	4	IO									
	safe_mode	7										
AC24	dss_data3	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	dssvenc656_data3	3	I									
	gpio_73	4	IO									
	safe_mode	7										
AC25	dss_data4	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart3_rx_ irrx	2	I									
	dssvenc656_data4	3	I									
	gpio_74	4	IO									
	safe_mode	7										
AB24	dss_data5	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart3_tx_ irtx	2	O									
	dssvenc656_data5	3	I									
	gpio_75	4	IO									
	safe_mode	7										
AB25	dss_data6	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart1_tx	2	O									
	dssvenc656_data6	3	I									
	gpio_76	4	IO									
	safe_mode	7										
AA23	dss_data7	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	uart1_rx	2	I									
	dssvenc656_data7	3	I									
	gpio_77	4	IO									
	safe_mode	7										
AA24	dss_data8	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_78	4	IO									
	safe_mode	7										
AA25	dss_data9	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_79	4	IO									
	safe_mode	7										
Y22	dss_data10	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_80	4	IO									

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	safe_mode	7										
Y23	dss_data11	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_81	4	IO									
	safe_mode	7										
Y24	dss_data12	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_82	4	IO									
	safe_mode	7										
Y25	dss_data13	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_83	4	IO									
	safe_mode	7										
W21	dss_data14	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_84	4	IO									
	safe_mode	7										
W22	dss_data15	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_85	4	IO									
	safe_mode	7										
W23	dss_data16	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_86	4	IO									
	safe_mode	7										
W24	dss_data17	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_87	4	IO									
	safe_mode	7										
W25	dss_data18	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	mcspi3_clk	2	IO									
	dss_data4	3	O									
	gpio_88	4	IO									
	safe_mode	7										
V24	dss_data19	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	mcspi3_ simo	2	IO									
	dss_data3	3	O									
	gpio_89	4	IO									
	safe_mode	7										
V25	dss_data20	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	mcspi3_ somi	2	IO									
	dss_data2	3	O									
	gpio_90	4	IO									
	safe_mode	7										
U21	dss_data21	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	mcspi3_cs0	2	IO									
	dss_data1	3	O									
	gpio_91	4	IO									
	safe_mode	7										
U22	dss_data22	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	mcspi3_cs1	2	O									
	dss_data0	3	O									
	gpio_92	4	IO									
	safe_mode	7										
U23	dss_data23	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	dss_data5	3	O									
	gpio_93	4	IO									
	safe_mode	7										
H24	tv_out2	0	O			0	VDDA_DAC	1.8V			NA	10-bit DAC
K21	tv_out1	0	O			0	VDDA_DAC	1.8V			NA	10-bit DAC

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
K20	tv_vfb1	0	O	Z	NA	0	VDDA_DAC	1.8V			NA	10-bit DAC
H23	tv_vfb2	0	O	Z	NA	0	VDDA_DAC	1.8V			NA	10-bit DAC
H20	tv_vref	0	I	Z	NA	0	VDDA_DAC	1.8V			NA	10-bit DAC
AD2	ccdc_pclk	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	gpio_94	4	IO									
	safe_mode	7										
AD1	ccdc_field	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	ccdc_data8	1	I									
	uart4_tx	2	O									
	i2c3_scl	3	OD									
	gpio_95	4	IO									
	safe_mode	7										
AE2	ccdc_ hd	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	uart4_rts	2	O									
	gpio_96	4	IO									
	safe_mode	7										
AD3	ccdc_vd	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	uart4_cts	2	I									
	gpio_97	4	IO									
	safe_mode	7										
AE3	ccdc_wen	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/PD	LVCMOS
	ccdc_data9	1	I									
	uart4_rx	2	I									
	gpio_98	4	IO									
	safe_mode	7										
AD4	ccdc_data0	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/PD	LVCMOS
	i2c3_sda	3	IOD									
	gpio_99	4	I									
	safe_mode	7										
AE4	ccdc_data1	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/PD	LVCMOS
	gpio_100	4	I									
	safe_mode	7										
AC5	ccdc_data2	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	gpio_101	4	IO									
	safe_mode	7										
AD5	ccdc_data3	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	gpio_102	4	IO									
	safe_mode	7										
AE5	ccdc_data4	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	gpio_103	4	IO									
	safe_mode	7										
Y6	ccdc_data5	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/ PD	LVCMOS
	gpio_104	4	IO									
	safe_mode	7										
AB6	ccdc_data6	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/PD	LVCMOS
	gpio_105	4	IO									
	safe_mode	7										
AC6	ccdc_data7	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	15	PU/PD	LVCMOS
	gpio_106	4	IO									
	safe_mode	7										
AE6	rmii_mdio_data	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/PD	LVCMOS
	ccdc_data8	1	I									
	gpio_107	4	IO						8			
	safe_mode	7										

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
AD6	rmii_mdio_clk	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/PD	LVCMOS
	ccdc_data9	1	I						8			
	gpio_108	4	IO									
	safe_mode	7										
Y7	rmii_rxd0	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/ PD	LVCMOS
	ccdc_data10	1	I									
	gpio_109	4	IO									
	safe_mode	7										
AA7	rmii_rxd1	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/ PD	LVCMOS
	ccdc_data11	1	I									
	gpio_110	4	IO									
	safe_mode	7										
AB7	rmii_crs_dv	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/ PD	LVCMOS
	ccdc_data12	1	I									
	gpio_111	4	IO									
	safe_mode	7										
AC7	rmii_rxer	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/ PD	LVCMOS
	ccdc_data13	1	I									
	gpio_167	4	IO									
	safe_mode	7										
AD7	rmii_txd0	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/ PD	LVCMOS
	ccdc_ data14	1	I									
	gpio_126	4	IO									
	safe_mode	7										
AE7	rmii_txd1	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	25	PU/PD	LVCMOS
	ccdc_data15	1	I									
	gpio_112	4	I									
	safe_mode	7										
AD8	rmii_txen	0	O	H	PU	7	VDDSHV	1.8V/3.3V		25	PU/PD	LVCMOS
	gpio_113	4	I						NA			
	safe_mode	7										
AE8	rmii_50mhz_clk	0	I	H	PU	7	VDDSHV	1.8V/3.3V		25	PU/ PD	LVCMOS
	gpio_114	4	I						NA			
	safe_mode	7										
D25	mcbsp2_fsx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_116	4	IO									
	safe_mode	7										
C25	mcbsp2_clkx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_117	4	IO									
	safe_mode	7										
B25	mcbsp2_dr	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_118	4	IO									
	safe_mode	7										
D24	mcbsp2_dx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_119	4	IO									
	safe_mode	7										
AA9	mmc1_clk	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_120	4	IO									
	safe_mode	7										
AB9	mmc1_cmd	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_121	4	IO									
	safe_mode	7										

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
AC9	mmc1_dat0	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi2_clk	1	IO									
	gpio_122	4	IO									
	safe_mode	7										
AD9	mmc1_dat1	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi2_simo	1	IO									
	gpio_123	4	IO									
	safe_mode	7										
AE9	mmc1_dat2	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi2_somi	1	IO									
	gpio_124	4	IO									
	safe_mode	7										
AA10	mmc1_dat3	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi2_cs0	1	O									
	gpio_125	4	IO									
	safe_mode	7										
AB10	mmc1_dat4	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
	gpio_126	4	IO									
	safe_mode	7										
AC10	mmc1_dat5	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
	gpio_127	4	IO									
	safe_mode	7										
AD10	mmc1_dat6	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
	gpio_128	4	IO									
	safe_mode	7										
AE10	mmc1_dat7	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	No	30	PU/ PD	LVCMOS
	gpio_129	4	IO									
	safe_mode	7										
AD11	mmc2_clk	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi3_clk	1	IO									
	uart4_cts	2	I									
	gpio_130	4	IO									
	safe_mode	7										
AE11	mmc2_ cmd	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi3_ simo	1	IO									
	uart4_rts	2	O									
	gpio_131	4	IO									
	safe_mode	7										
AB12	mmc2_ dat0	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi3_ somi	1	IO									
	uart4_tx	2	O									
	gpio_132	4	IO									
	safe_mode	7										
AC12	mmc2_ dat1	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart4_rx	2	I									
	gpio_133	4	IO									
	safe_mode	7										
AD12	mmc2_ dat2	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi3_cs1	1	O									
	gpio_134	4	IO									
	safe_mode	7										
AE12	mmc2_ dat3	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi3_cs0	1	IO									

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	gpio_135	4	IO									
	safe_mode	7										
AB13	mmc2_ dat4	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dir_dat0	1	O									
	mmc3_dat0	3	IO									
	gpio_136	4	IO									
	safe_mode	7										
AC13	mmc2_ dat5	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dir_dat1	1	O									
	mmc3_dat1	3	IO									
	gpio_137	4	IO									
	mm_fsusb3_rxdp	6	IO									
	safe_mode	7										
AD13	mmc2_ dat6	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dir_cmd	1	O									
	mmc3_dat2	3	IO									
	gpio_138	4	IO									
	safe_mode	7										
AE13	mmc2_ dat7	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_ clkin	1	I									
	mmc3_dat3	3	IO									
	gpio_139	4	IO									
	mm_fsusb3_rxdm	6	IO									
	safe_mode	7										
B24	mcbsp3_dx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart2_cts	1	I									
	gpio_140	4	IO									
	safe_mode	7										
C24	mcbsp3_dr	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart2_rts	1	O									
	gpio_141	4	IO									
	safe_mode	7										
A24	mcbsp3_clkx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart2_tx	1	O									
	gpio_142	4	IO									
	safe_mode	7										
C23	mcbsp3_fsx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	uart2_rx	1	I									
	gpio_143	4	IO									
	safe_mode	7										
F20	uart2_cts	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp3_dx	1	IO									
	gpt9_pwm_evt	2	IO									
	gpio_144	4	IO									
	safe_mode	7										
F19	uart2_rts	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp3_dr	1	I									
	gpt10_pwm_evt	2	IO									
	gpio_145	4	IO									

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	safe_mode	7										
E24	uart2_tx	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp3_ clkx	1	IO									
	gpt11_pwm _evt	2	IO									
	gpio_146	4	IO									
	safe_mode	7										
E23	uart2_rx	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp3_fsx	1	IO									
	gpt8_pwm_e vt	2	IO									
	gpio_147	4	IO									
	safe_mode	7										
AA19	uart1_tx	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_148	4	IO									
	safe_mode	7										
Y19	uart1_rts	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_149	4	IO									
	safe_mode	7										
Y20	uart1_cts	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_150	4	IO									
	safe_mode	7										
W20	uart1_rx	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp1_ clkr	2	I									
	mcspi4_clk	3	IO									
	gpio_151	4	IO									
	safe_mode	7										
B23	mcbsp4_ clkx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_152	4	IO									
	mm_fsusb3_t xse0	6	IO									
	safe_mode	7										
A23	mcbsp4_dr	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_153	4	IO									
	mm_fsusb3_r xrcv	6	IO									
	safe_mode	7										
B22	mcbsp4_dx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_154	4	IO									
	mm_fsusb3_t xdat	6	IO									
	safe_mode	7										
A22	mcbsp4_fsx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_155	4	IO									
	mm_fsusb3_t xen_ n	6	IO									
	safe_mode	7										
R25	mcbsp1_ clkr	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi4_clk	1	IO									
	gpio_156	4	IO									
	safe_mode	7										
P21	mcbsp1_fsr	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_157	4	IO									
	safe_mode	7										
P22	mcbsp1_dx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	mcspi4_ simo	1	IO									
	mcbsp3_dx	2	IO									
	gpio_158	4	IO									
	safe_mode	7										
P23	mcbsp1_dr	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi4_ somi	1	IO									
	mcbsp3_dr	2	I									
	gpio_159	4	IO									
	safe_mode	7										
P25	mcbsp_clks	0	I	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_160	4	IO									
	uart1_cts	5	I									
	safe_mode	7										
P24	mcbsp1_fsx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcspi4_cs0	1	IO									
	mcbsp3_fsx	2	IO									
	gpio_161	4	IO									
	safe_mode	7										
N24	mcbsp1_ clkx	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mcbsp3_ clkx	2	IO									
	gpio_162	4	IO									
	safe_mode	7										
N2	uart3_cts_ rctx	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_163	4	IO									
	safe_mode	7										
N3	uart3_rts_ sd	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_164	4	IO									
	safe_mode	7										
P1	uart3_rx_ irrx	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_165	4	IO									
	safe_mode	7										
P2	uart3_tx_ irtx	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_166	4	IO									
	safe_mode	7										
F25	usb0_dp	0	IO					5.0V	Yes		PU/ PD	LVCMOS
	uart3_tx_ irtx	1	O									
F24	usb0_dm	0	IO					5.0V	Yes		PU/ PD	LVCMOS
	uart3_rx_ irrx	1	I									
G24	usb0_vbus	0	IO				VDDA3P3V_ USBPHY	5.0V	Yes		PU/ PD	LVCMOS
G25	usb0_id	0	IO				VDDA3P3V_ USBPHY	3.3V	Yes		PU/ PD	LVCMOS
E25	usb0_drvvbus	0	O	L	PD	7	VDDSHV	1.8V/3.3V		30		
	uart3_tx_ irtx	2	O									
	gpio_125	4	IO									
	safe_mode	7										
V2	hecc1_ txd	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	24	PU/ PD	LVCMOS
	uart3_rx_ irrx	2	I									
	gpio_130	4	IO									
	safe_mode	7										
V3	hecc1_ rxd	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	24	PU/ PD	LVCMOS

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	uart3_rts_ sd	2	O									
	gpio_131	4	IO									
	safe_mode	7										
V4	i2c1_scl	0	OD	H	PU	0	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
V5	i2c1_ sda	0	IOD	H	PU	0	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
W1	i2c2_scl	0	OD	H	PU	7	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
	gpio_168	4	IO									
	safe_mode	7										
W2	i2c2_sda	0	IOD	H	PU	7	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
	gpio_183	4	IO									
	safe_mode	7										
W4	i2c3_scl	0	OD	H	PU	7	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
	gpio_184	4	IO									
	safe_mode	7										
W5	i2c3_sda	0	IOD	H	PU	7	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	Open Drain
	gpio_185	4	IO									
	safe_mode	7										
L25	hdq_sio	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	40	PU/ PD	LVCMOS
	sys_altclk	1	I									
	i2c2_sccbe	2	O									
	i2c3_sccbe	3	O									
	gpio_170	4	IO									
	safe_mode	7										
AE14	mcspi1_clk	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dat4	1	IO									
	gpio_171	4	IO									
	safe_mode	7										
AD15	mcspi1_ simo	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dat5	1	IO									
	gpio_172	4	IO									
	safe_mode	7										
AC15	mcspi1_ somi	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dat6	1	IO									
	gpio_173	4	IO									
	safe_mode	7										
AB15	mcspi1_cs0	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dat7	1	IO									
	gpio_174	4	IO									
	safe_mode	7										
AD14	mcspi1_cs1	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc3_cmd	3	IO									
	gpio_175	4	IO									
	safe_mode	7										
AE15	mcspi1_cs2	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc3_clk	3	O									
	gpio_176	4	IO									
	safe_mode	7										
AE16	mcspi1_cs3	0	O	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	hsusb2_tll_ data2	2	IO									
	hsusb2_ data2	3	IO									
	gpio_177	4	IO									

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	mm_fsusb2_txdat	5	IO									
	safe_mode	7										
AD16	mcspi2_clk	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	hsusb2_tll_data7	2	IO									
	hsusb2_data7	3	IO									
	gpio_178	4	IO									
	safe_mode	7										
AC16	mcspi2_simo	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpt9_pwm_evt	1	IO									
	hsusb2_tll_data4	2	IO									
	hsusb2_data4	3	IO									
	gpio_179	4	IO									
	safe_mode	7										
AB16	mcspi2_somi	0	IO	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpt10_pwm_evt	1	IO									
	hsusb2_tll_data5	2	IO									
	hsusb2_data5	3	IO									
	gpio_180	4	IO									
	safe_mode	7										
AA16	mcspi2_cs0	0	IO	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpt11_pwm_evt	1	IO									
	hsusb2_tll_data6	2	IO									
	hsusb2_data6	3	IO									
	gpio_181	4	IO									
	safe_mode	7										
AE17	mcspi2_cs1	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpt8_pwm_evt	1	IO									
	hsusb2_tll_data3	2	IO									
	hsusb2_data3	3	IO									
	gpio_182	4	IO									
	mm_fsusb2_txen_n	5	IO									
	safe_mode	7										
K24	sys_32k	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
K25	sys_xtalin	0	I	Z	Z	0	VDDSOSC	1.8V	NA		PU/ PD	LVCMOS
H25	sys_xtalout	0	O	Z	Z	0	VDDSOSC	1.8V	NA		PU/ PD	LVCMOS
M24	sys_clkreq	0	IO	L	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_1	4	IO									
Y1	sys_nirq	0	I	H	PU	7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_0	4	IO									
	safe_mode	7										
Y2	sys_nrespwron	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
Y3	sys_nreswarm	0	IO	L	PD	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	gpio_30	4	IO									Open Drain
Y4	sys_boot0	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_2	4	IO									
AA1	sys_boot1	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_3	4	IO									
AA2	sys_boot2	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_4	4	IO									
AA3	sys_boot3	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_5	4	IO									
AB1	sys_boot4	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dir_dat2	1	O									
	gpio_6	4	IO									
AB2	sys_boot5	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	mmc2_dir_dat3	1	O									
	gpio_7	4	IO									
AC1	sys_boot6	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_8	4	IO									
AC2	sys_boot7	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/PD	LVCMOS
AC3	sys_boot8	0	I	Z	Z	0	VDDSHV	1.8V/3.3V	Yes	30	PU/PD	LVCMOS
N25	sys_clkout1	0	O	H	PD	0/7	VDDSHV	1.8V/3.3V	Yes	30	PU/ PD	LVCMOS
	gpio_10	4	IO									
	safe_mode	7										
M25	sys_clkout2	0	O	L	PD	7	VDDSHV	1.8V/3.3V	Yes	10	PU/ PD	LVCMOS
	gpio_186	4	IO									
	safe_mode	7										
U24	jtag_ntrst	0	I	L	PD	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
U25	jtag_tck	0	I	L	PD	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
T21	jtag_rtck	0	O	L	Z	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
T22	jtag_tms_tmsc	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
T23	jtag_tdi	0	I	H	PU	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
T24	jtag_tdo	0	O	L	Z	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
T25	jtag_emu0	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_11	4	IO									
R24	jtag_emu1	0	IO	H	PU	0	VDDSHV	1.8V/3.3V	Yes	20	PU/ PD	LVCMOS
	gpio_31	4	IO									
AD17	etk_clk	0	O	H	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcbsp5_clkx	1	IO									
	mmc3_clk	2	O									
	hsusb1_stp	3	O									
	gpio_12	4	IO									
	hsusb1_tll_stp	6	I									
AE18	etk_ctl	0	O	H	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mmc3_cmd	2	IO									
	hsusb1_clk	3	O									
	gpio_13	4	IO									
	mm_fsusb1_rxdp	5	IO									
	hsusb1_tll_clk	6	O									
AD18	etk_d0	0	O	H	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_simo	1	IO									

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	mmc3_dat4	2	IO									
	hsusb1_data0	3	IO									
	gpio_14	4	IO									
	mm_fsusb1_rxrcv	5	IO									
	hsusb1_tll_data0	6	IO									
AC18	etk_d1	0	O	H	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_somi	1	IO									
	hsusb1_data1	3	IO									
	gpio_15	4	IO									
	mm_fsusb1_txse0	5	IO									
	hsusb1_tll_data1	6	IO									
AB18	etk_d2	0	O	H	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_cs0	1	IO									
	hsusb1_data2	3	IO									
	gpio_16	4	IO									
	mm_fsusb1_txdat	5	IO									
	hsusb1_tll_data2	6	IO									
AA18	etk_d3	0	O	L	PU	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_clk	1	IO									
	mmc3_dat3	2	IO									
	hsusb1_data7	3	IO									
	gpio_17	4	IO									
	hsusb1_tll_data7	6	IO									
Y18	etk_d4	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcbsp5_dr	1	I									
	mmc3_dat0	2	IO									
	hsusb1_data4	3	IO									
	gpio_18	4	IO									
	hsusb1_tll_data4	6	IO									
AE19	etk_d5	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcbsp5_fsx	1	IO									
	mmc3_dat1	2	IO									
	hsusb1_data5	3	IO									
	gpio_19	4	IO									
	hsusb1_tll_data5	6	IO									
AD19	etk_d6	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcbsp5_dx	1	IO									
	mmc3_dat2	2	IO									
	hsusb1_data6	3	IO									
	gpio_20	4	IO									
	hsusb1_tll_data6	6	IO									
AB19	etk_d7	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_cs1	1	O									

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	mmc3_dat7	2	IO									
	hsusb1_ data3	3	IO									
	gpio_21	4	IO									
	mm_fsusb1_t xen_n	5	IO									
	hsusb1_tll_ data3	6	IO									
AE20	etk_d8	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	sys_drm_ msecure	1	I									
	mmc3_dat6	2	IO									
	hsusb1_dir	3	I									
	gpio_22	4	IO									
	hsusb1_tll_di r	6	O									
AD20	etk_d9	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	sys_secure_i ndic ator	1	O									
	mmc3_dat5	2	IO									
	hsusb1_nxt	3	I									
	gpio_23	4	IO									
	mm_fsusb1_r xdm	5	IO									
	hsusb1_tll_n xt	6	O									
AC20	etk_d10	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	uart1_rx	2	I									
	hsusb2_clk	3	O									
	gpio_24	4	IO									
	hsusb2_tll_cl k	6	O									
AB20	etk_d11	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	mcspi3_clk	1	IO									
	hsusb2_stp	3	O									
	gpio_25	4	IO									
	mm_fsusb2_r xdp	5	IO									
	hsusb2_tll_st p	6	I									
AE21	etk_d12	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	hsusb2_dir	3	I									
	gpio_26	4	IO									
	hsusb2_tll_di r	6	O									
AD21	etk_d13	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	hsusb2_nxt	3	I									
	gpio_27	4	IO									
	mm_fsusb2_r xdm	5	IO									
	hsusb2_tll_n xt	6	O									
AC21	etk_d14	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS
	hsusb2_ data0	3	IO									
	gpio_28	4	IO									
	mm_fsusb2_r xrcv	5	IO									
	hsusb2_tll_ data0	6	IO									
AE22	etk_d15	0	O	L	PD	4	VDDSHV	1.8V/3.3V	Yes	9, 25	PU/ PD	LVCMOS

Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
	hsusb2_ data1	3	IO									
	gpio_29	4	IO									
	mm_fsusb2_t xse0	5	IO									
	hsusb2_tll_ data1	6	IO									
V16, V15, V11, V10, U16, U15, U11, U10, T18, T17, T9, T8, R18, R17, R9, R8, M18, L18, L9, L8, K18, K17, K9, K8, J16, J15, J11, J10, H15, H11, H10	VDD_CORE	0	PWR					1.2V				
AA13	VDDS_SRA M_MPU	0	PWR					1.8V				
E17	VDDS_SRA M_CORE_B G0	0	PWR					1.8V				
AA12	CAP_VDD_S RAM_MPU	0	PWR					1.8V				
E16	CAP_VDD_S RAM_CORE	0	PWR					1.2V				
AA15	VDDS_DPLL _MPU_USB HOST	0	PWR					1.8V				
N20	VDDS_DPLL _PER_CORE	0	PWR					1.8V				
H21	VDDA_DAC	0	PWR					1.8V				
F23	VDDA3P3V_ USBPHY	0	PWR					3.3V				
G22	VDDA1P8V_ USBPHY	0	PWR					1.8V				
F22	CAP_VDDA1 P2LDO_USB PHY	0	PWR					1.2V				
Y16, Y15, Y13, Y12, Y10, W16, W15, W13, W12,W10, W9, W6, V7, V6, U19, T20, T19, T7, T6, R7, R6, P20, P19, N19, N7, N6, M7, M6, M5, L19, K19, K7, K6, K5, J7, H18, H17	VDDSHV	0	PWR					1.8V/3.3V				
Y9, W18, U20, R5, H16, H8, G17, G16, G14, G13, G11, G10, G8, F16, F13, F11, F10, F8, N22	VDDS	0	PWR					1.8V				
F14	VREFSSTL	0	PWR									
L20	VDDSOSC	0	PWR					1.8V				

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Table 2-1. Ball Characteristics (ZCN Pkg.) (continued)

BALL LOCATION [1]	PIN NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	POWER [8]	VOLTAGE [9]	HYS [10]	LOAD (pF) [11]	PULL U/D TYPE [12]	IO CELL [13]
AE25, AE1, V18, V17, V14, V13, V12, V9, V8, U18, U17, U14, U13, U12, U9, U8, T14, T13, T12, R16, R15, R14, R13, R12, R11, R10, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, N18, N17, N14, N13, N12, N9, N8, M17, M16, M15, M14, M13,M12, M11, M10, M9, M8, L17, L16, L15, L14, L13, L12, L11, L10, K14, K13, K12, J18, J17, J14, J13, J12, J9, J8, H14, H13, H12, H9, A25, A1, N23	VSS	0	GND									
H22	VSSA_DAC	0	GND									
L24, L23, L22, L21, L20, K23, K22, H19	NC(1)											
F17(2)	Reserved											
U2(3)	Reserved											
V1(3)	Reserved											
N21(4)	Reserved											
G20(5)	Reserved											
G21(5)	Reserved											

(1) "NC" indicates "No Connect". For proper device operation, these pins ***must be*** left unconnected.
(2) For proper device operation, this pin should be left unconnected.
(3) For proper device operation, this pin ***must be*** pulled up via a 10k-Ω resistor.
(4) For proper device operation, this pin ***must be*** connected to ground via a 1µF capacitor.
(5) For proper device operation, this pin ***must be*** tied to VSS.

2.3 Multiplexing Characteristics

Table Table 2-2 provides descriptions of the AM3517/05 pin multiplexing on the ZCN package.

Table 2-2. Multiplexing Characteristics (ZCN Pkg.)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
B21	sdrc_d0							
A21	sdrc_d1							
D20	sdrc_d2							
C20	sdrc_d3							
E19	sdrc_d4							
D19	sdrc_d5							
C19	sdrc_d6							
B19	sdrc_d7							
B18	sdrc_d8							
D17	sdrc_d9							
C17	sdrc_d10							
D16	sdrc_d11							
C16	sdrc_d12							
B16	sdrc_d13							
A16	sdrc_d14							
A15	sdrc_d15							
A7	sdrc_d16							
B7	sdrc_d17							
D7	sdrc_d18							
E7	sdrc_d19							
C6	sdrc_d20							
D6	sdrc_d21							
B5	sdrc_d22							
C5	sdrc_d23							
B4	sdrc_d24							
A3	sdrc_d25							
B3	sdrc_d26							
C3	sdrc_d27							
C2	sdrc_d28							
D2	sdrc_d29							
B1	sdrc_d30							
C1	sdrc_d31							
A12	sdrc_ba0							
C13	sdrc_ba1							
D13	sdrc_ba2							
A11	sdrc_a0							
B11	sdrc_a1							
C11	sdrc_a2							
D11	sdrc_a3							
E11	sdrc_a4							
A10	sdrc_a5							
B10	sdrc_a6							
C10	sdrc_a7							
D10	sdrc_a8							
E10	sdrc_a9							
A9	sdrc_a10							

Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
B9	sdrc_a11							
A8	sdrc_a12							
B8	sdrc_a13							
D8	sdrc_a14							
E13	sdrc_ncs0							
A14	sdrc_ncs1							
A13	sdrc_clk							
B13	sdrc_nclk							
D14	sdrc_cke0							ddr_cke0_safe
C14	sdrc_nras							
E14	sdrc_ncas							
B14	sdrc_nwe							
C21	sdrc_dm0							
B15	sdrc_dm1							
E8	sdrc_dm2							
D1	sdrc_dm3							
B20	sdrc_dqs0p							
B17	sdrc_dqs1p							
A6	sdrc_dqs2p							
A2	sdrc_dqs3p							
A20	sdrc_dqs0n							
A17	sdrc_dqs1n							
B6	sdrc_dqs2n							
B2	sdrc_dqs3n							
C8	sdrc_odt0							
A19	sdrc_strben0							
A18	sdrc_strben_dly 0							
A5	sdrc_strben1							
A4	sdrc_strben_dly 1							
E3	gpmc_a1				gpio_34			safe_mode
E2	gpmc_a2				gpio_35			safe_mode
E1	gpmc_a3				gpio_36			safe_mode
F7	gpmc_a4				gpio_37			safe_mode
F6	gpmc_a5				gpio_38			safe_mode
F4	gpmc_a6				gpio_39			safe_mode
F3	gpmc_a7				gpio_40			safe_mode
F2	gpmc_a8				gpio_41			safe_mode
F1	gpmc_a9	sys_ndmareq2			gpio_42			safe_mode
G6	gpmc_a10	sys_ndmareq3			gpio_43			safe_mode
G5	gpmc_d0							
G4	gpmc_d1							
G3	gpmc_d2							
G2	gpmc_d3							
G1	gpmc_d4							
H2	gpmc_d5							
H1	gpmc_d6							
J5	gpmc_d7							
J4	gpmc_d8				gpio_44			
J3	gpmc_d9				gpio_45			

Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
J2	gpmc_d10				gpio_46			
J1	gpmc_d11				gpio_47			
K4	gpmc_d12				gpio_48			
K3	gpmc_d13				gpio_49			
K2	gpmc_d14				gpio_50			
K1	gpmc_d15				gpio_51			
L2	gpmc_ncs0							
L1	gpmc_ncs1				gpio_52			
M4	gpmc_ncs2		gpt9_pwm_evt		gpio_53			safe_mode
M3	gpmc_ncs3	sys_ndmareq0	gpt10_pwm_evt		gpio_54			safe_mode
M2	gpmc_ncs4	sys_ndmareq1		gpt9_pwm_evt	gpio_55			safe_mode
M1	gpmc_ncs5	sys_ndmareq2		gpt10_pwm_evt	gpio_56			safe_mode
N5	gpmc_ncs6	sys_ndmareq3		gpt11_pwm_evt	gpio_57			safe_mode
N4	gpmc_ncs7	gpmc_io_dir		gpt8_pwm_evt	gpio_58			safe_mode
N1	gpmc_clk				gpio_59			
R1	gpmc_nadv_ale							
R2	gpmc_noe							
R3	gpmc_nwe							
R4	gpmc_nbe0_cle				gpio_60			
T1	gpmc_nbe1				gpio_61			safe_mode
T2	gpmc_nwp				gpio_62			
T3	gpmc_wait0							
T4	gpmc_wait1	uart4_tx			gpio_63			safe_mode
T5	gpmc_wait2	uart4_rx			gpio_64			safe_mode
U1	gpmc_wait3	sys_ndmareq1	uart3_cts_rctx		gpio_65			safe_mode
AE23	dss_pclk				gpio_66	hw_dbg12		safe_mode
AD22	dss_hsync				gpio_67	hw_dbg13		safe_mode
AD23	dss_vsync				gpio_68			safe_mode
AE24	dss_acbias				gpio_69			safe_mode
AD24	dss_data0		uart1_cts		gpio_70			safe_mode
AD25	dss_data1		uart1_rts		gpio_71			safe_mode
AC23	dss_data2				gpio_72			safe_mode
AC24	dss_data3				gpio_73			safe_mode
AC25	dss_data4		uart3_rx_irrx		gpio_74			safe_mode
AB24	dss_data5		uart3_tx_irtx		gpio_75			safe_mode
AB25	dss_data6		uart1_tx		gpio_76	hw_dbg14		safe_mode
AA23	dss_data7		uart1_rx		gpio_77	hw_dbg15		safe_mode
AA24	dss_data8				gpio_78	hw_dbg16		safe_mode
AA25	dss_data9				gpio_79	hw_dbg17		safe_mode
Y22	dss_data10				gpio_80			safe_mode
Y23	dss_data11				gpio_81			safe_mode
Y24	dss_data12				gpio_82			safe_mode
Y25	dss_data13				gpio_83			safe_mode
W21	dss_data14				gpio_84			safe_mode
W22	dss_data15				gpio_85			safe_mode
W23	dss_data16				gpio_86			safe_mode
W24	dss_data17				gpio_87			safe_mode
W25	dss_data18		mcspi3_clk	dss_data4	gpio_88			safe_mode
V24	dss_data19		mcspi3_simo	dss_data3	gpio_89			safe_mode
V25	dss_data20		mcspi3_somi	dss_data2	gpio_90			safe_mode

Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
U21	dss_data21		mcspi3_cs0	dss_data1	gpio_91			safe_mode
U22	dss_data22		mcspi3_cs1	dss_data0	gpio_92			safe_mode
U23	dss_data23			dss_data5	gpio_93			safe_mode
K20	tv_vfb1							
K21	tv_out1							
H23	tv_vfb2							
H24	tv_out2							
H20	tv_vref							
AD2	ccdc_pclk				gpio_94	hw_dbg0		safe_mode
AD1	ccdc_field	ccdc_data8	uart4_tx	i2c3_scl	gpio_95	hw_dbg1		safe_mode
AE2	ccdc_hd		uart4_rts		gpio_96			safe_mode
AD3	ccdc_vd		uart4_cts		gpio_97	hw_dbg2		safe_mode
AE3	ccdc_wen	ccdc_data9	uart4_rx		gpio_98	hw_dbg3		safe_mode
AD4	ccdc_data0			i2c3_sda	gpio_99			safe_mode
AE4	ccdc_data1				gpio_100			safe_mode
AC5	ccdc_data2				gpio_101	hw_dbg4		safe_mode
AD5	ccdc_data3				gpio_102	hw_dbg5		safe_mode
AE5	ccdc_data4				gpio_103	hw_dbg6		safe_mode
Y6	ccdc_data5				gpio_104	hw_dbg7		safe_mode
AB6	ccdc_data6				gpio_105			safe_mode
AC6	ccdc_data7				gpio_106			safe_mode
AE6	rmii_mdio_data	ccdc_data8			gpio_107			safe_mode
AD6	rmii_mdio_clk	ccdc_data9			gpio_108			safe_mode
Y7	rmii_rxd0	ccdc_data10			gpio_109	hw_dbg8		safe_mode
AA7	rmii_rxd1	ccdc_data11			gpio_110	hw_dbg9		safe_mode
AB7	rmii_crs_dv	ccdc_data12			gpio_111			safe_mode
AC7	rmii_rxer	ccdc_data13			gpio_167	hw_dbg10		safe_mode
AD7	rmii_txd0	ccdc_data14			gpio_126	hw_dbg11		safe_mode
AE7	rmii_txd1	ccdc_data15			gpio_112			safe_mode
AD8	rmii_txen				gpio_113			safe_mode
AE8	rmii_50mhz_clk				gpio_114			safe_mode
D25	mcbsp2_fsx				gpio_116			safe_mode
C25	mcbsp2_clkx				gpio_117			safe_mode
B25	mcbsp2_dr				gpio_118			safe_mode
D24	mcbsp2_dx				gpio_119			safe_mode
AA9	mmc1_clk				gpio_120			safe_mode
AB9	mmc1_cmd				gpio_121			safe_mode
AC9	mmc1_dat0	mcspi2_clk			gpio_122			safe_mode
AD9	mmc1_dat1	mcspi2_simo			gpio_123			safe_mode
AE9	mmc1_dat2	mcspi2_somi			gpio_124			safe_mode
AA10	mmc1_dat3	mcspi2_cs0			gpio_125			safe_mode
AB10	mmc1_dat4				gpio_126			safe_mode
AC10	mmc1_dat5				gpio_127			safe_mode
AD10	mmc1_dat6				gpio_128			safe_mode
AE10	mmc1_dat7				gpio_129			safe_mode
AD11	mmc2_clk	mcspi3_clk	uart4_cts		gpio_130			safe_mode
AE11	mmc2_cmd	mcspi3_simo	uart4_rts		gpio_131			safe_mode
AB12	mmc2_dat0	mcspi3_somi	uart4_tx		gpio_132			safe_mode
AC12	mmc2_dat1		uart4_rx		gpio_133			safe_mode
AD12	mmc2_dat2	mcspi3_cs1			gpio_134			safe_mode

Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
AE12	mmc2_dat3	mcspi3_cs0			gpio_135			safe_mode
AB13	mmc2_dat4	mmc2_dir_dat0		mmc3_dat0	gpio_136			safe_mode
AC13	mmc2_dat5	mmc2_dir_dat1		mmc3_dat1	gpio_137		mm_fsusb3_rxdp	safe_mode
AD13	mmc2_dat6	mmc2_dir_cmd		mmc3_dat2	gpio_138			safe_mode
AE13	mmc2_dat7	mmc2_clkin		mmc3_dat3	gpio_139		mm_fsusb3_rxdm	safe_mode
B24	mcbsp3_dx	uart2_cts			gpio_140			safe_mode
C24	mcbsp3_dr	uart2_rts			gpio_141			safe_mode
A24	mcbsp3_clkx	uart2_tx			gpio_142			safe_mode
C23	mcbsp3_fsx	uart2_rx			gpio_143			safe_mode
F20	uart2_cts	mcbsp3_dx	gpt9_pwm_evt		gpio_144			safe_mode
F19	uart2_rts	mcbsp3_dr	gpt10_pwm_evt		gpio_145			safe_mode
E24	uart2_tx	mcbsp3_clkx	gpt11_pwm_evt		gpio_146			safe_mode
E23	uart2_rx	mcbsp3_fsx	gpt8_pwm_evt		gpio_147			safe_mode
AA19	uart1_tx				gpio_148			safe_mode
Y19	uart1_rts				gpio_149			safe_mode
Y20	uart1_cts				gpio_150			safe_mode
W20	uart1_rx		mcbsp1_clkr	mcspi4_clk	gpio_151			safe_mode
B23	mcbsp4_clkx				gpio_152		mm_fsusb3_txse0	safe_mode
A23	mcbsp4_dr				gpio_153		mm_fsusb3_rxrcv	safe_mode
B22	mcbsp4_dx				gpio_154		mm_fsusb3_txdat	safe_mode
A22	mcbsp4_fsx				gpio_155		mm_fsusb3_txen_n	safe_mode
R25	mcbsp1_clkr	mcspi4_clk			gpio_156			safe_mode
P21	mcbsp1_fsr				gpio_157			safe_mode
P22	mcbsp1_dx	mcspi4_simo	mcbsp3_dx		gpio_158			safe_mode
P23	mcbsp1_dr	mcspi4_somi	mcbsp3_dr		gpio_159			safe_mode
P25	mcbsp_clks				gpio_160	uart1_cts		safe_mode
P24	mcbsp1_fsx	mcspi4_cs0	mcbsp3_fsx		gpio_161			safe_mode
N24	mcbsp1_clkx		mcbsp3_clkx		gpio_162			safe_mode
N2	uart3_cts_rctx				gpio_163			safe_mode
N3	uart3_rts_sd				gpio_164			safe_mode
P1	uart3_rx_irrx				gpio_165			safe_mode
P2	uart3_tx_irtx				gpio_166			
F25	usb0_dp	uart3_rx_irrx						
F24	usb0_dm	uart3_tx_irtx						
G24	usb0_vbus							
G25	usb0_id							
E25	usb0_drvvbus		uart3_tx_irtx					safe_mode
V2	hecc1_txd		uart3_rx_irrx		gpio_130			safe_mode
V3	hecc1_rxd		uart3_rts_sd		gpio_131			safe_mode
V4	i2c1_scl							
V5	i2c1_sda							
W1	i2c2_scl				gpio_168			safe_mode
W2	i2c2_sda				gpio_183			safe_mode
W4	i2c3_scl				gpio_184			safe_mode
W5	i2c3_sda				gpio_185			safe_mode
L25	hdq_sio	sys_altclk	i2c2_sccbe	i2c3_sccbe	gpio_170			safe_mode

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Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
AE14	mcspi1_clk	mmc2_dat4			gpio_171			safe_mode
AD15	mcspi1_simo	mmc2_dat5			gpio_172			safe_mode
AC15	mcspi1_somi	mmc2_dat6			gpio_173			safe_mode
AB15	mcspi1_cs0	mmc2_dat7			gpio_174			safe_mode
AD14	mcspi1_cs1			mmc3_cmd	gpio_175			safe_mode
AE15	mcspi1_cs2			mmc3_clk	gpio_176			safe_mode
AE16	mcspi1_cs3		hsusb2_tll_data2	hsusb2_data2	gpio_177	mm_fsusb2_txdat		safe_mode
AD16	mcspi2_clk		hsusb2_tll_data7	hsusb2_data7	gpio_178			safe_mode
AC16	mcspi2_simo	gpt9_pwm_evt	hsusb2_tll_data4	hsusb2_data4	gpio_179			safe_mode
AB16	mcspi2_somi	gpt10_pwm_evt	hsusb2_tll_data5	hsusb2_data5	gpio_180			safe_mode
AA16	mcspi2_cs0	gpt11_pwm_evt	hsusb2_tll_data6	hsusb2_data6	gpio_181			safe_mode
AE17	mcspi2_cs1	gpt8_pwm_evt	hsusb2_tll_data3	hsusb2_data3	gpio_182	mm_fsusb2_txen_n		safe_mode
Y1	sys_nirq				gpio_0			safe_mode
M25	sys_clkout2				gpio_186			safe_mode
AD17	etk_clk	mcbsp5_clkx	mmc3_clk	hsusb1_stp	gpio_12		hsusb1_tll_stp	hw_dbg0
AE18	etk_ctl		mmc3_cmd	hsusb1_clk	gpio_13	mm_fsusb1_rxdp	hsusb1_tll_clk	hw_dbg1
AD18	etk_d0	mcspi3_simo	mmc3_dat4	hsusb1_data0	gpio_14	mm_fsusb1_rxrcv	hsusb1_tll_data0	hw_dbg2
AC18	etk_d1	mcspi3_somi		hsusb1_data1	gpio_15	mm_fsusb1_txse0	hsusb1_tll_data1	hw_dbg3
AB18	etk_d2	mcspi3_cs0		hsusb1_data2	gpio_16	mm_fsusb1_txdat	hsusb1_tll_data2	hw_dbg4
AA18	etk_d3	mcspi3_clk	mmc3_dat3	hsusb1_data7	gpio_17		hsusb1_tll_data7	hw_dbg5
Y18	etk_d4	mcbsp5_dr	mmc3_dat0	hsusb1_data4	gpio_18		hsusb1_tll_data4	hw_dbg6
AE19	etk_d5	mcbsp5_fsx	mmc3_dat1	hsusb1_data5	gpio_19		hsusb1_tll_data5	hw_dbg7
AD19	etk_d6	mcbsp5_dx	mmc3_dat2	hsusb1_data6	gpio_20		hsusb1_tll_data6	hw_dbg8
AB19	etk_d7	mcspi3_cs1	mmc3_dat7	hsusb1_data3	gpio_21	mm_fsusb1_txen_n	hsusb1_tll_data3	hw_dbg9
AE20	etk_d8	sys_drm_msecure	mmc3_dat6	hsusb1_dir	gpio_22		hsusb1_tll_dir	hw_dbg10
AD20	etk_d9	sys_secure_indicator	mmc3_dat5	hsusb1_nxt	gpio_23	mm_fsusb1_rxdm	hsusb1_tll_nxt	hw_dbg11
AC20	etk_d10		uart1_rx	hsusb2_clk	gpio_24		hsusb2_tll_clk	hw_dbg12
AB20	etk_d11	mcspi3_clk		hsusb2_stp	gpio_25	mm_fsusb2_rxdp	hsusb2_tll_stp	hw_dbg13
AE21	etk_d12			hsusb2_dir	gpio_26		hsusb2_tll_dir	hw_dbg14
AD21	etk_d13			hsusb2_nxt	gpio_27	mm_fsusb2_rxdm	hsusb2_tll_nxt	hw_dbg15
AC21	etk_d14			hsusb2_data0	gpio_28	mm_fsusb2_rxrcv	hsusb2_tll_data0	hw_dbg16
AE22	etk_d15			hsusb2_data1	gpio_29	mm_fsusb2_txse0	hsusb2_tll_data1	hw_dbg17
K24	sys_32k							
K25	sys_xtalin							
H25	sys_xtalout							
M24	sys_clkreq				gpio_1			

Table 2-2. Multiplexing Characteristics (ZCN Pkg.) (continued)

PIN MULTIPLEXING CONFIGURATIONS								
Ball No.	**Option 0**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Option 5**	**Option 6**	**Option 7**
Y2	sys_nrespwron							
Y3	sys_nreswarm				gpio_30			
Y4	sys_boot0				gpio_2			
AA1	sys_boot1				gpio_3			
AA2	sys_boot2				gpio_4			
AA3	sys_boot3				gpio_5			
AB1	sys_boot4	mmc2_dir_dat2			gpio_6			
AB2	sys_boot5	mmc2_dir_dat3			gpio_7			
AC1	sys_boot6				gpio_8			
AC2	sys_boot7							
AC3	sys_boot8							
N25	sys_clkout1				gpio_10			safe_mode
U24	jtag_ntrst							
U25	jtag_tck							
T21	jtag_rtck							
T22	jtag_tms_tmsc							
T23	jtag_tdi							
T24	jtag_tdo							
T25	jtag_emu0				gpio_11			
R24	jtag_emu1				gpio_31			
B12	ddr_padref							

2.4 Signal Description

Many signals are available on multiple pins according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The signal name
2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Type = Ball type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - D = Open Drain
   - DS = Differential
   - A = Analog
4. **BALL:** Associated ball location
5. **SUBSYSTEM PIN MULTIPLEXING:** Contains a list of the pin multiplexing options at the module/subsystem level. The pin function is selected at the module/system level.

   Note: The Subsystem Multiplexing Signals are not described in Table 2-1 through .

2.4.1 External Memory Interfaces

Table 2-3. External Memory Interfaces – GPMC Signals Description (ZCN Pkg.)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL (ZCN Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [5]
gpmc_a1	General-purpose memory address bit 1	O	E3/ G5	gpmc_a17/ gpmc_d0
gpmc_a2	General-purpose memory address bit 2	O	E2/ G4	gpmc_a18/ gpmc_d1
gpmc_a3	General-purpose memory address bit 3	O	E1/ G3	gpmc_a19/ gpmc_d2
gpmc_a4	General-purpose memory address bit 4	O	F7/ G2	gpmc_a20/ gpmc_d3
gpmc_a5	General-purpose memory address bit 5	O	F6/ G1	gpmc_a21/ gpmc_d4
gpmc_a6	General-purpose memory address bit 6	O	F4/ H2	gpmc_a22/ gpmc_d5
gpmc_a7	General-purpose memory address bit 7	O	F3/ H1	gpmc_a23/ gpmc_d6
gpmc_a8	General-purpose memory address bit 8	O	F2/ J5	gpmc_a24/ gpmc_d7
gpmc_a9	General-purpose memory address bit 9	O	F1/ J4	gpmc_a25/ gpmc_d8
gpmc_a10	General-purpose memory address bit 10	O	G6/ J3	gpmc_a26/ gpmc_d9
gpmc_a11	General-purpose memory address bit 11	O	J2	/ gpmc_d10
gpmc_a12	General-purpose memory address bit 12	O	J1	/ gpmc_d11
gpmc_a13	General-purpose memory address bit 13	O	K4	/ gpmc_d12
gpmc_a14	General-purpose memory address bit 14	O	K3	/ gpmc_d13
gpmc_a15	General-purpose memory address bit 15	O	K2	/ gpmc_d14
gpmc_a16	General-purpose memory address bit 16	O	K1	/ gpmc_d15
gpmc_a17	General-purpose memory address bit 17	O	E3	/ gpmc_d16
gpmc_a18	General-purpose memory address bit 18	O	E2	/ gpmc_a1
gpmc_a19	General-purpose memory address bit 19	O	E1	/ gpmc_a2
gpmc_a20	General-purpose memory address bit 20	O	F7	/ gpmc_a3
gpmc_a21	General-purpose memory address bit 21	O	F6	/ gpmc_a4
gpmc_a22	General-purpose memory address bit 22	O	F4	/ gpmc_a5
gpmc_a23	General-purpose memory address bit 23	O	F3	/ gpmc_a6
gpmc_a24	General-purpose memory address bit 24	O	F2	/ gpmc_a7
gpmc_a25	General-purpose memory address bit 25	O	F1	/ gpmc_a8
gpmc_a26	General-purpose memory address bit 26	O	G6	/ gpmc_a9

Table 2-3. External Memory Interfaces – GPMC Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL (ZCN Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [5]
gpmc_d0	GPMC Data bit 0	IO	G5	gpmc_a1/ gpmc_d0
gpmc_d1	GPMC Data bit 1	IO	G4	gpmc_a2/ gpmc_d1
gpmc_d2	GPMC Data bit 2	IO	G3	gpmc_a3/ gpmc_d2
gpmc_d3	GPMC Data bit 3	IO	G2	gpmc_a4/ gpmc_d3
gpmc_d4	GPMC Data bit 4	IO	G1	gpmc_a5/ gpmc_d4
gpmc_d5	GPMC Data bit 5	IO	H2	gpmc_a6/ gpmc_d5
gpmc_d6	GPMC Data bit 6	IO	H1	gpmc_a7 /gpmc_d6
gpmc_d7	GPMC Data bit 7	IO	J5	gpmc_a8/ gpmc_d7
gpmc_d8	GPMC Data bit 8	IO	J4	gpmc_a9/ gpmc_d8
gpmc_d9	GPMC Data bit 9	IO	J3	gpmc_a10/ gpmc_d9
gpmc_d10	GPMC Data bit 10	IO	J2	gpmc_a11/ gpmc_d10
gpmc_d11	GPMC Data bit 11	IO	J1	gpmc_a12/ gpmc_d11
gpmc_d12	GPMC Data bit 12	IO	K4	gpmc_a13/ gpmc_d12
gpmc_d13	GPMC Data bit 13	IO	K3	gpmc_a14/ gpmc_d13
gpmc_d14	GPMC Data bit 14	IO	K2	gpmc_a15/ gpmc_d14
gpmc_d15	GPMC Data bit 15	IO	K1	gpmc_a16/ gpmc_d15
gpmc_ncs0	GPMC Chip Select 0	O	L2	NA
gpmc_ncs1	GPMC Chip Select 1	O	L1	NA
gpmc_ncs2	GPMC Chip Select 2	O	M4	NA
gpmc_ncs3	GPMC Chip Select 3	O	M3	NA
gpmc_ncs4	GPMC Chip Select 4	O	M2	NA
gpmc_ncs5	GPMC Chip Select 5	O	M1	NA
gpmc_ncs6	GPMC Chip Select 6	O	N5	NA
gpmc_ncs7	GPMC Chip Select 7	O	N4	NA
gpmc_clk	GPMC clock	O	N1	NA
gpmc_nadv_ale	Address Valid or Address Latch Enable	O	R1	NA
gpmc_noe	Output Enable	O	R2	NA
gpmc_nwe	Write Enable	O	R3	NA
gpmc_nbe0_cle	Lower Byte Enable. Also used for Command Latch Enable	O	R4	NA
gpmc_nbe1	Upper Byte Enable	O	T1	NA
gpmc_nwp	Flash Write Protect	O	T2	NA
gpmc_wait0	External indication of wait	I	T3	NA
gpmc_wait1	External indication of wait	I	T4	NA
gpmc_wait2	External indication of wait	I	T5	NA
gpmc_wait3	External indication of wait	I	U1	NA

Table 2-4. External Memory Interfaces – SDRC Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
sdrc_d0	SDRAM data bit 0	IO	B21
sdrc_d1	SDRAM data bit 1	IO	A21
sdrc_d2	SDRAM data bit 2	IO	D20
sdrc_d3	SDRAM data bit 3	IO	C20
sdrc_d4	SDRAM data bit 4	IO	E19
sdrc_d5	SDRAM data bit 5	IO	D19

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Table 2-4. External Memory Interfaces – SDRC Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
sdrc_d6	SDRAM data bit 6	IO	C19
sdrc_d7	SDRAM data bit 7	IO	B19
sdrc_d8	SDRAM data bit 8	IO	B18
sdrc_d9	SDRAM data bit 9	IO	D17
sdrc_d10	SDRAM data bit 10	IO	C17
sdrc_d11	SDRAM data bit 11	IO	D16
sdrc_d12	SDRAM data bit 12	IO	C16
sdrc_d13	SDRAM data bit 13	IO	B16
sdrc_d14	SDRAM data bit 14	IO	A16
sdrc_d15	SDRAM data bit 15	IO	A15
sdrc_d16	SDRAM data bit 16	IO	A7
sdrc_d17	SDRAM data bit 17	IO	B7
sdrc_d18	SDRAM data bit 18	IO	D7
sdrc_d19	SDRAM data bit 19	IO	E7
sdrc_d20	SDRAM data bit 20	IO	C6
sdrc_d21	SDRAM data bit 21	IO	D6
sdrc_d22	SDRAM data bit 22	IO	B5
sdrc_d23	SDRAM data bit 23	IO	C5
sdrc_d24	SDRAM data bit 24	IO	B4
sdrc_d25	SDRAM data bit 25	IO	A3
sdrc_d26	SDRAM data bit 26	IO	B3
sdrc_d27	SDRAM data bit 27	IO	C3
sdrc_d28	SDRAM data bit 28	IO	C2
sdrc_d29	SDRAM data bit 29	IO	D2
sdrc_d30	SDRAM data bit 30	IO	B1
sdrc_d31	SDRAM data bit 31	IO	C1
sdrc_ba0	SDRAM bank select 0	O	A12
sdrc_ba1	SDRAM bank select 1	O	C13
sdrc_ba2	SDRAM bank select 1	O	D13
sdrc_a0	SDRAM address bit 0	O	A11
sdrc_a1	SDRAM address bit 1	O	B11
sdrc_a2	SDRAM address bit 2	O	C11
sdrc_a3	SDRAM address bit 3	O	D11
sdrc_a4	SDRAM address bit 4	O	E11
sdrc_a5	SDRAM address bit 5	O	A10
sdrc_a6	SDRAM address bit 6	O	B10
sdrc_a7	SDRAM address bit 7	O	C10
sdrc_a8	SDRAM address bit 8	O	D10
sdrc_a9	SDRAM address bit 9	O	E10
sdrc_a10	SDRAM address bit 10	O	A9
sdrc_a11	SDRAM address bit 11	O	B9
sdrc_a12	SDRAM address bit 12	O	A8
sdrc_a13	SDRAM address bit 13	O	B8
sdrc_a14	SDRAM address bit 14	O	D8
sdrc_ncs0	Chip select 0	O	E13
sdrc_ncs1	Chip select 1	O	A14

Table 2-4. External Memory Interfaces – SDRC Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
sdrc_clk	Clock	IO	A13
sdrc_nclk	Clock Invert	O	B13
sdrc_cke0	Clock Enable 0	O	D14
sdrc_nras	SDRAM Row Access	O	C14
sdrc_ncas	SDRAM column address strobe	O	E14
sdrc_nwe	SDRAM write enable	O	B14
sdrc_dm0	Data Mask 0	O	C21
sdrc_dm1	Data Mask 1	O	B15
sdrc_dm2	Data Mask 2	O	E8
sdrc_dm3	Data Mask 3	O	D1
sdrc_strben0	PCB layout trace loop 0 pin 0	A	A19
sdrc_strben_dly0	PCB layout trace loop 0 pin 1	A	A18
sdrc_strben1	PCB layout trace loop 1 pin 0	A	A5
sdrc_strben_dly1	PCB layout trace loop 1 pin 1	A	A4
sdrc_odt0	On-die termination output	O	C8
sdrc_dqs0p	Data Strobe 0	IO	B20
sdrc_dqs0n	Data Strobe 0	IO	A20
sdrc_dqs1p	Data Strobe 1	IO	B17
sdrc_dqs1n	Data Strobe 1	IO	A17
sdrc_dqs2p	Data Strobe 2	IO	A6
sdrc_dqs2n	Data Strobe 2	IO	B6
sdrc_dqs3p	Data Strobe 3	IO	A2
sdrc_dqs3n	Data Strobe 3	IO	B2
ddr_padref	Impedance control for DDR2 output. This pin must be connected to ground via a 50-ohm (± 1%) resistor.	IO	B12

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2.4.2 Video Interfaces

Table 2-5. Video Interfaces – CCDC Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
ccdc_pclk	CCDC pixel clock	IO	AD2
ccdc_field	CCDC field ID signal	IO	AD1
ccdc_hd	CCDC horizontal sync	IO	AE2
ccdc_vd	CCDC vertical sync	IO	AD3
ccdc_wen	CCDC write enable	I	AE3
ccdc_data0	CCDC data bit 0	I	AD4
ccdc_data1	CCDC data bit 1	I	AE4
ccdc_data2	CCDC data bit 2	I	AC5
ccdc_data3	CCDC data bit 3	I	AD5
ccdc_data4	CCDC data bit 4	I	AE5
ccdc_data5	CCDC data bit 5	I	Y6
ccdc_data6	CCDC data bit 6	I	AB6
ccdc_data7	CCDC data bit 7	I	AC6

Table 2-6. Video Interfaces – DSS Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
dss_pclk	LCD Pixel Clock	O	AE23
dss_hsync	LCD Horizontal Synchronization	O	AD22
dss_vsync	LCD Vertical Synchronization	O	AD23
dss_acbias	AC bias control (STN) or pixel data enable (TFT) output	O	AE24
dss_data0	LCD Pixel Data bit 0	IO	AD24
dss_data1	LCD Pixel Data bit 1	IO	AD25
dss_data2	LCD Pixel Data bit 2	IO	AC23
dss_data3	LCD Pixel Data bit 3	IO	AC24
dss_data4	LCD Pixel Data bit 4	IO	AC25
dss_data5	LCD Pixel Data bit 5	IO	AB24
dss_data6	LCD Pixel Data bit 6	IO	AB25
dss_data7	LCD Pixel Data bit 7	IO	AA23
dss_data8	LCD Pixel Data bit 8	IO	AA24
dss_data9	LCD Pixel Data bit 9	IO	AA25
dss_data10	LCD Pixel Data bit 10	IO	Y22
dss_data11	LCD Pixel Data bit 11	IO	Y23
dss_data12	LCD Pixel Data bit 12	IO	Y24
dss_data13	LCD Pixel Data bit 13	IO	Y25
dss_data14	LCD Pixel Data bit 14	IO	W21
dss_data15	LCD Pixel Data bit 15	IO	W22
dss_data16	LCD Pixel Data bit 16	IO	W23
dss_data17	LCD Pixel Data bit 17	IO	W24
dss_data18	LCD Pixel Data bit 18	IO	W25
dss_data19	LCD Pixel Data bit 19	IO	V24
dss_data20	LCD Pixel Data bit 20	O	V25
dss_data21	LCD Pixel Data bit 21	O	U21
dss_data22	LCD Pixel Data bit 22	O	U22
dss_data23	LCD Pixel Data bit 23	O	U23

Table 2-7. Video Interfaces – RFBI Signals Description

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL BOTTOM (ZCN Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [5]
rfbi_a0	RFBI command/data control	O	AE24	dss_acbias
rfbi_cs0	1st LCD chip select	O	AD22	dss_hsync
rfbi_da0	RFBI data bus 0	IO	AD24	dss_data0
rfbi_da1	RFBI data bus 1	IO	AD25	dss_data1
rfbi_da2	RFBI data bus 2	IO	AC23	dss_data2
rfbi_da3	RFBI data bus 3	IO	AC24	dss_data3
rfbi_da4	RFBI data bus 4	IO	AC25	dss_data4
rfbi_da5	RFBI data bus 5	IO	AB24	dss_data5
rfbi_da6	RFBI data bus 6	IO	AB25	dss_data6
rfbi_da7	RFBI data bus 7	IO	AA23	dss_data7
rfbi_da8	RFBI data bus 8	IO	AA24	dss_data8
rfbi_da9	RFBI data bus 9	IO	AA25	dss_data9
rfbi_da10	RFBI data bus 10	IO	Y22	dss_data10

Table 2-7. Video Interfaces – RFBI Signals Description (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL BOTTOM (ZCN Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [5]
rfbi_da11	RFBI data bus 11	IO	Y23	dss_data11
rfbi_da12	RFBI data bus 12	IO	Y24	dss_data12
rfbi_da13	RFBI data bus 13	IO	Y25	dss_data13
rfbi_da14	RFBI data bus 14	IO	W21	dss_data14
rfbi_da15	RFBI data bus 15	IO	W22	dss_data15
rfbi_rd	Read enable for RFBI	O	AE23	dss_pclk
rfbi_wr	Write Enable for RFBI	O	AD23	dss_vsync
rfbi_te_vsync0	tearing effect removal and Vsync input from 1st LCD	I	W23	dss_data16
rfbi_hsync0	Hsync for 1st LCD	I	W24	dss_data17
rfbi_te_vsync1	tearing effect removal and Vsync input from 2nd LCD	I	W25	dss_data18
rfbi_hsync1	Hsync for 2nd LCD	I	V24	dss_data19
rfbi_cs1	2nd LCD chip select	O	V25	dss_data20

Table 2-8. Video Interfaces – TV Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
tv_out1	TV analog output Composite: tv_out1	O	K21
tv_out2	TV analog output S-VIDEO: tv_out2	O	H24
tv_vfb1	tv_vfb1: Feedback through external resistorto composite	O	K20
tv_vfb2	tv_vfb2: Feedback through external resistorto S-VIDEO	O	H23
tv_vref	External capacitor	I	H20

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2.4.3 Serial Communication Interfaces

Table 2-9. Serial Communication Interfaces – HDQ/1-Wire Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
hdq_sio	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.	IOD	L25

Table 2-10. Serial Communication Interfaces – I^2C Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
INTER-INTEGRATED CIRCUIT INTERFACE (I2C1)			
i2c1_scl	I^2C Master Serial clock. Output is open drain.	IOD	V4
i2c1_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	V5
INTER-INTEGRATED CIRCUIT INTERFACE (I2C2)			
i2c2_scl	I^2C Master Serial clock. Output is open drain.	IOD	W1
i2c2_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	W2
INTER-INTEGRATED CIRCUIT INTERFACE (I2C3)			
i2c3_scl	I^2C Master Serial clock. Output is open drain.	IOD	W4
i2c3_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	W5

Table 2-11. Serial Communication Interfaces – McBSP LP Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 1)			
mcbsp1_dr	Received serial data	I	P23
mcbsp1_clkr	Receive Clock	IO	R25
mcbsp1_fsr	Receive frame synchronization	IO	P21
mcbsp1_dx	Transmitted serial data	IO	P22
mcbsp1_clkx	Transmit clock	IO	N24
mcbsp1_fsx	Transmit frame synchronization	IO	P24
mcbsp_clks	External clock input (shared by McBSP1, 2, 3, 4, and 5)	I	P25
MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 2)			
mcbsp2_dr	Received serial data	I	B25
mcbsp2_dx	Transmitted serial data	IO	D24
mcbsp2_clkx	Combined serial clock	IO	C25
mcbsp2_fsx	Combined frame synchronization	IO	D25
MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 3)			
mcbsp3_dr	Received serial data	I	C24
mcbsp3_dx	Transmitted serial data	IO	B24
mcbsp3_clkx	Combined serial clock	IO	A24
mcbsp3_fsx	Combined frame synchronization	IO	C23
MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 4)			
mcbsp4_dr	Received serial data	I	A23
mcbsp4_dx	Transmitted serial data	IO	B22
mcbsp4_clkx	Combined serial clock	IO	B23
mcbsp4_fsx	Combined frame synchronization	IO	A22
MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 5)			
mcbsp5_dr	Received serial data	I	Y18
mcbsp5_dx	Transmitted serial data	IO	AD19
mcbsp5_clkx	Combined serial clock	IO	AD17
mcbsp5_fsx	Combined frame synchronization	IO	AE19

Table 2-12. Serial Communication Interfaces – McSPI Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)			
mcspi1_clk	SPI Clock	IO	AE14
mcspi1_simo	Slave data in, master data out	IO	AD15
mcspi1_somi	Slave data out, master data in	IO	AC15
mcspi1_cs0	SPI Enable 0, polarity configured by software	IO	AB15
mcspi1_cs1	SPI Enable 1, polarity configured by software	O	AD14
mcspi1_cs2	SPI Enable 2, polarity configured by software	O	AE15
mcspi1_cs3	SPI Enable 3, polarity configured by software	O	AE16
MULTICHANNEL SERIAL PORT INTERFACE (McSPI2)			
mcspi2_clk	SPI Clock	IO	AD16,AC9
mcspi2_simo	Slave data in, master data out	IO	AC16,AD9
mcspi2_somi	Slave data out, master data in	IO	AB16,AE9
mcspi2_cs0	SPI Enable 0, polarity configured by software	IO	AA16,AA10

Table 2-12. Serial Communication Interfaces – McSPI Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
mcspi2_cs1	SPI Enable 1, polarity configured by software	O	AE17
MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)			
mcspi3_clk	SPI Clock	IO	W25,AD11,AA18
mcspi3_simo	Slave data in, master data out	IO	V24,AE11,AD18
mcspi3_somi	Slave data out, master data in	IO	V25, AB12, AC18
mcspi3_cs0	SPI Enable 0, polarity configured by software	IO	U21,AE12,AB18
mcspi3_cs1	SPI Enable 1, polarity configured by software	O	U22, AD12, AB19
MULTICHANNEL SERIAL PORT INTERFACE (McSPI4)			
mcspi4_clk	SPI Clock	IO	W20, R25
mcspi4_simo	Slave data in, master data out	IO	P22
mcspi4_somi	Slave data out, master data in	IO	P23
mcspi4_cs0	SPI Enable 0, polarity configured by software	IO	P24

Table 2-13. Serial Communication Interfaces – HECC Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
HIGH-END CONTROLLER AREA NETWORK CONTROLLER (HECC)			
hecc1_txd	Transmit serial data pin	IO	V2
hecc1_rxd	Receive serial data pin	IO	V3

Table 2-14. Serial Communication Interfaces – EMAC (RMII) Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
EMAC (RMII)			
rmii_mdio_data	Management data I/O	IO	AE6
rmii_mdio_clk	Management data clock	IO	AD6
rmii_rxd0	EMAC receive data pin 0	I	Y7
rmii_rxd1	EMAC receive data pin 1	I	AA7
rmii_crs_dv	EMAC carrier sense/receive data valid	I	AB7
rmii_rxer	EMAC receive error	I	AC7
rmii_txd0	EMAC transmit data pin 0	O	AD7
rmii_txd1	EMAC transmit data pin 1	O	AE7
rmii_txen	EMAC transmit enable	O	AD8
rmii_50mhz_clk	EMAC RMII 50 MHz clock	I	AE8

Table 2-15. Serial Communication Interfaces – UARTs Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)			
uart1_cts	UART1 Clear To Send	I	AD24,Y20,P25
uart1_rts	UART1 Request To Send	O	AD25,Y19
uart1_rx	UART1 Receive data	I	AA23,W20,AC20
uart1_tx	UART1 Transmit data	O	AB25,AA19
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)			
uart2_cts	UART2 Clear To Send	I	B24,F20
uart2_rts	UART2 Request To Send	O	C24,F19

Table 2-15. Serial Communication Interfaces – UARTs Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
uart2_rx	UART2 Receive data	I	C23,E23
uart2_tx	UART2 Transmit data	O	A24,E24
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA			
uart3_cts_rctx	UART3 Clear To Send (input), Remote TX (output)	IO	U1,N2
uart3_rts_sd	UART3 Request To Send, IR enable	O	N3,V3
uart3_rx_irrx	UART3 Receive data, IR and Remote RX	I	AC25,P1,F25,V2
uart3_tx_irtx	UART3 Transmit data, IR TX	O	AB24,P2,F24,E25
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)			
uart4_cts	UART4 Clear To Send	I	AD3,AD11
uart4_rts	UART4 Request To Send	O	AE2,AE11
uart4_rx	UART4 Receive data	I	T5,AE3,AC12
uart4_tx	UART4 Transmit data	O	T4,AD1,AB12

Table 2-16. Serial Communication Interfaces – USB Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
UNIVERSAL SERIAL BUS INTERFACE (USB0)			
usb0_dp	USB D+ (differential signal pair)	A I/O/Z	F25
usb0_dm	USB D- (differential signal pair)	A I/O/Z	F24
usb0_drvvbus	Digital output to control external supply	O/Z	E25
usb0_id	USB operating mode identification pin	A I/O/Z	G25
usb0_vbus	For host or device mode operation, tie the VBUS/USB power signal to the USB connector. When used in OTG mode operation, tie VBUS to the external charge pump and to the VBUS signal on the USB connector.	A I/O/Z	G24
MM_FSUSB3			
mm_fsusb3_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AE13
mm_fsusb3_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AC13
mm_fsusb3_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	A23
mm_fsusb3_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	B23
mm_fsusb3_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	B22
mm_fsusb3_txen_n	Transmit enable	IO	A22
MM_FSUSB2			
mm_fsusb2_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AD21
mm_fsusb2_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AB20
mm_fsusb2_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	AC21
mm_fsusb2_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AE22
mm_fsusb2_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	AE16
mm_fsusb2_txen_n	Transmit enable	IO	AE17
MM_FSUSB1			
mm_fsusb1_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AD20
mm_fsusb1_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AE18
mm_fsusb1_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	AD18
mm_fsusb1_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AC18
mm_fsusb1_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	AB18
mm_fsusb1_txen_n	Transmit enable	IO	AB19
HSUSB2			

Table 2-16. Serial Communication Interfaces – USB Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
hsusb2_clk	Dedicated for external transceiver 60-MHz clock input from PHY	O	AC20
hsusb2_stp	Dedicated for external transceiver Stop signal	O	AB20
hsusb2_dir	Dedicated for external transceiver Data direction control from PHY	I	AE21
hsusb2_nxt	Dedicated for external transceiver Next signal from PHY	I	AD21
hsusb2_data0	Dedicated for external transceiver Bidirectional data bus	IO	AC21
hsusb2_data1	Dedicated for external transceiver Bidirectional data bus	IO	AE22
hsusb2_data2	Dedicated for external transceiver Bidirectional data bus	IO	AE16
hsusb2_data3	Dedicated for external transceiver Bidirectional data bus	IO	AE17
hsusb2_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AC16
hsusb2_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AB16
hsusb2_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA16
hsusb2_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AD16
HSUSB2_TLL			
hsusb2_tll_clk	Dedicated for external transceiver 60-MHz clock input from PHY	O	AC20
hsusb2_tll_stp	Dedicated for external transceiver Stop signal	I	AB20
hsusb2_tll_dir	Dedicated for external transceiver data direction control from PHY	O	AE21
hsusb2_tll_nxt	Dedicated for external transceiver Next signal from PHY	O	AD21
hsusb2_tll_data0	Dedicated for external transceiver Bidirectional data bus	IO	AC21
hsusb2_tll_data1	Dedicated for external transceiver Bidirectional data bus	IO	AE22
hsusb2_tll_data2	Dedicated for external transceiver Bidirectional data bus	IO	AE16
hsusb2_tll_data3	Dedicated for external transceiver Bidirectional data bus	IO	AE17
hsusb2_tll_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AC16
hsusb2_tll_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AB16
hsusb2_tll_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA16
hsusb2_tll_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AD16
HSUSB1			
hsusb1_clk	Dedicated for external transceiver 60-MHz clock input from PHY	O	AE18
hsusb1_stp	Dedicated for external transceiver Stop signal	O	AD17
hsusb1_dir	Dedicated for external transceiver data direction control from PHY	I	AE20
hsusb1_nxt	Dedicated for external transceiver Next signal from PHY	I	AD20
hsusb1_data0	Dedicated for external transceiver Bidirectional data bus	IO	AD18
hsusb1_data1	Dedicated for external transceiver Bidirectional data bus	IO	AC18
hsusb1_data2	Dedicated for external transceiver Bidirectional data bus	IO	AB18
hsusb1_data3	Dedicated for external transceiver Bidirectional data bus	IO	AB19
hsusb1_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y18
hsusb1_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE19
hsusb1_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AD19
hsusb1_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA18

Table 2-16. Serial Communication Interfaces – USB Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
HSUSB1_TLL			
hsusb1_tll_clk	Dedicated for external transceiver 60-MHz clock input from PHY	O	AE18
hsusb1_tll_stp	Dedicated for external transceiver Stop signal	I	AD17
hsusb1_tll_dir	Dedicated for external transceiver data direction control from PHY	O	AE20
hsusb1_tll_nxt	Dedicated for external transceiver Next signal from PHY	O	AD20
hsusb1_tll_data0	Dedicated for external transceiver Bidirectional data bus	IO	AD18
hsusb1_tll_data1	Dedicated for external transceiver Bidirectional data bus	IO	AC18
hsusb1_tll_data2	Dedicated for external transceiver Bidirectional data bus	IO	AB18
hsusb1_tll_data3	Dedicated for external transceiver Bidirectional data bus	IO	AB19
hsusb1_tll_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y18
hsusb1_tll_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE19
hsusb1_tll_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AD19
hsusb1_tll_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA18

2.4.4 Removable Media Interfaces

Table 2-17. Removable Media Interfaces – MMC/SDIO Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
MULTIMEDIA MEMORY CARD (MMC1) / SECURE DIGITAL IO (SDIO1)			
mmc1_clk	MMC/SD Output Clock	O	AA9
mmc1_cmd	MMC/SD command signal	IO	AB9
mmc1_dat0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	AC9
mmc1_dat1	MMC/SD Card Data bit 1	IO	AD9
mmc1_dat2	MMC/SD Card Data bit 2	IO	AE9
mmc1_dat3	MMC/SD Card Data bit 3	IO	AA10
mmc1_dat4	MMC/SD Card Data bit 4	IO	AB10
mmc1_dat5	MMC/SD Card Data bit 5	IO	AC10
mmc1_dat6	MMC/SD Card Data bit 6	IO	AD10
mmc1_dat7	MMC/SD Card Data bit 7	IO	AE10
MULTIMEDIA MEMORY CARD (MMC2) / SECURE DIGITAL IO (SDIO2)			
mmc2_clk	MMC/SD Output Clock	O	AD11
mmc2_dir_dat0	Direction control for DAT0 signal case an external transceiver used	O	AB13
mmc2_dir_dat1	Direction control for DAT1 and DAT3 signals case an external transceiver used	O	AC13
mmc2_dir_dat2	Direction control for DAT2 signal case an external transceiver used	O	AB1
mmc2_dir_dat3	Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used	O	AB2
mmc2_clkin	MMC/SD input Clock	I	AE13
mmc2_dat0	MMC/SD Card Data bit 0	IO	AB12
mmc2_dat1	MMC/SD Card Data bit 1	IO	AC12
mmc2_dat2	MMC/SD Card Data bit 2	IO	AD12
mmc2_dat3	MMC/SD Card Data bit 3	IO	AE12
mmc2_dat4	MMC/SD Card Data bit 4	IO	AB13

Table 2-17. Removable Media Interfaces – MMC/SDIO Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
mmc2_dat5	MMC/SD Card Data bit 5	IO	AC13
mmc2_dat6	MMC/SD Card Data bit 6	IO	AD13
mmc2_dat7	MMC/SD Card Data bit 7	IO	AE13
mmc2_dir_cmd	Direction control for CMD signal case an external transceiver is used	O	AD13
mmc2_cmd	MMC/SD command signal	IO	AE11
MULTIMEDIA MEMORY CARD (MMC3) / SECURE DIGITAL IO (SDIO3)			
mmc3_clk	MMC/SD Output Clock	O	AD15,AE17
mmc3_cmd	MMC/SD command signal	IO	AD14,AE18
mmc3_dat0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	AB13,Y18
mmc3_dat1	MMC/SD Card Data bit 1	IO	AC13,AE19
mmc3_dat2	MMC/SD Card Data bit 2	IO	AD13,AD19
mmc3_dat3	MMC/SD Card Data bit 3	IO	AE13,AA18
mmc3_dat4	MMC/SD Card Data bit 4	IO	AD18
mmc3_dat5	MMC/SD Card Data bit 5	IO	AD20
mmc3_dat6	MMC/SD Card Data bit 6	IO	AE20
mmc3_dat7	MMC/SD Card Data bit 7	IO	AB19

2.4.5 Test Interfaces

Table 2-18. Test Interfaces – ETK Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
etk_ctl	ETK trace ctl	O	AE18
etk_clk	ETK trace clock	O	AD17
etk_d0	ETK data 0	O	AD18
etk_d1	ETK data 1	O	AC18
etk_d2	ETK data 2	O	AB18
etk_d3	ETK data 3	O	AA18
etk_d4	ETK data 4	O	Y18
etk_d5	ETK data 5	O	AE19
etk_d6	ETK data 6	O	AD19
etk_d7	ETK data 7	O	AB19
etk_d8	ETK data 8	O	AE20
etk_d9	ETK data 9	O	AD20
etk_d10	ETK data 10	O	AC20
etk_d11	ETK data 11	O	AB20
etk_d12	ETK data 12	O	AE21
etk_d13	ETK data 13	O	AD21
etk_d14	ETK data 14	O	AC21
etk_d15	ETK data 15	O	AE22

Table 2-19. Test Interfaces – JTAG Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
jtag_ntrst	Test Reset	I	U24
jtag_tck	Test Clock	I	U25
jtag_rtck	ARM Clock Emulation	O	T21
jtag_tms_tmsc	Test Mode Select	IO	T22
jtag_tdi	Test Data Input	I	T23
jtag_tdo	Test Data Output	O	T24
jtag_emu0	Test emulation 0	IO	T25
jtag_emu1	Test emulation 1	IO	R24

Table 2-20. Test Interfaces – HWDBG Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
hw_dbg0	Debug signal 0	O	AD2,AD17
hw_dbg1	Debug signal 1	O	AD1,AE18
hw_dbg2	Debug signal 2	O	AD3,AD18
hw_dbg3	Debug signal 3	O	AE3,AC18
hw_dbg4	Debug signal 4	O	AC5,AC18
hw_dbg5	Debug signal 5	O	AD5,AA18
hw_dbg6	Debug signal 6	O	Y18,AE5
hw_dbg7	Debug signal 7	O	Y6,AE19
hw_dbg8	Debug signal 8	O	Y7,AD19
hw_dbg9	Debug signal 9	O	AA7,AB19

Table 2-20. Test Interfaces – HWDBG Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
hw_dbg10	Debug signal 10	O	AC7,AE20
hw_dbg11	Debug signal 11	O	AD7,AD20
hw_dbg12	Debug signal 12	O	AE23,AC20
hw_dbg13	Debug signal 13	O	AD22,AB20
hw_dbg14	Debug signal 14	O	AB25,AE21
hw_dbg15	Debug signal 15	O	AA23,AD21
hw_dbg16	Debug signal 16	O	AA24,AC21
hw_dbg17	Debug signal 17	O	AA25,AE22

2.4.6 Miscellaneous

Table 2-21. Miscellaneous – GP Timer Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
gpt8_pwm_evt	PWM or event for GP timer 8	IO	N4,E23,AE17
gpt9_pwm_evt	PWM or event for GP timer 9	IO	M4,M2,F20,AC16
gpt10_pwm_evt	PWM or event for GP timer 10	IO	M3,M1,F19,AB16
gpt11_pwm_evt	PWM or event for GP timer 11	IO	N5,E24,AA16,AA12

2.4.7 General-Purpose IOs

Table 2-22. General-Purpose IOs Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
gpio_0	General-purpose IO 0	IO	Y1
gpio_1	General-purpose IO 1	IO	M24
gpio_2	General-purpose IO 2	IO	Y4
gpio_3	General-purpose IO 3	IO	AA1
gpio_4	General-purpose IO 4	IO	AA2
gpio_5	General-purpose IO 5	IO	AA3
gpio_6	General-purpose IO 6	IO	AB1
gpio_7	General-purpose IO 7	IO	AB2
gpio_8	General-purpose IO 8	IO	AC1
gpio_10	General-purpose IO 10	IO	N25
gpio_11	General-purpose IO 11	IO	T25
gpio_12	General-purpose IO 12	IO	AD17
gpio_13	General-purpose IO 13	IO	AE18
gpio_14	General-purpose IO 14	IO	AD18
gpio_15	General-purpose IO 15	IO	AC18
gpio_16	General-purpose IO 16	IO	AB18
gpio_17	General-purpose IO 17	IO	AA18
gpio_18	General-purpose IO 18	IO	Y18
gpio_19	General-purpose IO 19	IO	AE19
gpio_20	General-purpose IO 20	IO	AD19
gpio_21	General-purpose IO 21	IO	AB19
gpio_22	General-purpose IO 22	IO	AE20
gpio_23	General-purpose IO 23	IO	AD20
gpio_24	General-purpose IO 24	IO	AC20
gpio_25	General-purpose IO 25	IO	AB20
gpio_26	General-purpose IO 26	IO	AE21
gpio_27	General-purpose IO 27	IO	AD21
gpio_28	General-purpose IO 28	IO	AC21
gpio_29	General-purpose IO 29	IO	AE22
gpio_30	General-purpose IO 30	IO	Y3
gpio_31	General-purpose IO 31	IO	R24
gpio_34	General-purpose IO 34	IO	E3
gpio_35	General-purpose IO 35	IO	E2
gpio_36	General-purpose IO 36	IO	E1
gpio_37	General-purpose IO 37	IO	F7
gpio_38	General-purpose IO 38	IO	F6
gpio_39	General-purpose IO 39	IO	F4
gpio_40	General-purpose IO 40	IO	F3
gpio_41	General-purpose IO 41	IO	F2
gpio_42	General-purpose IO 42	IO	F1
gpio_43	General-purpose IO 43	IO	G6
gpio_44	General-purpose IO 44	IO	J4
gpio_45	General-purpose IO 45	IO	J3
gpio_46	General-purpose IO 46	IO	J2

Table 2-22. General-Purpose IOs Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
gpio_47	General-purpose IO 47	IO	J1
gpio_48	General-purpose IO 48	IO	K4
gpio_49	General-purpose IO 49	IO	K3
gpio_50	General-purpose IO 50	IO	K2
gpio_51	General-purpose IO 51	IO	K1
gpio_52	General-purpose IO 52	IO	L1
gpio_53	General-purpose IO 53	IO	M4
gpio_54	General-purpose IO 54	IO	M3
gpio_55	General-purpose IO 55	IO	M2
gpio_56	General-purpose IO 56	IO	M1
gpio_57	General-purpose IO 57	IO	N5
gpio_58	General-purpose IO 58	IO	N4
gpio_59	General-purpose IO 59	IO	N1
gpio_60	General-purpose IO 60	IO	R4
gpio_61	General-purpose IO 61	IO	T1
gpio_62	General-purpose IO 62	IO	T2
gpio_63	General-purpose IO 63	IO	T4
gpio_64	General-purpose IO 64	IO	T5
gpio_65	General-purpose IO 65	IO	U1
gpio_66	General-purpose IO 66	IO	AE23
gpio_67	General-purpose IO 67	IO	AD22
gpio_68	General-purpose IO 68	IO	AD23
gpio_69	General-purpose IO 69	IO	AE24
gpio_70	General-purpose IO 70	IO	AD24
gpio_71	General-purpose IO 71	IO	AD25
gpio_72	General-purpose IO 72	IO	AC23
gpio_73	General-purpose IO 73	IO	AC24
gpio_74	General-purpose IO 74	IO	AC25
gpio_75	General-purpose IO 75	IO	AB24
gpio_76	General-purpose IO 76	IO	AB25
gpio_77	General-purpose IO 77	IO	AA23
gpio_78	General-purpose IO 78	IO	AA24
gpio_79	General-purpose IO 79	IO	AA25
gpio_80	General-purpose IO 80	IO	Y22
gpio_81	General-purpose IO 81	IO	Y23
gpio_82	General-purpose IO 82	IO	Y24
gpio_83	General-purpose IO 83	IO	Y25
gpio_84	General-purpose IO 84	IO	W21
gpio_85	General-purpose IO 85	IO	W22
gpio_86	General-purpose IO 86	IO	W23
gpio_87	General-purpose IO 87	IO	W24
gpio_88	General-purpose IO 88	IO	W25
gpio_89	General-purpose IO 89	IO	V24
gpio_90	General-purpose IO 90	IO	V25
gpio_91	General-purpose IO 91	IO	U21
gpio_92	General-purpose IO 92	IO	U22

Table 2-22. General-Purpose IOs Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
gpio_93	General-purpose IO 93	IO	U23
gpio_94	General-purpose IO 94	IO	AD2
gpio_95	General-purpose IO 95	IO	AD1
gpio_96	General-purpose IO 96	IO	AE2
gpio_97	General-purpose IO 97	IO	AD3
gpio_98	General-purpose IO 98	IO	AE3
gpio_99	General-purpose IO 99	I	AD4
gpio_100	General-purpose IO 100	I	AE4
gpio_101	General-purpose IO 101	IO	AC5
gpio_102	General-purpose IO 102	IO	AD5
gpio_103	General-purpose IO 103	IO	AE5
gpio_104	General-purpose IO 104	IO	Y6
gpio_105	General-purpose IO 105	IO	AB6
gpio_106	General-purpose IO 106	IO	AC6
gpio_107	General-purpose IO 107	IO	AE6
gpio_108	General-purpose IO 108	IO	AD6
gpio_109	General-purpose IO 109	IO	Y7
gpio_110	General-purpose IO 110	IO	AA7
gpio_111	General-purpose IO 111	IO	AB7
gpio_112	General-purpose IO 112	I	AE7
gpio_113	General-purpose IO 113	I	AD8
gpio_114	General-purpose IO 114	I	AE8
gpio_116	General-purpose IO 116	IO	D25
gpio_117	General-purpose IO 117	IO	C25
gpio_118	General-purpose IO 118	IO	B25
gpio_119	General-purpose IO 119	IO	D24
gpio_120	General-purpose IO 120	IO	AA9
gpio_121	General-purpose IO 121	IO	AB9
gpio_122	General-purpose IO 122	IO	AC9
gpio_123	General-purpose IO 123	IO	AD9
gpio_124	General-purpose IO 124	IO	AE9
gpio_125	General-purpose IO 125	IO	AA10
gpio_126	General-purpose IO 126	IO	AB10
gpio_127	General-purpose IO 127	IO	AC10
gpio_128	General-purpose IO 128	IO	AD10
gpio_129	General-purpose IO 129	IO	AE10
gpio_130	General-purpose IO 130	IO	AD11
gpio_131	General-purpose IO 131	IO	AE11
gpio_132	General-purpose IO 132	IO	AB12
gpio_133	General-purpose IO 133	IO	AC12
gpio_134	General-purpose IO 134	IO	AD12
gpio_135	General-purpose IO 135	IO	AE12
gpio_136	General-purpose IO 136	IO	AB13
gpio_137	General-purpose IO 137	IO	AC13
gpio_138	General-purpose IO 138	IO	AD13
gpio_139	General-purpose IO 139	IO	AE13

Table 2-22. General-Purpose IOs Signals Description (ZCN Pkg.) (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
gpio_140	General-purpose IO 140	IO	B24
gpio_141	General-purpose IO 141	IO	C24
gpio_142	General-purpose IO 142	IO	A24
gpio_143	General-purpose IO 143	IO	C23
gpio_144	General-purpose IO 144	IO	F20
gpio_145	General-purpose IO 145	IO	F19
gpio_146	General-purpose IO 146	IO	E24
gpio_147	General-purpose IO 147	IO	E23
gpio_148	General-purpose IO 148	IO	AA19
gpio_149	General-purpose IO 149	IO	Y19
gpio_150	General-purpose IO 150	IO	Y20
gpio_151	General-purpose IO 151	IO	W20
gpio_152	General-purpose IO 152	IO	B23
gpio_153	General-purpose IO 153	IO	A23
gpio_154	General-purpose IO 154	IO	B22
gpio_155	General-purpose IO 155	IO	A22
gpio_156	General-purpose IO 156	IO	R25
gpio_157	General-purpose IO 157	IO	P21
gpio_158	General-purpose IO 158	IO	P22
gpio_159	General-purpose IO 159	IO	P23
gpio_160	General-purpose IO 160	IO	P25
gpio_161	General-purpose IO 161	IO	P24
gpio_162	General-purpose IO 162	IO	N24
gpio_163	General-purpose IO 163	IO	N2
gpio_164	General-purpose IO 164	IO	N3
gpio_165	General-purpose IO 165	IO	P1
gpio_166	General-purpose IO 166	IO	P2
gpio_167	General-purpose IO 167	IO	AC7
gpio_168	General-purpose IO 168	IO	W1
gpio_170	General-purpose IO 170	IO	L25
gpio_171	General-purpose IO 171	IO	AE14
gpio_172	General-purpose IO 172	IO	AD15
gpio_173	General-purpose IO 173	IO	AC15
gpio_174	General-purpose IO 174	IO	AB15
gpio_175	General-purpose IO 175	IO	AD14
gpio_176	General-purpose IO 176	IO	AE15
gpio_177	General-purpose IO 177	IO	AE16
gpio_178	General-purpose IO 178	IO	AD16
gpio_179	General-purpose IO 179	IO	AC16
gpio_180	General-purpose IO 180	IO	AB16
gpio_181	General-purpose IO 181	IO	AA16
gpio_182	General-purpose IO 182	IO	AE17
gpio_183	General-purpose IO 183	IO	W2
gpio_184	General-purpose IO 184	IO	W4
gpio_185	General-purpose IO 185	IO	W5
gpio_186	General-purpose IO 186	IO	M25

2.4.8 System and Miscellaneous Terminals

Table 2-23. System and Miscellaneous Signals Description (ZCN Pkg.)

SIGNAL NAME[1]	DESCRIPTION[2]	TYPE[3]	BALL (ZCN Pkg.) [4]
sys_32k	32-kHz clock input	I	K24
sys_xtalin	Main input clock. Oscillator input or LVCMOS at 19.2, 13, or 12 MHz.	I	K25
sys_xtalout	Output of oscillator	O	H25
sys_altclk	Alternate clock source selectable for GPTIMERs (maximum 54 MHz), USB (48 MHz), or NTSC/PAL (54 MHz)	I	L25
sys_clkreq	Request from device for system clock (open source type)	IO	M24
sys_clkout1	Configurable output clock1	O	N25
sys_clkout2	Configurable output clock2	O	M25
sys_boot0	Boot configuration mode bit 0	I	Y4
sys_boot1	Boot configuration mode bit 1	I	AA1
sys_boot2	Boot configuration mode bit 2	I	AA2
sys_boot3	Boot configuration mode bit 3	I	AA3
sys_boot4	Boot configuration mode bit 4	I	AB1
sys_boot5	Boot configuration mode bit 5	I	AB2
sys_boot6	Boot configuration mode bit 6	I	AC1
sys_boot7	Boot configuration mode bit 7	I	AC2
sys_boot8	Boot configuration mode bit 8	I	AC3
sys_nrespwron	Power On Reset	I	Y2
sys_nreswarm	Warm Boot Reset (open drain output)	IOD	Y3
sys_nirq	External FIQ input	I	Y1
sys_ndmareq0	External DMA request 0 (system expansion). Level (active low) or edge (falling) selectable.	I	M3
sys_ndmareq1	External DMA request 1 (system expansion). Level (active low) or edge (falling) selectable.	I	M2,U1
sys_ndmareq2	External DMA request 2 (system expansion). Level (active low) or edge (falling) selectable.	I	F1,M1
sys_ndmareq3	External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.	I	G6,N5

2.4.9 Power Supplies

Table 2-24. Power Supplies Description

SIGNAL NAME[1]	DESCRIPTION[2]	BALL (ZCN Pkg.) [4]
VDD_CORE	1.2-V core and oscillator macros power supply.	V16, V15, V11, V10, U16, U15, U11, U10, T18, T17, T9, T8, R18, R17, R9, R8, M18, L18, L9, L8, K18, K17, K9, K8, J16, J15, J11, J10, H15, H11, H10
VSS	Core and I/O common ground.	AE25, AE1, V18, V17, V14, V13, V12, V9, V8, U18, U17, U14, U13, U12, U9, U8, T14, T13, T12, R16, R15, R14, R13, R12, R11, R10, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, N18, N17, N14, N13, N12, N9, N8, M17, M16, M15, M14, M13,M12, M11, M10, M9, M8, L17, L16, L15, L14, L13, L12, L11, L10, K14, K13, K12, J18, J17, J14, J13, J12, J9, J8, H14, H13, H12, H9, A25, A1, N23, G20, G21
VDDS_SRAM_MPU	1.8-V MPU SLDO analog power supply.	AA13
VDDS_SRAM_CORE_BG	1.8-V Core SLDO and VDDA of BandGap analog power supply.	E17
CAP_VDD_SRAM_MPU	1.2-V SRAMOUT for MPU SLDO. For proper device operation, connect to a 1µF decoupling capacitor.	AA12
CAP_VDD_SRAM_CORE	1.2-V SRAMOUT for Core SLDO. For proper device operation, connect to a 1µF decoupling capacitor.	E16
VDDS_DPLL_MPU_USBHOST	1.8-V MPUSS DPLL and USBHOST DPLL analog power supply.	AA15
VDDS_DPLL_PER_CORE	1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER analog power supply.	N20
VDDA_DAC	1.8-V DAC analog power supply.	H21
VSSA_DAC	DAC analog ground.	H22
VDDA3P3V_USBPHY	3.3-V USB transceiver analog power supply.	F23
VDDA1P8V_USBPHY	1.8-V USB transceiver power supply.	G22
CAP_VDDA1P2LDO_USBPHY	Output of the 1.2-V internal LDO. For proper device operation, connect a 0.22uF capacitor between this pin and VSSA.	F22
VDDSHV	1.8/3.3-V power supply.	Y16, Y15, Y13, Y12, Y10, W16, W15, W13, W12,W10, W9, W6, V7, V6, U19, T20, T19, T7, T6, R7, R6, P20, P19, N19, N7, N6, M7, M6, M5, L19, K19, K7, K6, K5, J7, H18, H17
VDDS	1.8-V power supply.	Y9, W18, U20, R5, H16, H8, G17, G16, G14, G13, G11, G10, G8, F16, F13, F11, F10, F8, N22

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Table 2-24. Power Supplies Description (continued)

SIGNAL NAME[1]	DESCRIPTION[2]	BALL (ZCN Pkg.) [4]
VREFSSTL	0.9-V DDR data PHY0 reference voltage input.	F14
VDDSOSC	1.8-V oscillator power supply.	L20

3 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Ratings

The following table specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes:

- Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.
- The AM3517/05 device adheres to EIA/JESD22–A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Minimum pass level for HBM is 2 kV.

Table 3-1. Absolute Maximum Ratings Over Operating Junction Temperature Range

PARAMETER			MIN	MAX	UNIT
VDD_CORE	Supply voltage range for core macros		0.5	1.6	V
VDDS	Second supply voltage range for 1.8-V I/O macros		0.5	2.25	V
VDDSHV	Supply voltage range for 1.8/3.3V I/O macros		TBD	TBD	V
VDDS_SRAM_MPU	Analog Supply voltage range for 1.8-V MPU SLDO		TBD	TBD	V
VDDS_SRAM_CORE_BG	Analog Supply voltage range for 1.8-V Core SLDO and VDDA of BandGap		TBD	TBD	V
VDDS_DPLL_MPU_USBHOST	Analog power supply for 1.8-V MPUSS DPLL and USBHOST DPLL		TBD	TBD	V
VDDS_DPLL_PER_CORE	Analog power supply for 1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER		TBD	TBD	V
VDDA_DAC	Analog Power Supply for 1.8-V DAC		TBD	TBD	V
VDDA3P3V_USBPHY	Analog power supply for 3.3-V USB transceiver		TBD	TBD	V
VDDA1P8V_USBPHY	Power Supply for 1.8-V USB transceiver		TBD	TBD	V
VDDSOSC	Power Supply for 1.8-V oscillator		TBD	TBD	V
V_{PAD}	Voltage range at PAD		0.5	Vdds + 0.5	V
vdda	Supply voltage range for analog macros		0.5	2.43	V
V_{ESD}	ESD stress voltage(1)	HBM (human body model)(2)		TBD	V
		CDM (charged device model)(3)		TBD	
I_{IOI}	Current-pulse injection on each I/O pin(4)			200	mA
I_{clamp}	Clamp current for an input or output		20	20	mA
T_{stg}	Storage temperature range(5)		65	150	C

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
(2) JEDEC JESD22–A114 D with the following exception-no connect pins are not stressed. 2000V Human Body Model (HBM)
(3) JEDEC JESD22–C101C with the following exception-split out pin groupings to eliminate cumulative stress effect
(4) Each device is tested with I/O pin injection of 200 mA with a stress voltage of 1.5 times maximum vdd at room temperature.
(5) These temperatures extreme do not simulate actual operating conditions but exaggerate any faults that might exist.

The supply voltages and power consumption estimates are detailed in Table 3-2.

Table 3-2. Estimated Power Consumption at Ball Level

SIGNAL NAME	DESCRIPTION	MAX CURRENT (mA)
VDD_CORE	1.2-V core and oscillator macros power supply	1500 mA

Table 3-2. Estimated Power Consumption at Ball Level (continued)

VDDS_SRAM_MPU	1.8-V MPU SLDO analog power supply	40 mA
VDDS_SRAM_CORE_BG	1.8-V Core SLDO and VDDA of BandGap analog power supply	40 mA
VDDS_DPLL_MPU_USBHOST	1.8-V MPUSS DPLL and USBHOST DPLL analog power supply	25 mA
VDDS_DPLL_PER_CORE	1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER analog power supply	25 mA
VDDA_DAC	1.8-V DAC analog power supply	65 mA
VDDA3P3V_USBPHY	3.3-V USB transceiver analog power supply	10 mA
VDDA1P8V_USBPHY	1.8-V USB transceiver power supply	50 mA
VDDSHV	3.3-/1.8-V power supply	300 mA
VDDS	1.8-V power supply	200 mA
VDDSOSC	1.8-V oscillator power supply	20 mA

3.2 Recommended Operating Conditions

All AM3517/05 modules are used under the operating conditions contained in Table 3-3.

Note: Logic functions and parameter values are not assured if the device is operated out of the range specified in the recommended operating conditions.

Table 3-3. Recommended Operating Conditions

PARAMETER	DESCRIPTION		NOM	UNIT
VDD_CORE	Core and oscillator macros power supply.		1.2	V
VSS	Core and I/O common ground.		0	V
VDDS_SRAM_MPU	MPU SLDO analog power supply.		1.8	V
VDDS_SRAM_CORE_BG	Core SLDO and VDDA of BandGap analog power supply.		1.8	V
VDDS_DPLL_MPU_USBHOST	MPUSS DPLL and USBHOST DPLL analog power supply.		1.8	V
VDDS_DPLL_PER_CORE	DPLL and HSDIVIDER/ CORE and HSDIVIDER analog power supply		1.8	V
VDDA_DAC	DAC analog power supply.		1.8	V
VSSA_DAC	DAC analog ground.		0	V
VDDA3P3V_USBPHY	USB transceiver analog power supply.		3.3	V
VDDSHV	3.3-/1.8-V power supply.		3.3/1.8	V
VDDS	1.8-V power supply.		1.8	V
T_J	Operating junction temperature range	Commercial Temperature	TBD	°C
		Extended Temperature	TBD	°C
T_J	Operating junction temperature range	Commercial Temperature	TBD	°C
		Extended Temperature	TBD	°C

PRODUCT PREVIEW

Figure 3-1 illustrates the power domains:

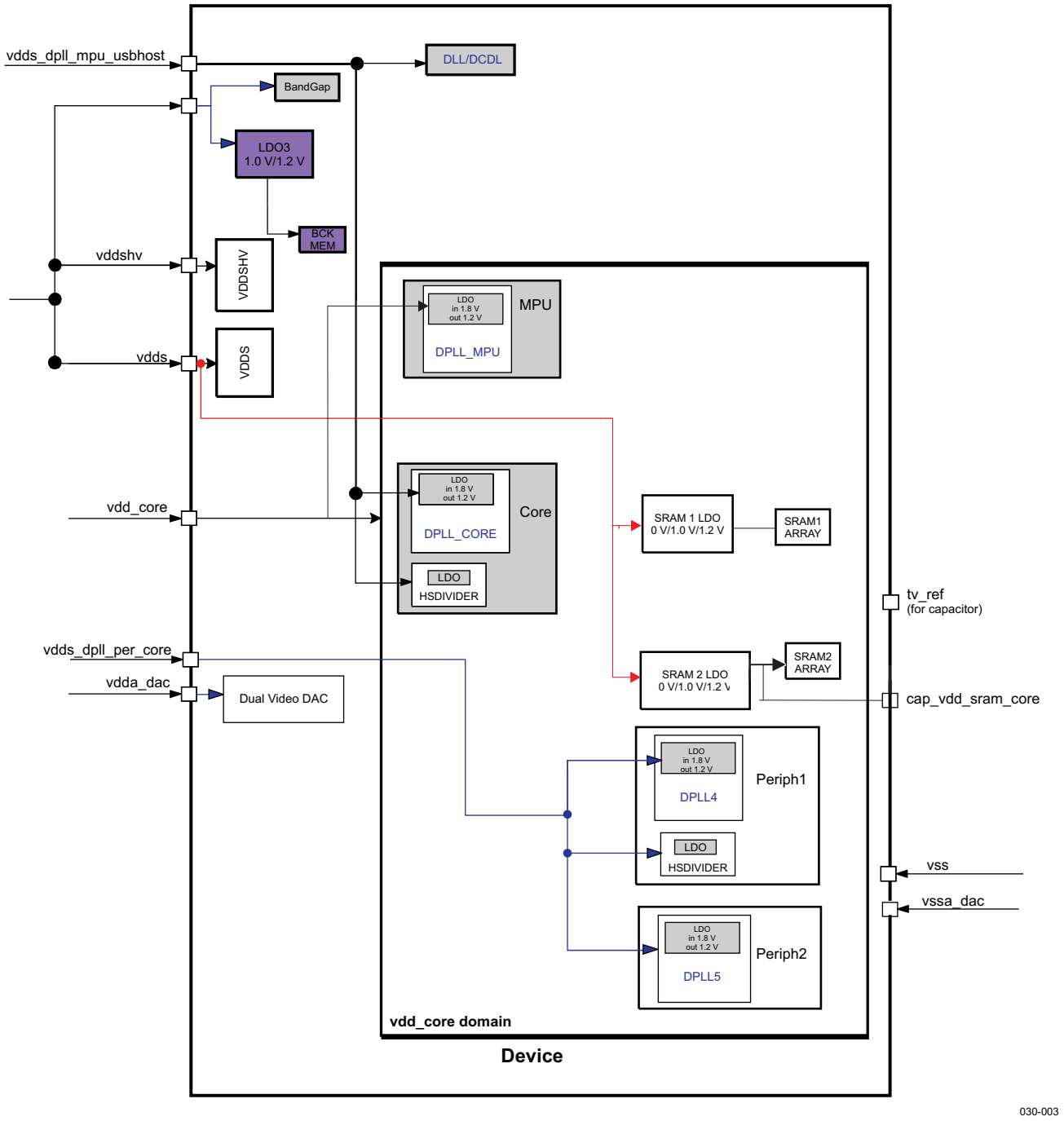


Figure 3-1. AM3517/05 Voltage Domains

3.3 DC Electrical Characteristics

Table 3-4 summarizes the dc electrical characteristics.

Table 3-4. DC Electrical Characteristics(1)

PARAMETER			MIN	NOM	MAX	UNIT
LVCMOS Pin Buffers						
V_{IH}	High-level input voltage	vddshv = 1.8 V	0.6 x vddshv		vddshv + 0.3	V
		vddshv = 3.3 V	0.6 x vddshv		vddshv + 0.3	
V_{IL}	Low-level input voltage	vddshv = 1.8 V	TBD		0.3 x vddshv	V
		vddshv = 3.3 V	TBD		0.6	
V_{OH}	High-level output voltage(2)	vddshv = 1.8 V	vddshv x 0.2			V
		vddshv = 3.3 V	0.75 x vddshv			
V_{OL}	Low-level output voltage(2)	vddshv = 1.8 V			0.2	V
		vddshv = 3.3 V			0.125 x vddshv	
t_T	Input transition time (rise time, t_R or fall time, t_F evaluated between 10% and 90% at PAD)				10	ns
I_I	Input current with $V_I = V_I$ max		TBD		TBD	A
I_{OZ}	Off-state output current for output in high impedance with driver only, driver disabled		TBD		TBD	A
	Off-state output current for output in high impedance with driver/receiver/pullup only, driver disabled, pullup not inhibited			TBD		
	Off-state output current for output in high impedance with driver/receiver/pulldown only, driver disabled, pulldown not inhibited			TBD		
I_Z	Total leakage current through the PAD connection of a driver/receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		TBD		TBD	A
LVCMOS Open-Drain Pin Buffers Dedicated to I2C IOs						
V_{IH}	High level input voltage		TBD		TBD	V
V_{IL}	Low level input voltage		TBD		0.6	V
V_{OL}	Low-level output voltage open-drain at 3-mA sink current		TBD		TBD	V
I_I	Input current at each I/O pin with an input voltage between 0.1 x vddshv to 0.9 x vddshv		TBD		TBD	A
C_I	Capacitance for each I/O pin				TBD	pF
T_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 10 pF to 400 pF	Fast mode	TBD		TBD	ns
		Standard mode			TBD	
	Output fall time with a capacitive load from 10 pF to 100 pF at 3-mA sink current	High-speed mode	TBD		TBD	
	Output fall time with a capacitive load of 400 pF at 3-mA sink current		TBD		TBD	
	Output fall time with a capacitive load of 40 pF (for CBUS compatibility)				TBD	
Complex IO Dedicated to USB						
V_{IH}	High-level input voltage		TBD		TBD	V
V_{IL}	Low-level input voltage		TBD		0.6	V
V_{OH}	High-level output voltage at 4-mA sink current		TBD			V
V_{OL}	Low-level output voltage at 4-mA sink current				TBD	V
I_I	Input current at each I/O pin with an input voltage between 0.1 x vddshv to 0.9 x vddshv		TBD		TBD	A
C_I	Capacitance for each I/O pin				TBD	pF

(1) Values are subject to change after characterization.
(2) With 100 A sink / source current at vddsxmin.

Table 3-4. DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
T_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 10 pF to 400 pF	Fast mode	TBD		TBD	ns
		Standard mode			TBD	
	Output fall time with a capacitive load from 10 pF to 100 pF at 3-mA sink current	High-speed mode	TBD		TBD	
	Output fall time with a capacitive load of 400 pF at 3-mA sink current		TBD		TBD	
	Output fall time with a capacitive load of 40 pF (for CBUS compatibility)				TBD	

3.4 Core Voltage Decoupling

For module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device because this minimizes the inductance of the circuit board wiring and interconnects.

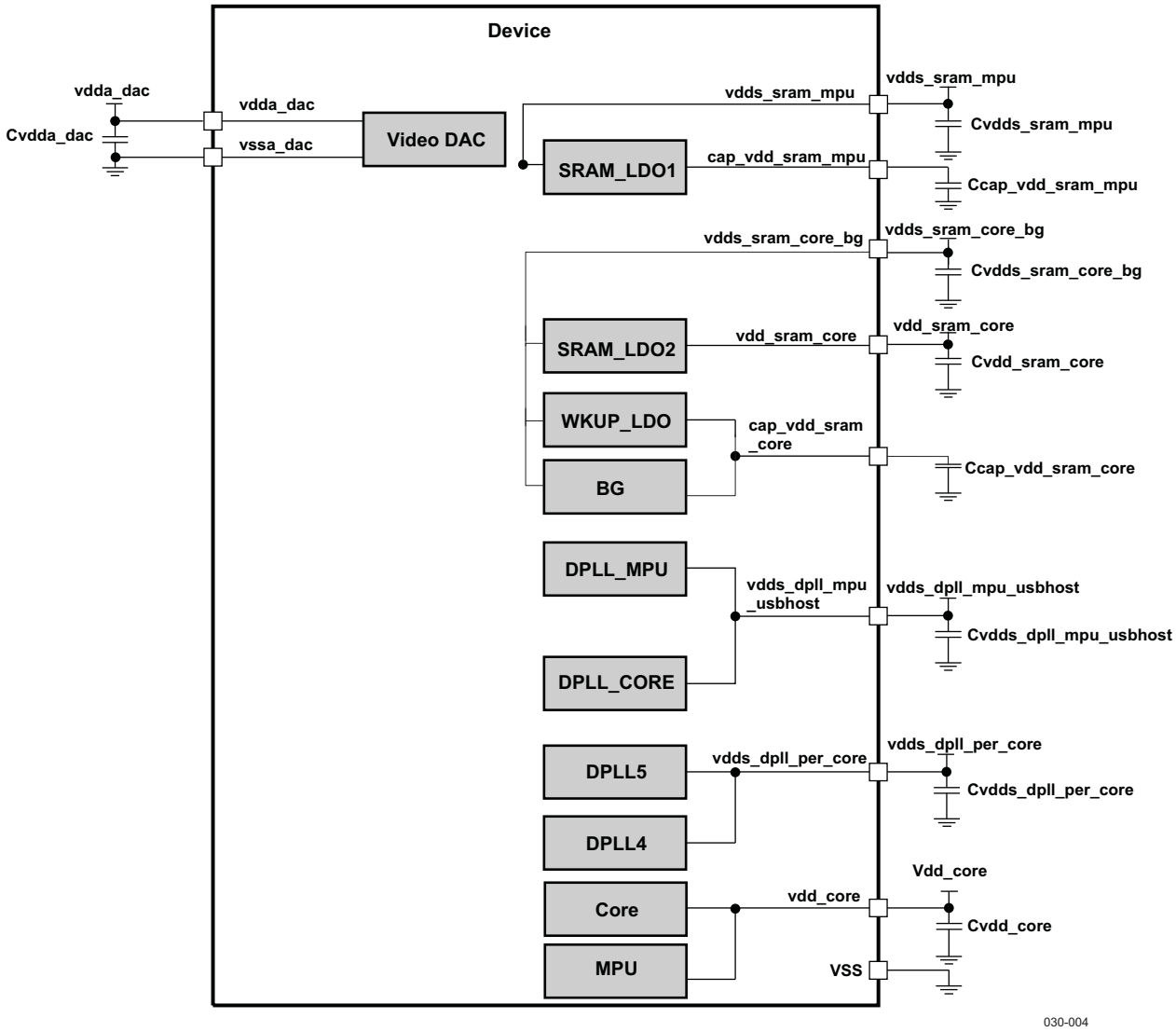
Table 3-5 summarizes the power supplies decoupling characteristics.

Table 3-5. Core Voltage Decoupling Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Cvdd_core(1)	50	100	120	nF
Ccap_vdd_sram_core		100		nF
Cvdds_dpll_mpu_usbhost		100		nF
Cvdds_dpll_per_core		100		nF
Cvdda_dac		100		nF
Cvdd_sram_core		100		nF
Cvdd_sram_core_bg		100		nF
Cvdds_mmc1		100		nF
Cvdds_sram_mpu		100		nF

(1) 1 capacitor per 2 to 4 balls

Figure 3-2 illustrates an example of power supply decoupling.



(1) Decoupling capacitors must be placed as closed as possible to the power ball. Choose the ground located closest to the power pin for each decoupling capacitor. Place the decoupling capacitor Ci in a group of 1, 2, or 3 balls; the total must be equal to the decoupling requirement. In case you interconnect powers, first insert the decoupling capacitor and then interconnect the powers.

(2) The decoupling capacitor value depends on the board characteristics.

Figure 3-2. Power Supply Decoupling

3.5 Power-up and Power-down

This section provides the timing requirements for the AM3517/05 hardware signals.

3.5.1 Power-up Sequence

The following steps give an example of power-up sequence supported by the AM3517/05.

3.3-V Operation Sequence:

1. IO 1.8V (VDDS) supply should come up first. This is required to bias the circuitry for the 3.3V IO's.
2. IO 3.3V (VDDSHV) supply should be ramped up next.
3. Band-gap, LDO supplies (VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU) should be ramped up next.
4. Core supply follows next.
5. All the PLL supplies (VDDS_DPLL_PER_CORE, VDDS_DPLL_MPU_USBHOST) should be ramped up next. Ensure PLL is powered-up in OFFMODE=1 to control any transients.
6. All the other complex IO power supplies should be ramped up next (DAC, USB).
7. sys_nrespwron must be held low at the time the power supplies are ramped up till the time the sys_32k and sys_xtalin clocks are stable.

1.8-V Operation Sequence:

1. IO 1.8V (VDDS and VDDSHV) supply should come up first. This is required to bias the circuitry for the 3.3V IO's.
2. Band-gap, LDO supplies (VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU) should be ramped up next.
3. Core supply follows next.
4. All the PLL supplies (VDDS_DPLL_PER_CORE, VDDS_DPLL_MPU_USBHOST) should be ramped up next. Ensure PLL is powered-up in OFFMODE=1 to control any transients.
5. All the other complex IO power supplies should be ramped up next (DAC, USB).
6. sys_nrespwron must be held low at the time the power supplies are ramped up till the time the sys_32k and sys_xtalin clocks are stable.
7. The other power supplies can then be turned on upon software request.

Notes: Depending on the target Power IC

- VDDS, VDDSHV (1.8-V operation only), VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU, and VDDSOSC can be grouped and powered up together.
- VDDS_DPLL_PER_CORE, VDDS_DPLL_MPU_HOST and all the other complex IO power supplies can be grouped together.

Figure 3-3 shows the power-up sequence.

Note: If an external square clock is provided, it could be started after sys_nrespwron release provided it is clean: no glitch, stable frequency, and duty cycle.

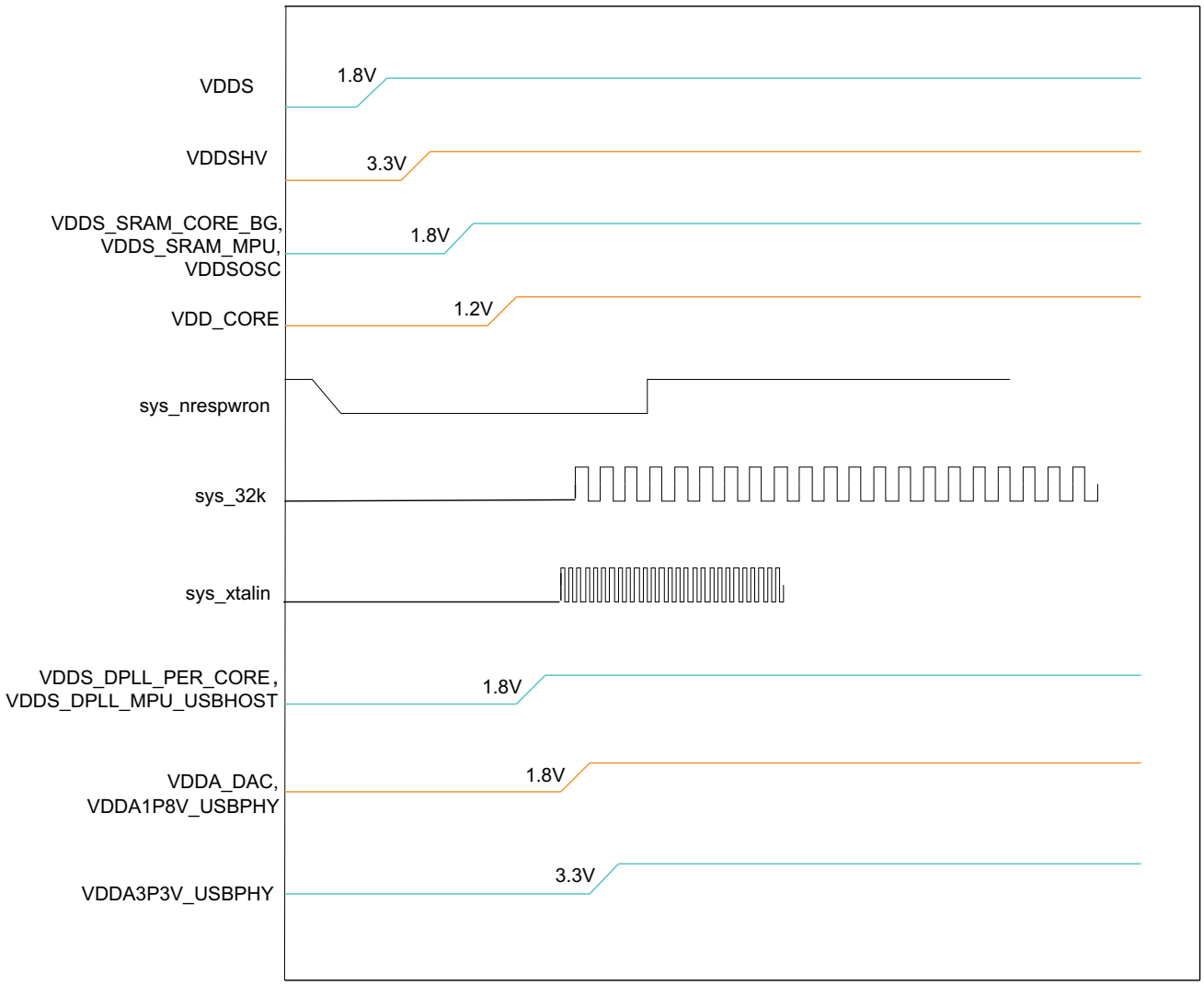


Figure 3-3. Power-up Sequence

3.5.2 Power-down Sequence

The AM3517/05 device proceeds with the power-down sequence shown below.

The following steps give an example of the power-down sequence supported by the AM3517/05 device.

1. Reset AM3517/05 device.
2. Stop all signals driven to AM3517/05.
3. Option 1: Power down all domains simutaneously.
4. Option 2: If all domains cannot be powered down simultaneously, follow the below sequence:
   a. Power off all complex I/O domains
   b. Power off core domain (VDD_CORE)
   c. Power off all PLL domains (VDDS_DPLL_MPU_USBHOST and VDDS_DPLL_PER_CORE)
   d. Power off all SRAM LDOs
   e. Power off all standard I/O domains (VDDS and VDDSHV)

4 CLOCK SPECIFICATIONS

The AM3517/05 device has three external input clocks, a low frequency (sys_32k), a high frequency (sys_xtalin), and an optional (sys_altclk). The AM3517/05 device has two configurable output clocks, sys_clkout1 and sys_clkout2.

Figure 4-1 shows the interface to the external clock sources and clock outputs.

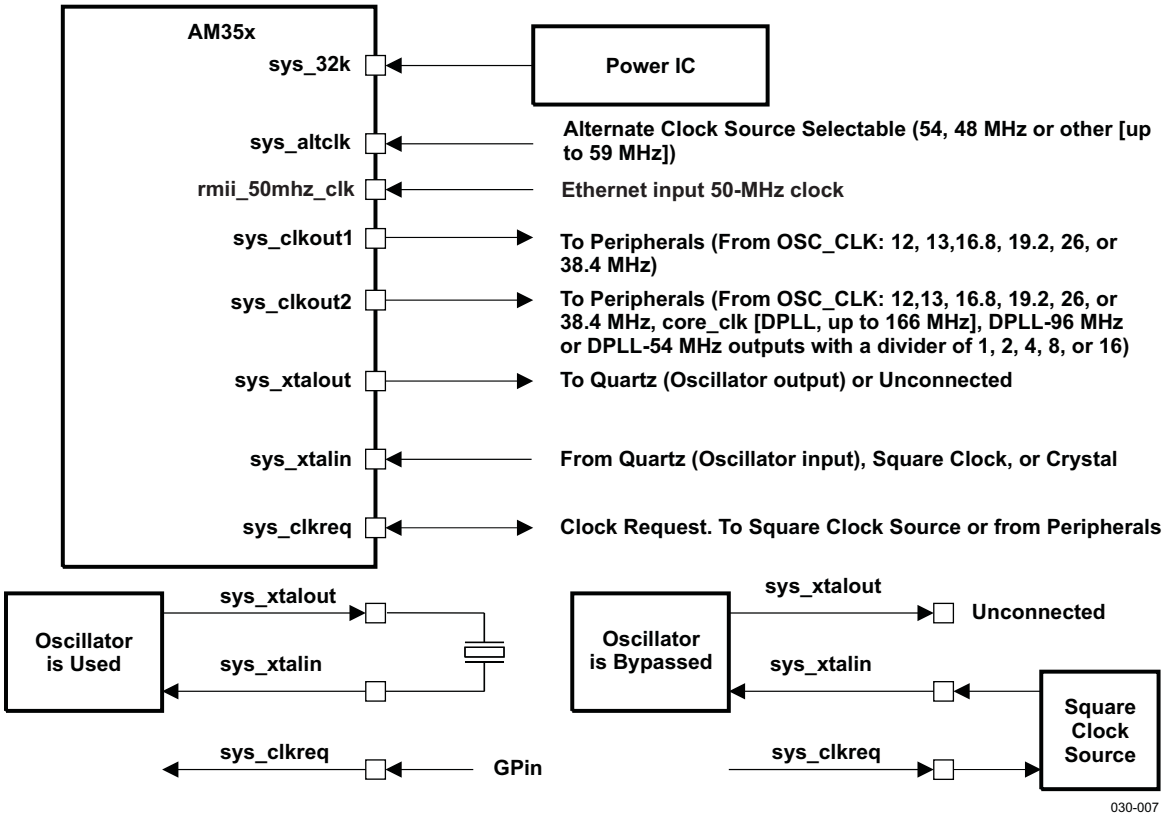


Figure 4-1. Clock Interface

The AM3517/05 device operation requires the following three input clocks:

- The 32-kHz clock can be generated using one of the following options and can be selected via the sys_boot7 pin. See Figure 4-2.
  - External: Supplied by an oscillator on the sys_32k pin.
  - Internal: 32-kHz clock generation using a fixed divider on the HS system clock (26MHz).
- The system alternative clock can be used (through the sys_altclk pin) to provide alternative 48 or 54 MHz or other clock source (up to 54 MHz).
- The system clock input (26 MHz) is used to generate the main source clock of the AM3517/05 device. It supplies the DPLLs as well as several AM3517/05 modules. The system clock input can be connected to either:
  - A crystal oscillator clock managed by sys_xtalin and sys_xtalout. In this case, the sys_clkreq is used as an input (GPIN).
  - A CMOS digital clock through the sys_xtalin pin. In this case, the sys_clkreq is used as an output to request the external system clock.

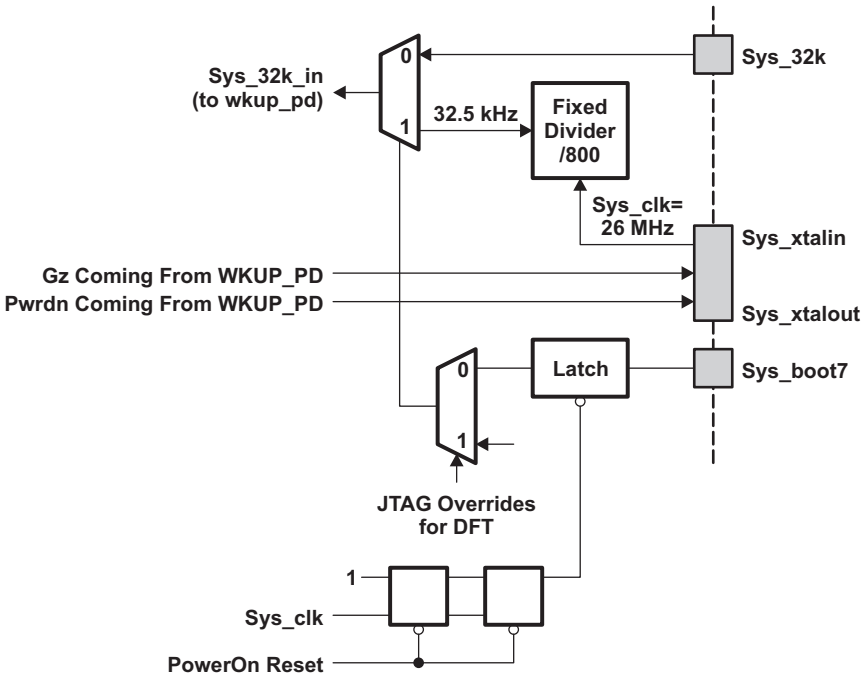


Figure 4-2. 32-kHz Clock Generation

The AM3517/05 outputs externally two clocks:

- sys_clkout1 can output the oscillator clock (26 MHz) at any time.
- sys_clkout2 can output the oscillator clock, core_clk, 96 MHz or 54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable.

4.1 Oscillator

On AM3517/05, VSSOSC has a dedicated ground (sys_xtalgnd) that is used to help reduce jitter. The load capacitors for sys_xtalin and sys_xtalout should be connected between the corresponding xtal pin to sys_xtalgnd as shown in Figure 4-3.

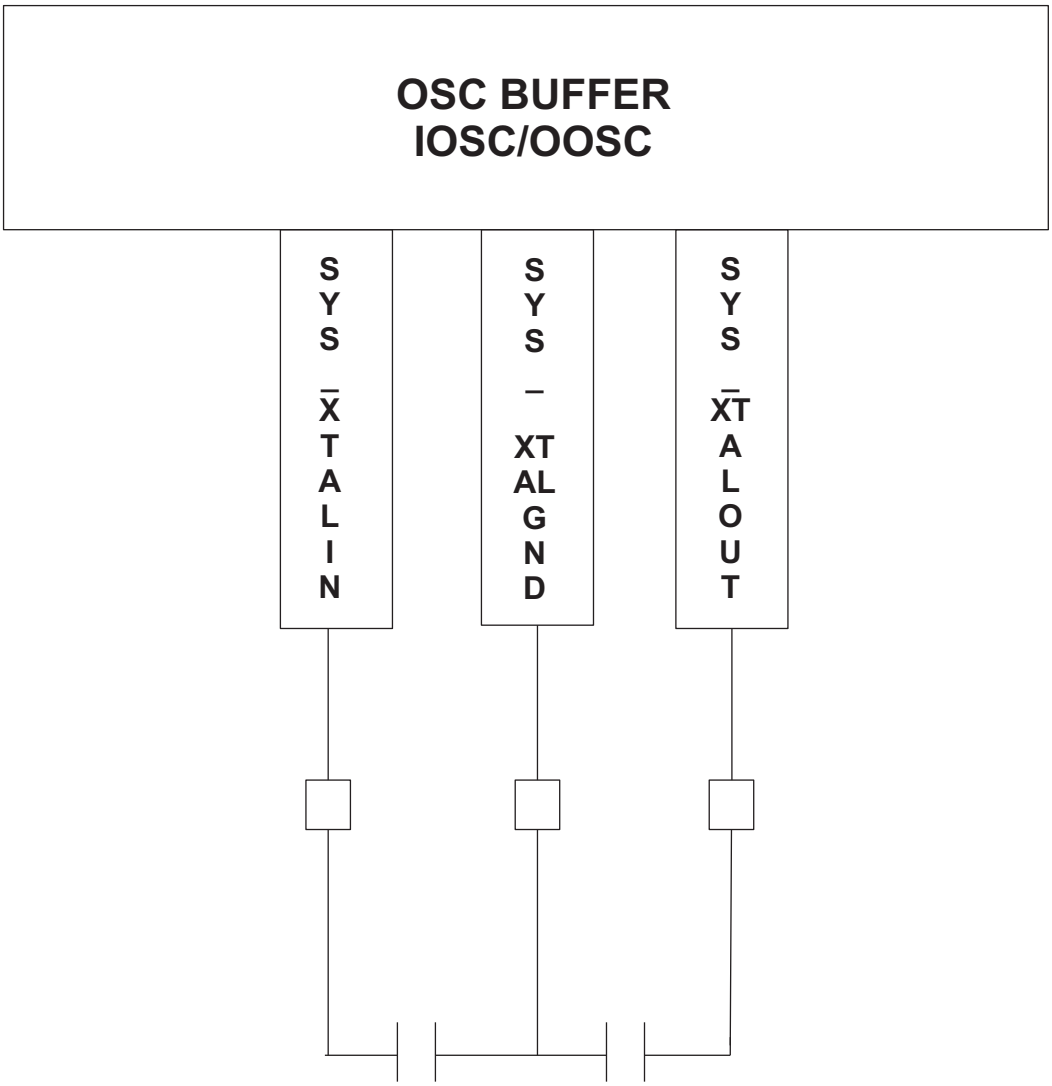


Figure 4-3. AM3517/05 Oscillator Connections

4.2 Input Clock Specifications

The clock system accepts three input clock sources:

- 32-kHz digital CMOS clock
- Crystal oscillator clock or CMOS digital clock (26 MHz)
- Alternate clock (48 or 54 MHz, or other up to 54 MHz)

4.3 Output Clock Specifications

Two output clocks (pin sys_clkout1 and pin sys_clkout2) are available:

- sys_clkout1 can output the oscillator clock (26 MHz) at any time. It can be controlled by software or externally using sys_clkreq control. When the device is in the off state, the sys_clkreq can be asserted to enable the oscillator and activate the sys_clkout1 without waking up the device. The off state polarity of sys_clkout1 is programmable.
- sys_clkout2 can output sys_clk (26 MHz), core_clk (core DPLL output), APLL-96 MHz, or APLL-54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable. This output is active only when the core domain is active.

Table 4-1 summarizes the sys_clkout1 output clock electrical characteristics.

Table 4-1. sys_clkout1 Output Clock Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	Frequency			26		MHz
C_I	Load capacitance(1)	f(max) = 38.4 MHz		70		pF
		f(max) = 26 MHz		125		

(1) The load capacitance is adapted to a frequency.

Table 4-2 details the sys_clkout1 output clock timing characteristics.

Table 4-2. sys_clkout1 Output Clock Switching Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	1 / CO0	Frequency		26		MHz
CO1	$t_{w(CLKOUT1)}$	Pulse duration, sys_clkout1 low or high	0.40 * $t_{c(CLKOUT1)}$		0.60 * $t_{c(CLKOUT1)}$	ns
CO2	$t_{R(CLKOUT1)}$	Rise time, sys_clkout1(1)			3.31	ns
CO3	$t_{F(CLKOUT1)}$	Fall time, sys_clkout1(1)			3.31	ns

(1) With a load capacitance of 25 pF.

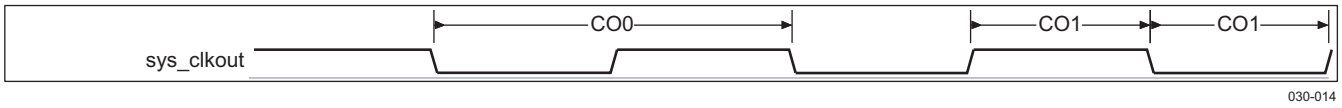


Figure 4-4. sys_clkout1 System Output Clock

Table 4-3 summarizes the sys_clkout2 output clock electrical characteristics.

Table 4-3. sys_clkout2 Output Clock Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	Frequency, sys_clkout2(1)				166	MHz
C_L	Load capacitance(2)	f(max) = 166 MHz	2	8	12	pF

(1) The maximum frequency supported is core_clk/2 MHz.
(2) The load capacitance is adapted to a frequency.

Table 4-4 details the sys_clkout2 output clock timing characteristics.

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Table 4-4. sys_clkout2 Output Clock Switching Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	1 / CO0	Frequency			322	MHz
CO1	$t_{w(CLKOUT2)}$	Pulse duration, sys_clkout2 low or high	0.40 * tc(CLKOUT2)		0.60 * tc(CLKOUT2)	ns
CO2	$t_{R(CLKOUT2)}$	Rise time, sys_clkout2 (1)			3.7	ns
CO3	$t_{F(CLKOUT2)}$	Fall time, sys_clkout2 (1)			4.3	ns

(1) With a load capacitance of 25 pF.

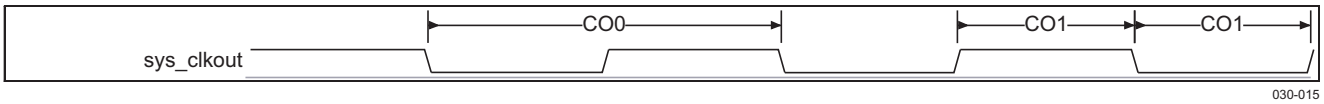

Figure 4-5. sys_clkout2 System Output Clock

PRODUCT PREVIEW

4.4 DPLL Specifications

The AM3517/05 integrates four DPLLs. The PRM and CM drive them.

The four main DPLLs are:

- DPLL1 (MPU)
- DPLL3 (Core)
- DPLL4 (Peripherals)
- DPLL5 (Second Peripherals DPLL)

Figure 4-6 illustrates the DPLL implementation.

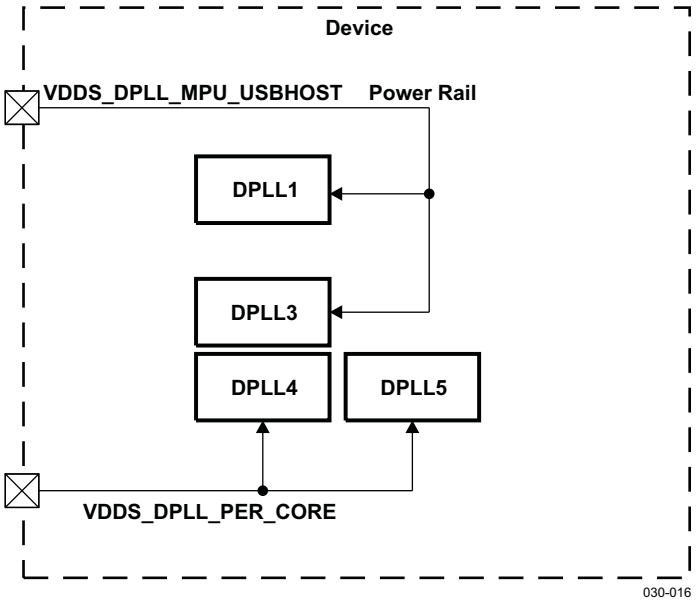

Figure 4-6. DPLL Implementation

4.4.1 Digital Phase-Locked Loop (DPLL)

The DPLL provides all interface clocks and some functional clocks (such as the processor clocks) of the AM3517/05 device.

DPLL1 gets an always-on clock used to produce the synthesized clock. They get a high-speed bypass clock used to switch the DPLL output clock on this high-speed clock during bypass mode.

The high-speed bypass clock is an L3 divided clock (programmable by 1 or 2) that saves DPLL processor power consumption when the processor does not need to run faster than the L3 clock speed, or optimizes performance during frequency scaling.

Each DPLL synthesized frequency is set by programming M (multiplier) and N (divider) factors. In addition, all DPLL outputs can be controlled by an independent divider (M2 to M6).

The clock generating DPLLs of the AM3517/05 device have following features:

- Independent power domain per DPLL
- Controlled by clock-manager (CM)
- Fed with always-on system clock with independent gating control per DPLL
- Analog part supplied through dedicated power supply (1.8 V) and an embedded LDO to get rid of 1-MHz noise
- Up to four independent output dividers for simultaneous generation of multiple clock frequencies

4.4.1.1 DPLL1 (MPU)

DPLL1 is located in the MPU subsystem and supplies all clocks of the subsystem. All MPU subsystem clocks are internally generated in the subsystem. When the core domain is on, it can use the DPLL3 (CORE DPLL) output as a high-frequency bypass input clock.

4.4.1.2 DPLL3 (CORE)

DPLL3 supplies all interface clocks and also a few module functional clocks. It can be also source of the emulation trace clock. It is located in the core domain area. All interface clocks and a few module functional clocks are generated in the CM. When the core domain is on, it can be used as a bypass input to DPLL1.

4.4.1.3 DPLL4 (Peripherals)

DPLL4 generates clocks for the peripherals. It supplies five clock sources: 96-MHz functional clocks to subsystems and peripherals, 54 MHz to TV DAC, display functional clock, camera sensor clock, and emulation trace clock. It is located in the core domain area. All interface clocks and few module functional clocks are generated in the CM. Its outputs to the DSS, PER, and EMU domains are propagated with always-on clock trees.

4.4.1.4 DPLL5 (Second peripherals DPLL)

DPLL5 supplies the 120-MHz functional clock to the CM.

4.4.2 DPLL Noise Isolation

The DPLL requires dedicated power supply pins to isolate the core analog circuit from the switching noise generated by the core logic that can cause jitter on the clock output signal. Guard rings are added to the cell to isolate it from substrate noise injection.

The vdd supplies are the most sensitive to noise; decoupling capacitance is recommended below the supply rails. The maximum input noise level allowed is 30 mV_{PP} for frequencies below 1 MHz.

illustrates an example of a noise filter.

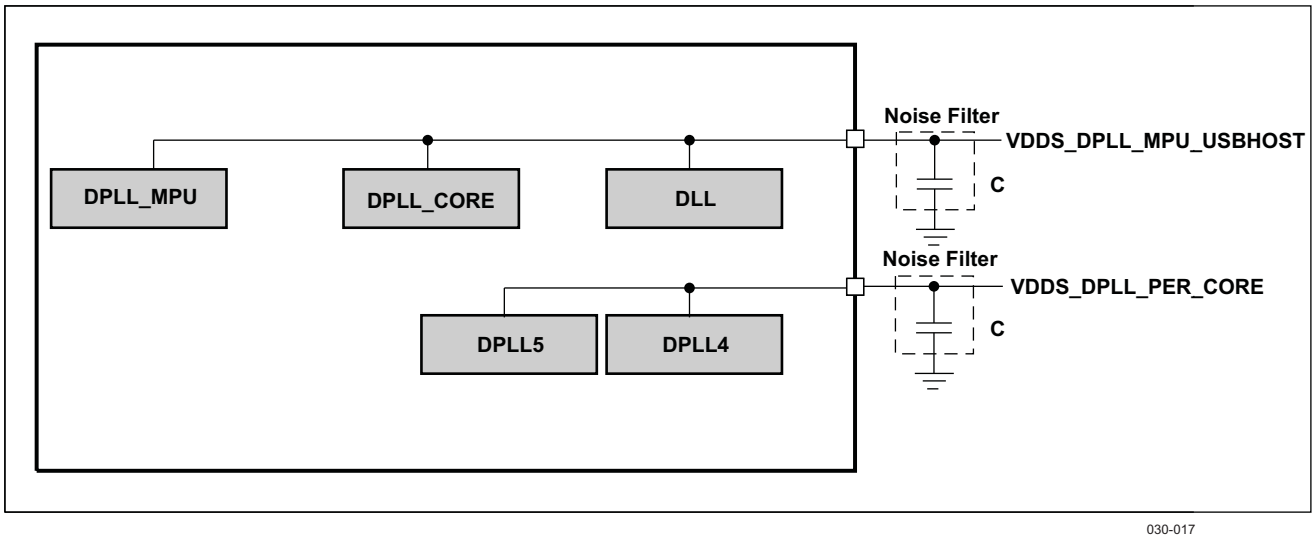

Figure 4-7. DPLL Noise Filter

Table 4-5 specifies the noise filter requirements.

Table 4-5. DPLL Noise Filter Requirements

NAME	MIN	TYP	MAX	UNIT
Filtering capacitor		100		nF

(1) The capacitors must be inserted between power and ground as close as possible.
(2) This circuit is provided only as an example.
(3) The filter must be located as close as possible to the device.
(4) No filtering required if noise is below 10 mV_{PP}.

5 VIDEO DAC SPECIFICATIONS

A dual-display interface equips the AM3517/05 processor. This display subsystem provides the necessary control signals to interface the memory frame buffer directly to the external displays (TV-set). Two (one per channel) 10-bit current steering DACs are inserted between the DSS and the TV set to generate the video analog signal. One of the video DACs also includes TV detection and power-down mode. Figure 5-1 illustrates the AM3517/05 DAC architecture.

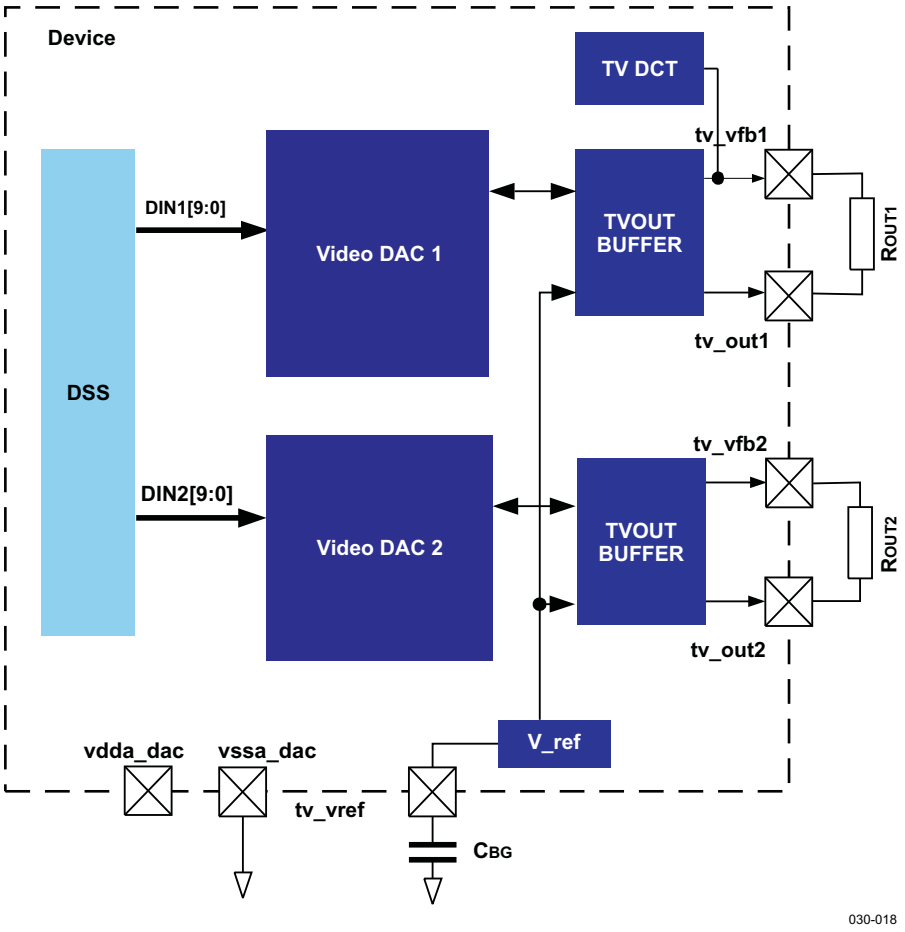

Figure 5-1. Video DAC Architecture

The following paragraphs detail the 10-bit DAC interface pinout, static and dynamic specifications, and noise requirements. The operating conditions and absolute maximum ratings are detailed in Table 5-2 and Table 5-4.

5.1 Interface Description

Table 5-1 summarizes the external pins of the video DAC.

Table 5-1. External Pins of 10-bit Video DAC

PIN NAME	I/O	DESCRIPTION	
tv_out1	O	TV analog output composite	DAC1 video output. An external resistor is connected between this node and tv_vfb1. The nominal value of ROUT1 is 1650 . Finally, note that this is the output node that drives the load (75).
tv_out2	O	TV analog output S-VIDEO	DAC2 video output. An external resistor is connected between this node and tv_vfb2. The nominal value of ROUT2 is 1650 . Finally, note that this is the output node that drives the load (75).
tv_vref	I	Reference output voltage from internal bandgap	A decoupling capacitor (CBG) needs to be connected for optimum performance.
tv_vfb1	O	Amplifier feedback node	Amplifier feedback node. An external resistor is connected between this node and tv_out1. The nominal value of ROUT1 is 1650 (1%).
tv_vfb2	O	Amplifier feedback node	Amplifier feedback node. An external resistor is connected between this node and tv_out2. The nominal value of ROUT2 is 1650 (1%).

5.2 Electrical Specifications Over Recommended Operating Conditions

(T_{MIN} to T_{MAX}, vdda_dac = 1.8 V, $R_{OUT1/2}$ = 1650 , R_{LOAD} = 75 , unless otherwise noted)

Table 5-2. DAC Static Electrical Specification

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
R	Resolution			10		Bits
DC ACCURACY						
INL(1)	Integral nonlinearity		1		1	LSB
DNL(2)	Differential nonlinearity		1		1	LSB
ANALOG OUTPUT						
-	Full-scale output voltage	R_{LOAD} = 75	0,7	0.88	1	V
-	Output offset voltage			50		mV
-	Output offset voltage drift			20		mV/C
-	Gain error		17		19	% FS
R_{VOUT}	Output impedance		67.5	75	82.5	
REFERENCE						
V_{REF}	Reference voltage range		0.525	0.55	0.575	V
-	Reference noise density	100-kHz reference noise bandwidth		129		
R_{SET}	Full-scale current adjust resistor		3700	4000	4200	
P_{SRR}	Reference PSRR(3) (Up to 6 MHz)			40		dB
POWER CONSUMPTION						
$I_{vdda-up}$	Analog Supply Current(4)	2 channels, no load		8		mA
-	Analog supply driving a 75- load (RMS)	2 channels		50		mA
$I_{vdda-up}$ (peak)	Peak analog supply current:	Lasts less than 1 ns		60		mA
I_{vdd-up}	Digital supply current(5)	Measured at f_{CLK} = 54 MHz, f_{OUT} = 2 MHz sine wave, vdd = 1.3 V		2		mA
$I_{vdd-up\ (peak)}$	Peak digital supply current(6)	Lasts less than 1 ns		2.5		mA
$I_{vdda-down}$	Analog power at power-down	T = 30C, vdda = 1.8 V		1.5		mA
$I_{vdd-down}$	Digital power at power-down	T = 30C, vdd = 1.3 V		1		mA

(1) The INL is measured at the output of the DAC (accessible at an external pin during bypass mode).
(2) The DNL is measured at the output of the DAC (accessible at an external pin during bypass mode).
(3) Assuming a capacitor of 0.1 F at the tv_ref node.
(4) The analog supply current I_{vdda} is directly proportional to the full-scale output current IFS and is insensitive to f_{CLK}
(5) The digital supply current I_{VDD} is dependent on the digital input waveform, the DAC update rate f_{CLK}, and the digital supply VDD.
(6) The peak digital supply current occurs at full-scale transition for duration less than 1 ns.

(T_{MIN} to T_{MAX}, vdda_dac = 1.8 V, $R_{OUT1/2}$ = 1650 , R_{LOAD} = 75 , unless otherwise noted)

Table 5-3. Video DAC Dynamic Electrical Specification

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
f_{CLK} (1)	Output update rate	Equal to input clock frequency		54		MHz
	Clock jitter	rms clock jitter required in order to assure 10-bit accuracy			40	ps
	Attenuation at 5.1 MHz	Corner frequency for signal	0.1	0.5	1.5	dB
	Attenuation at 54 MHz (1)	Image frequency	25	30	33	dB
t_{ST}	Output settling time	Time from the start of the output transition to output within 1 LSB of final value.		85		ns
t_{Rout}	Output rise time	Measured from 10% to 90% of full-scale transition		25		ns
t_{Fout}	Output fall time	Measured from 10% to 90% of full-scale transition		25		ns
BW	Signal bandwidth			6		MHz
	Differential gain (2)			1.5%		
	Differential phase (2)			1		deg.
SFDR	Within bandwidth	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz		45		dB
SNR	Signal-to-noise ratio 1 kHz to 6 MHz bandwidth	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz		55 (3)		dB
PSRR	Power supply rejection ratio	Up to 6 MHz		20 (4)		dB
Crosstalk	Between the two video channels			50	40	dB

(1) For internal input clock information, For more information, see the *Device Display Interface Subsystem Reference Guide* [literature number SPRUFV2].
(2) The differential gain and phase value is for dc coupling. Note that there is degradation for the ac coupling.
(3) The SNR value is for dc coupling. Note that there is a 6-dB degradation for ac coupling.
(4) The PSSR value is for dc coupling. Note that there is a 10-dB degradation for ac coupling.

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5.3 Analog Supply (vdda_dac) Noise Requirements

In order to assure 10-bit accuracy of the DAC analog output, the analog supply vdda_dac has to meet the noise requirements stated in this section.

The DAC Power Supply Rejection Ratio is defined as the relative variation of the full-scale output current divided by the supply variation. Thus, it is expressed in percentage of Full-Scale Range (FSR) per volt of supply variation as shown in the following equation:

$$PSRR_{DAC} = \frac{100 \cdot \frac{\Delta I_{OUT}}{I_{OUTFS}}}{V_{AC}} \qquad \left[\% \ FSR/V\right]$$

Depending on frequency, the PSRR is defined in Table 5-4.

Table 5-4. Video DAC Power Supply Rejection Ratio

Supply Noise Frequency	PSRR % FSR/V
0 to 100 kHz	1
> 100 kHz	The rejection decreases 20 dB/dec. Example: at 1 MHz the PSRR is 10% of FSR/V

A graphic representation is shown in Figure 5-2.

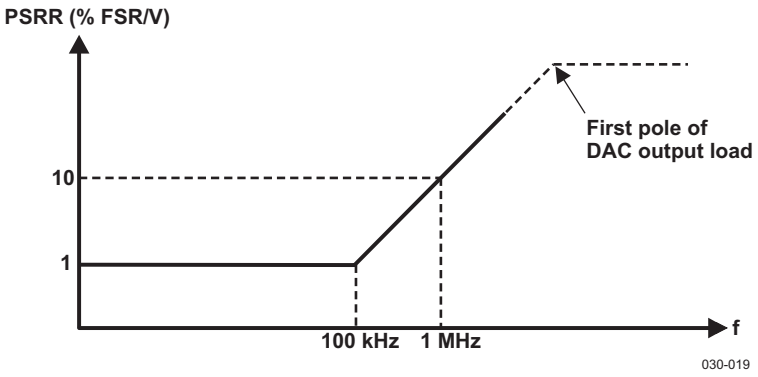

Figure 5-2. Video DAC Power Supply Rejection Ratio

To ensure that the DAC SFDR specification is met, the PSRR values and the clock jitter requirements translate to the following limits on vdda_dac (for the Video DAC).

The maximum peak-to-peak noise on vdda (ripple) is defined in Table 5-5:

Table 5-5. Video DAC Maximum Peak-to-Peak Noise on vdda_dac

Tone Frequency	Maximum Peak-to-Peak Noise on vdda_dac
0 to 100 kHz	< 30 mVpp
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum is 3 mVpp

The maximum noise spectral density (white noise) is defined in Table 5-6:

Table 5-6. Video DAC Maximum Noise Spectral Density

Supply Noise Bandwidth	Maximum Supply Noise Density
0 to 100 kHz	< 20 V / $\overline{\text{Hz}}$
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum noise density is 2 / $\overline{\text{Hz}}$

Because the DAC PSRR deteriorates at a rate of 20 dB/dec after 100 kHz, it is highly recommended to have vdda_dac low pass filtered (proper decoupling) (see the illustrated application: Section 5.4, *External Component Value Choice*).

5.4 External Component Value Choice

The full-scale output voltage V_{OUTMAX} is regulated by the reference amplifier, and is set by an internal resistor R_{SET}. I_{OUTMAX} can be expressed as:

$$I_{OUTMAX} = I_{REF} /8 * (63 + 15/16)$$

Where:

$$V_{REF} = 0.5V$$

$$I_{REF} = V_{REF}/R_{SET}$$

The output current I_{OUT} appearing at DAC output is a function of both the input code and I_{OUTMAX} and can be expressed as:

$$I_{OUT} = (DAC\_CODE/1023) * I_{OUTMAX}$$

Where:

DAC_CODE = 0 to 1023 is the DAC input code in decimal.

The output voltage is:

$$V_{OUT} = I_{OUT} *N* R_{CABLE}$$

Where:

(N = amplifier gain = 21)

R_{CABLE} = 75 (cable typical impedance)

The TV-out buffer requires a per channel external resistors: $R_{OUT1/2}$. The equation below can be used to select different resistor values (if necessary):

$$R_{OUT} = (N+1) R_{CABLE} = 1650$$

Recommended parameter values are:

Table 5-7. Video DAC Recommended External Components Values

	Recommended Value	UNIT
C_{BG}	100	nF
$R_{OUT1/2}$	1650	

In order to limit the reference noise bandwidth and to suppress transients on V_{REF}, it is necessary to connect a large decoupling capacitor $_{BG}$) between the tv_vref and vssa_dac pins.

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6 TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

Note: The timing data shown is ***preliminary*** data and is subject to change in future revisions.

6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions of Table 3-3, unless otherwise specified.

6.2 Interface Clock Specifications

6.2.1 Interface Clock Terminology

The Interface clock is used at the system level to sequence the data and/or control transfers accordingly with the interface protocol.

6.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the AM3517/05 IC and doesn't take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and AM3517/05 IC timings characteristics as well, to define properly the maximum operating frequency, which corresponds to the maximum frequency supported to transfer the data on this interface.

6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology identifies this type of jitter.

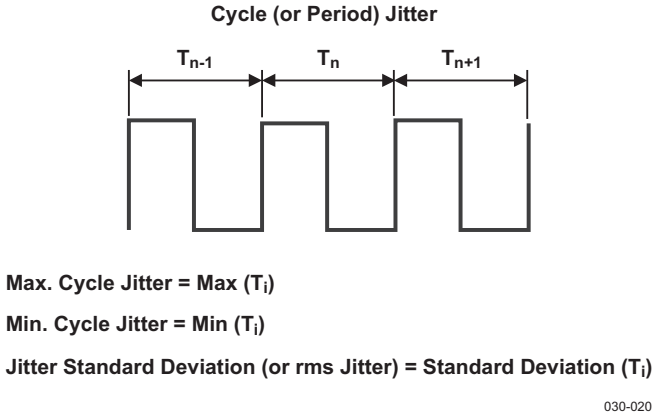


Figure 6-1. Cycle (or Period) Jitter

6.2.4 Clock Duty Cycle Error

The duty cycle error is the ratio between either the high-level pulse duration or the low-level pulse duration and the cycle time of a clock signal.

6.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as follows:

Table 6-1. Timing Parameters

LOWERCASE SUBSCRIPTS	
Symbols	**Parameter**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or dont care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.4 External Memory Interfaces

The AM3517/05 processor includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- SDRAM controller (SDRC)

6.4.1 General-Purpose Memory Controller (GPMC)

The GPMC is the AM3517/05 unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

6.4.1.1 GPMC/NOR Flash Interface Synchronous Timing

Table 6-3 and Table 6-4 assume testing over the recommended operating conditions (see Figure 6-2 through Figure 6-5) and electrical characteristic conditions.

Table 6-2. GPMC/NOR Flash Synchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance		TBD	pF

Table 6-3. GPMC/NOR Flash Interface Timing Requirements Synchronous Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
F12	$t_{su(DV-CLKH)}$	Setup time, read gpmc_d[15:0] valid before gpmc_clk high	TBD		ns
F13	$t_{h(CLKH-DV)}$	Hold time, gpmc_d[15:0] valid after gpmc_clk high	TBD		ns
F21	$t_{su(WAITV-CLKH)}$	Setup time, gpmc_waitx(1) valid before gpmc_clk high	TBD		ns
F22	$t_{h(CLKH-WAITV)}$	Hold Time, gpmc_waitx(1) valid after gpmc_clk high	TBD		ns

(1) Wait monitoring support is limited to a WaitMonitoringTime value > 0.

Table 6-4. GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode

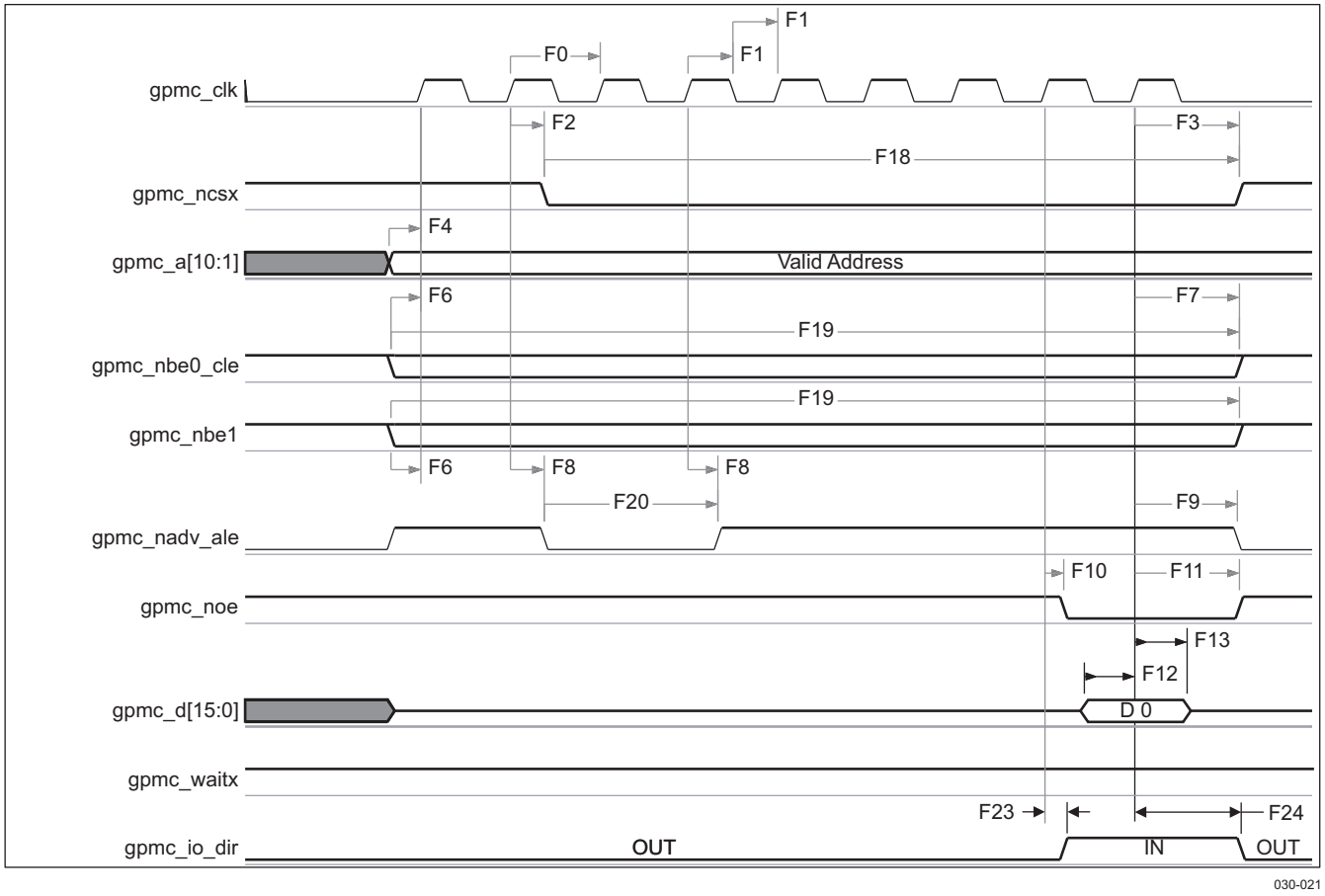
NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
F0	$t_{c(CLK)}$	Cycle time(1), output clock gpmc_clk period	TBD		ns
F1	$t_{w(CLKH)}$	Typical pulse duration, output clock gpmc_clk high	TBD	TBD	ns
F1	$t_{w(CLKL)}$	Typical pulse duration, output clock gpmc_clk low	TBD	TBD	ns
	$t_{dc(CLK)}$	Duty cycle error, output clk gpmc_clk	TBD	TBD	ps
	$t_{j(CLK)}$	Jitter standard deviation(2), output clock gpmc_clk		TBD	ps

(1) Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.
(2) The jitter probability density can be approximated by a Gaussian function.

Table 6-4. GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode (continued)

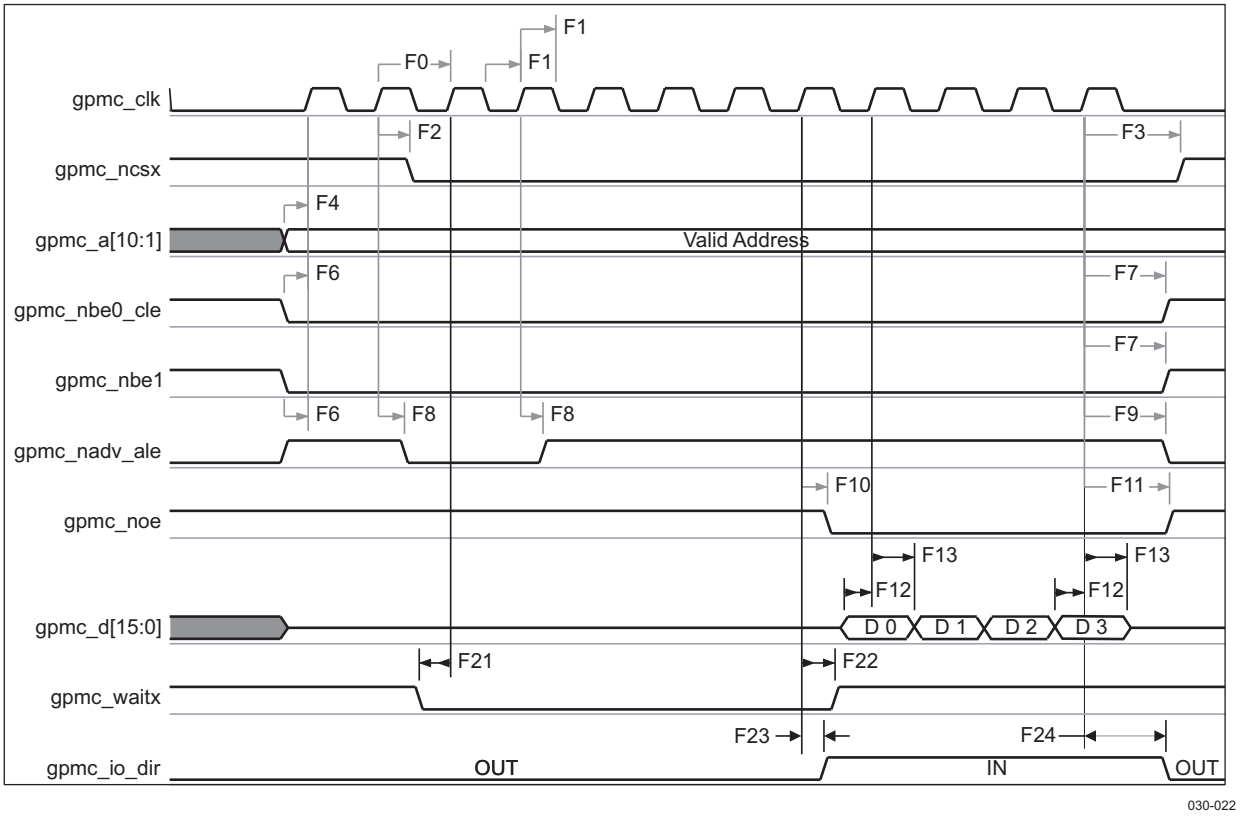
NO.	PARAMETER			1.8V, 3.3V		UNIT
				MIN	MAX	
	$t_{R(CLK)}$	Rise time, output clock gpmc_clk			TBD	ns
	$t_{F(CLK)}$	Fall time, output clock gpmc_clk			TBD	ns
	$t_{R(DO)}$	Rise time, output data			TBD	ns
	$t_{F(DO)}$	Fall time, output data			TBD	ns
F2	$t_{d(CLKH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(3) transition		TBD	TBD	ns
F3	$t_{d(CLKH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(3) invalid		TBD	TBD	ns
F4	$t_{d(ADDV-CLK)}$	Delay time, address bus valid to gpmc_clk first edge		TBD	TBD	ns
F5	$t_{d(CLKH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[16:1] invalid		TBD		ns
F6	$t_{d(nBEV-CLK)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge		TBD	TBD	ns
F7	$t_{d(CLKH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid		TBD	TBD	ns
F8	$t_{d(CLKH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale transition		TBD	TBD	ns
F9	$t_{d(CLKH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		TBD	TBD	ns
F10	$t_{d(CLKH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe transition		TBD	TBD	ns
F11	$t_{d(CLKH-nOEIV)}$	Delay time, gpcm rising edge to gpmc_noe invalid		TBD	TBD	ns
F14	$t_{d(CLKH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_nwe transition		TBD	TBD	ns
F15	$t_{d(CLKH-Data)}$	Delay time, gpmc_clk rising edge to data bus transition		TBD	TBD	ns
F17	$t_{d(CLKH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_nbex_cle transition		TBD	TBD	ns
F18	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(3) low	Read	TBD		ns
			Write	TBD		ns
F19	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	TBD		ns
			Write	TBD		ns
F20	$t_{W(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	TBD		ns
			Write	TBD		ns
F23	$t_{d(CLKH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)		TBD	TBD	ns
F24	$t_{d(CLKH-IODIRIV)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir low (OUT direction)		TBD		ns

(3) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-2. GPMC/NOR Flash Synchronous Single Read (GpmcFCLKDivider = 0)



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-3. GPMC/NOR Flash Synchronous Burst Read 4x16-bit (GpmcFCLKDivider = 0)

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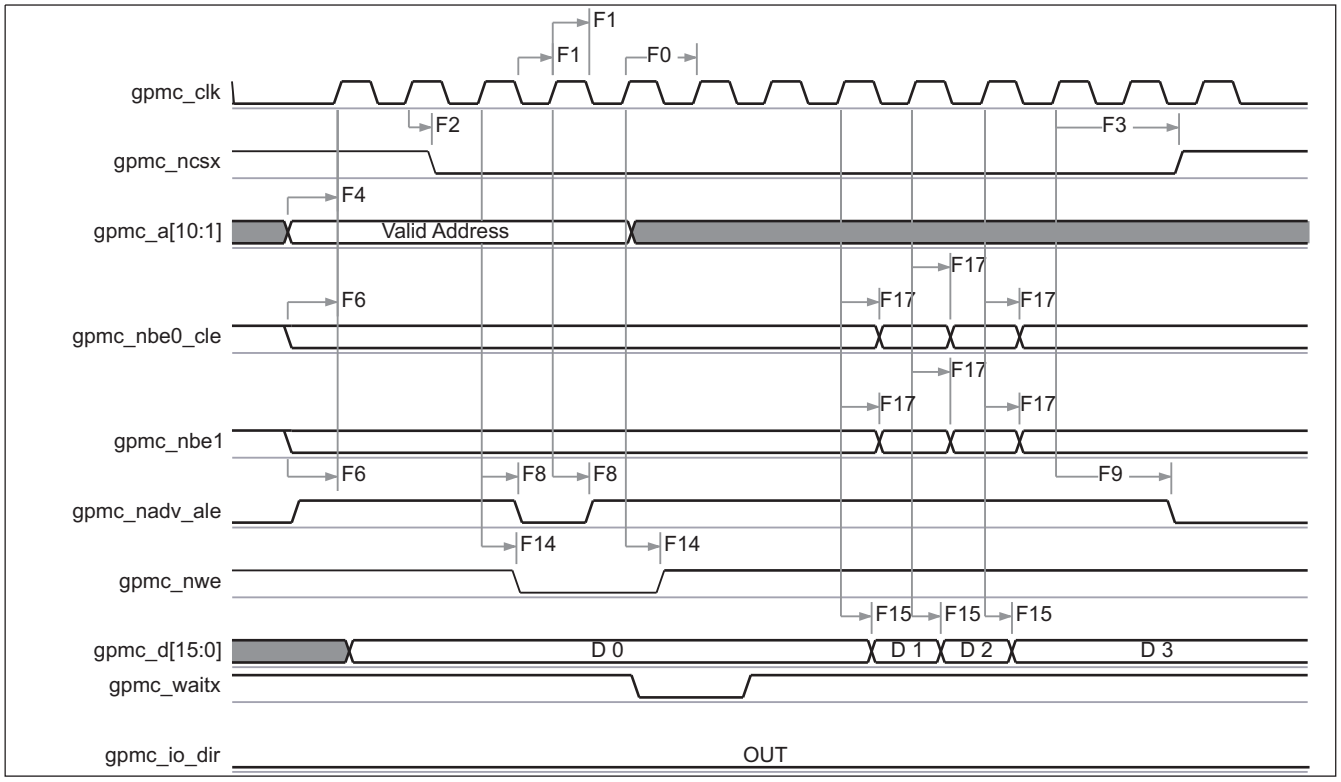
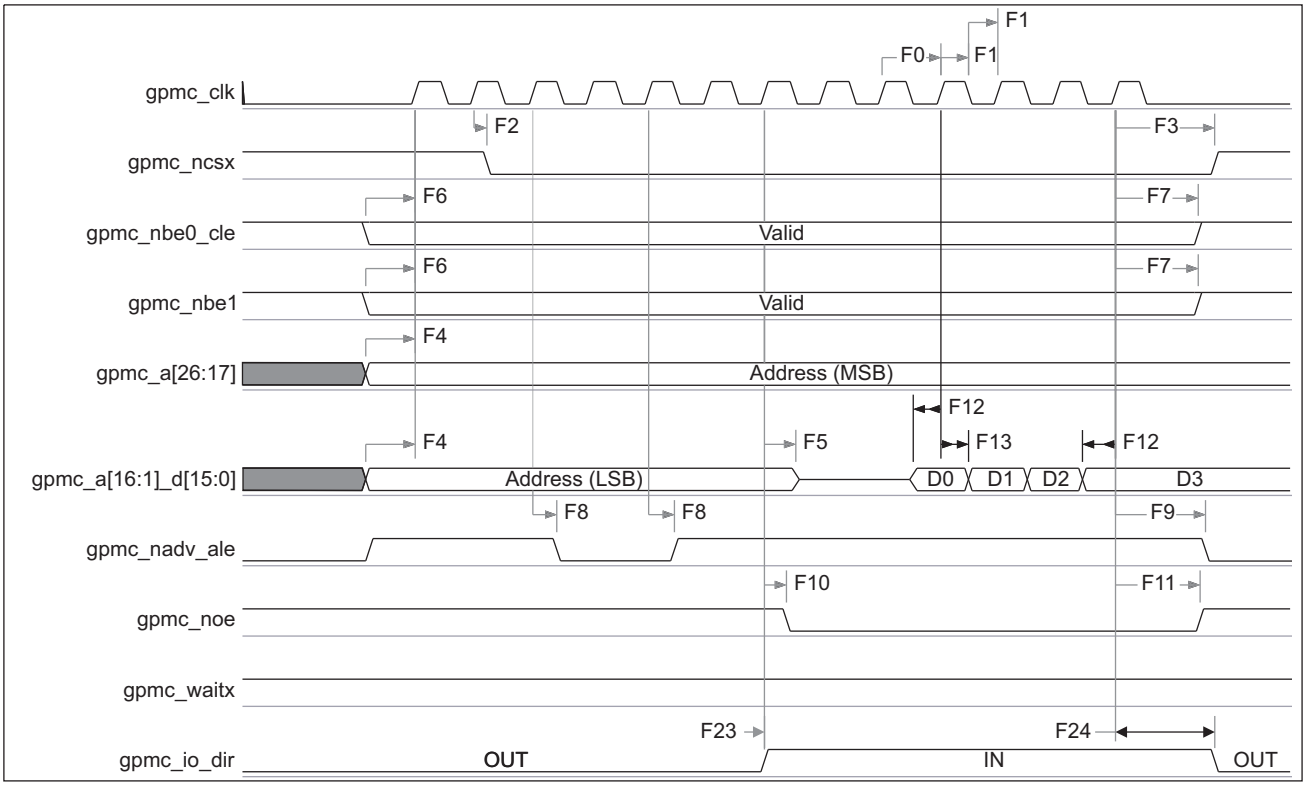


In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-4. GPMC/NOR Flash Synchronous Burst Write (GpmcFCLKDivider = 0)



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-5. GPMC/Multiplexed NOR Flash Synchronous Burst Read

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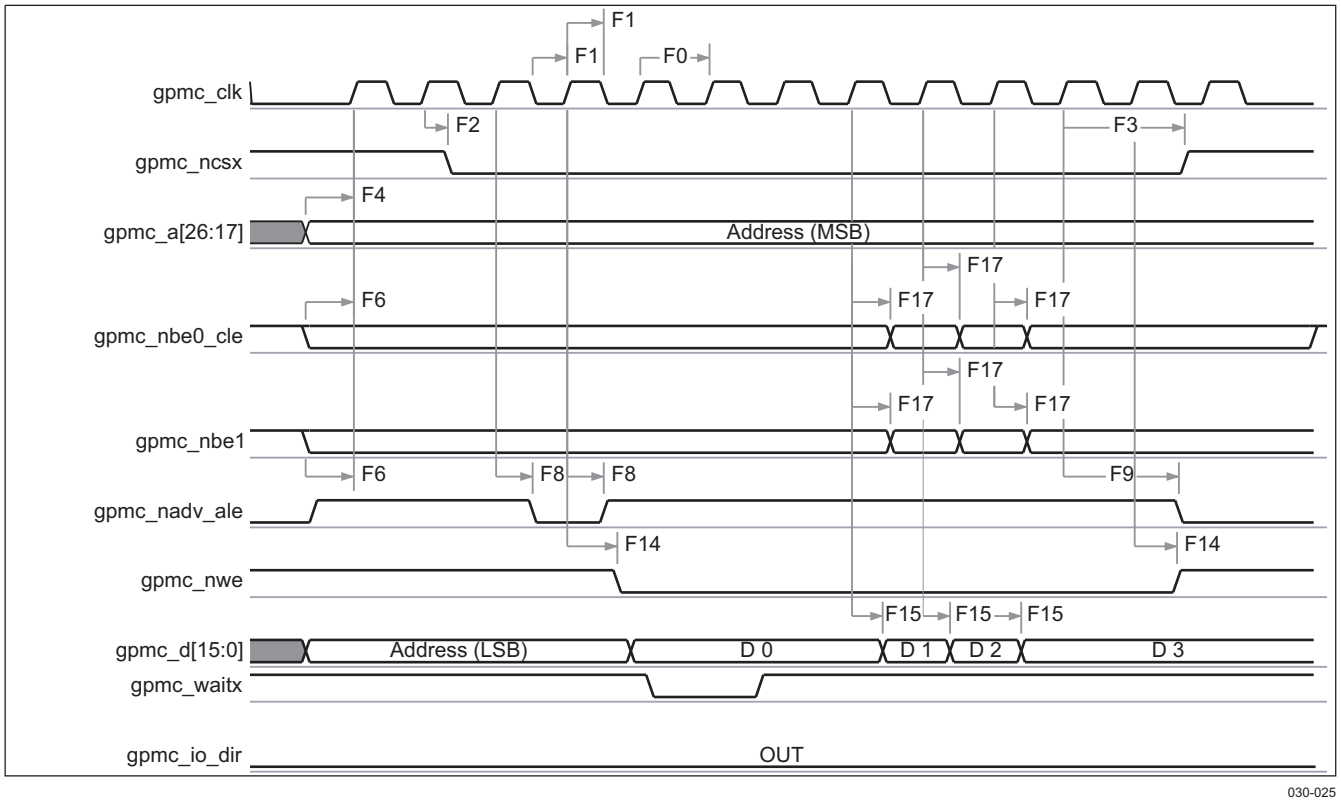

In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-6. GPMC/Multiplexed NOR Flash Synchronous Burst Write

6.4.1.2 GPMC/NOR Flash Interface Asynchronous Timing

Table 6-7 and Table 6-8 assume testing over the recommended operating conditions (see Figure 6-7 through Figure 6-12) and electrical characteristic conditions.

Table 6-5. GPMC/NOR Flash Asynchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	1.8	ns
t_F	Input signal fall time	1.8	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.94	pF

Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters(1)(2)

NO.	PARAMETER	1.8V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
FI1	Maximum output data generation delay from internal functional clock		6.5		9.1		13.7	ns
FI2	Maximum input data capture delay by internal functional clock		4		5.6		8.1	ns
FI3	Maximum device select generation delay from internal functional clock		6.5		9.1		13.7	ns

(1) The internal parameters table must be used to calculate Data Access Time stored in the corresponding CS register bit field.
(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters (continued)

NO.	PARAMETER	1.8V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
FI4	Maximum address generation delay from internal functional clock		6.5		9.1		13.7	ns
FI5	Maximum address valid generation delay from internal functional clock		6.5		9.1		13.7	ns
FI6	Maximum byte enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI7	Maximum output enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI8	Maximum write enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI9	Maximum functional clock skew		100		170		200	ps

Table 6-7. GPMC/NOR Flash Interface Timing Requirements – Asynchronous Mode

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
FA5(1)	$t_{acc(DAT)}$	Data maximum access time		H(2)		H(2)		H(2)	GPMC_FCLK cycles
FA20(3)	$t_{acc1-pgmode(DAT)}$	Page mode successive data maximum access time		P(4)		P(4)		P(4)	GPMC_FCLK cycles
FA21(5)	$t_{acc2-pgmode(DAT)}$	Page mode first data maximum access time		H(2)		H(2)		H(2)	GPMC_FCLK cycles

(1) The FA5 parameter illustrates the amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) H = AccessTime * (TimeParaGranularity + 1)
(3) The FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(4) P = PageBurstAccessTime * (TimeParaGranularity + 1)
(5) The FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode

NO.	PARAMETER			1.15 V		1.0 V		0.9 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{R(DO)}$	Rise time, output data			2.0		2.0		2.0	ns
	$t_{F(DO)}$	Fall time, output data			2.0		2.0		2.0	ns
FA0	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time	Read	N(12)		N(12)		N(12)		ns
			Write	N(12)		N(12)		N(12)		ns
FA1	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(13) v low	Read	A(1)		A(1)		A(1)		ns
			Write	A(1)		A(1)		A(1)		ns
FA3	$t_{d(nCSV-nADVIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale invalid	Read	B(2) – 0.2	B(2) + 2.0	B(2) – 0.2	B(2) + 2.6	B(2) – 0.2	B(2) + 3.7	ns
			Write	B(2) – 0.2	B(2) + 2.0	B(2) – 0.2	B(2) + 2.6	B(2) – 0.2	B(2) + 3.7	ns
FA4	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Single read)		C(3) – 0.2	C(3) + 2.0	C(3) – 0.2	C(3) + 2.6	C(3) – 0.2	C(3) + 3.7	ns

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Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
FA9	$t_{d(AV-nCSV)}$	Delay time, address bus valid to gpmc_ncsx(13) valid	J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns
FA10	$t_{d(nBEV-nCSV)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx(13) valid	J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns
FA12	$t_{d(nCSV-nADVV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale valid	K(10) – 0.2	K(10) + 2.0	K(10) – 0.2	K(10) + 2.6	K(10) – 0.2	K(10) + 3.7	ns
FA13	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe valid	L(11) – 0.2	L(11) + 2.0	L(11) – 0.2	L(11) + 2.6	L(11) – 0.2	L(11) + 3.7	ns
FA14	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx(13) valid to gpmc_io_dir high	L(11) – 0.2	L(11) + 2.0	L(11) – 0.2	L(11) + 2.6	L(11) – 0.2	L(11) + 3.7	ns
FA15	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx(13) valid to gpmc_io_dir low	M(14) – 0.2	M(14) + 2.0	M(14) – 0.2	M(14) + 2.6	M(14) – 0.2	M(14) + 3.7	ns
FA16	$t_{w(AIV)}$	Address invalid duration between 2 successive R/W accesses	G(7)		G(7)		G(7)		ns
FA18	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Burst read)	I(8) – 0.2	I(8) + 2.0	I(8) – 0.2	I(8) + 2.6	I(8) – 0.2	I(8) + 3.7	ns
FA20	$t_{w(AV)}$	Pulse duration, address valid – 2nd, 3rd, and 4th accesses	D(4)		D(4)		D(4)		ns
FA25	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nwe valid	E(5) – 0.2	E(5) + 2.0	E(5) – 0.2	E(5) + 2.6	E(5) – 0.2	E(5) + 3.7	ns
FA27	$t_{d(nCSV-nWEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nwe invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 2.6	F(6) – 0.2	F(6) + 3.7	ns
FA28	$t_{d(nWEV-DV)}$	Delay time, gpmc_ new valid to data bus valid		2.0		2.6		3.7	ns
FA29	$t_{d(DV-nCSV)}$	Delay time, data bus valid to gpmc_ncsx(13) valid	J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns
FA37	$t_{d(nOEV-AIV)}$	Delay time, gpmc_noe valid to gpmc_a[16:1]_d[15:0] address phase end		2.0		2.6		3.7	ns

(1) **For single read:** A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n being the page burst access number

(2) **For reading:** B = ((ADVRdOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

(3) C = ((OEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(4) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(5) E = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(6) F = ((WEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(7) G = Cycle2CycleDelay * GPMC_FCLK

(8) I = ((OEOffTime + (n – 1) * PageBurstAccessTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(9) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK

(10) K = ((ADVOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

(11) L = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(12) **For single read:** N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(13) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(14) M = ((RdCycleTime - CSOnTime) * (TimeParaGranularity + 1) - 0.5 * CSExtraDelay) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non-multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behavior is automatically handled by GPMC controller.

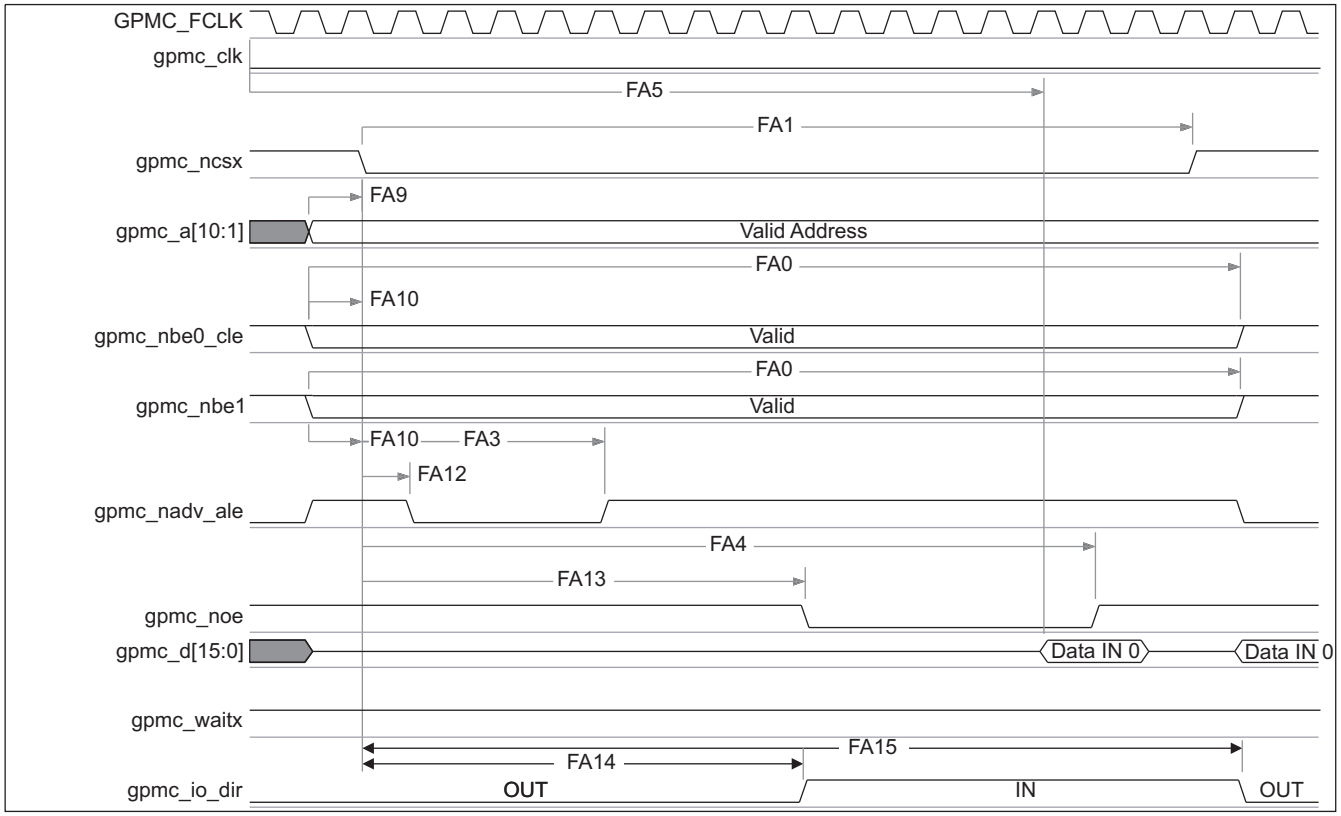

Figure 6-7. GPMC/NOR Flash – Asynchronous Read – Single Word Timing[(1)(2)(3)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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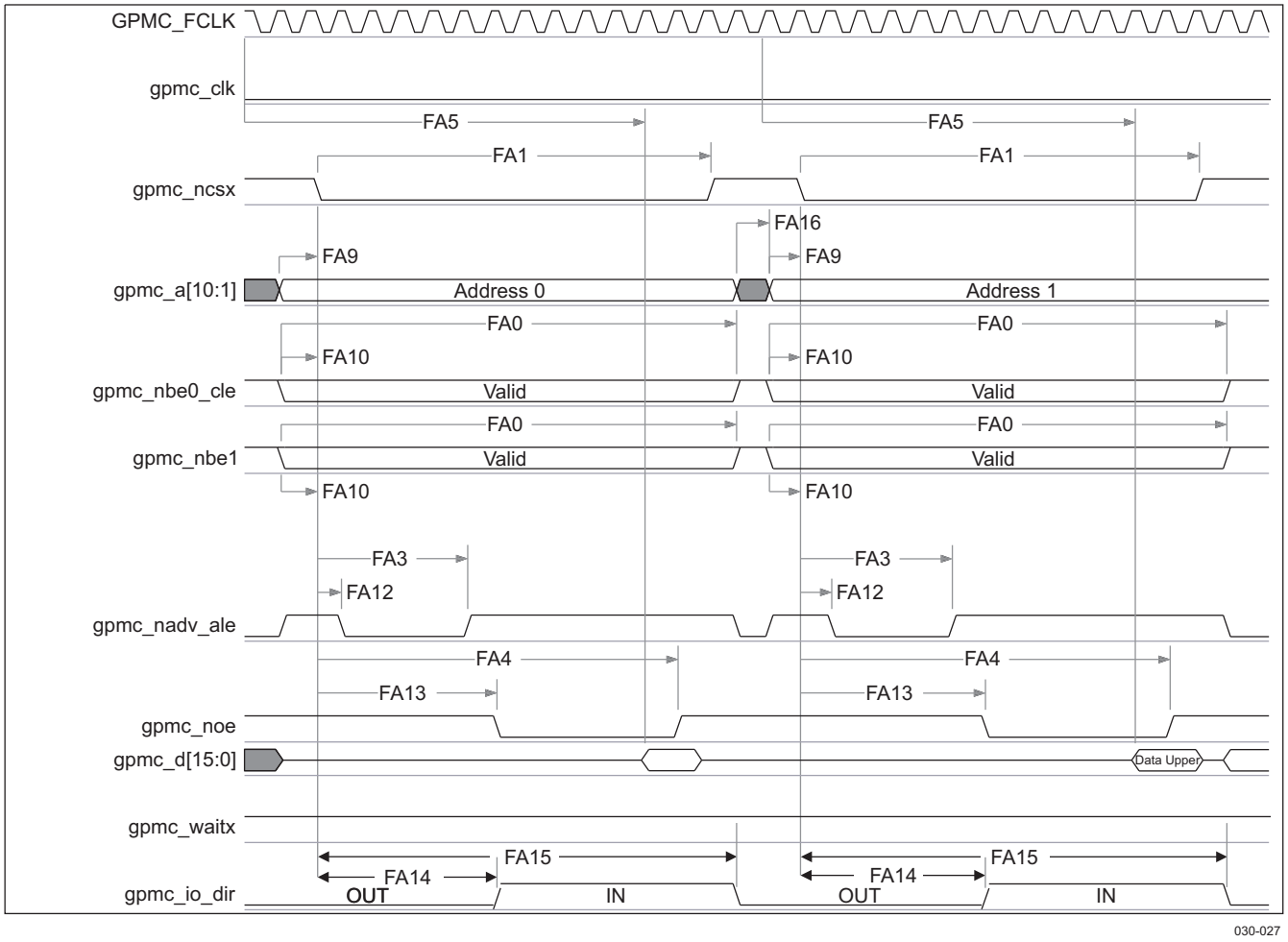


Figure 6-8. GPMC/NOR Flash – Asynchronous Read – 32-bit Timing[(1)(2)(3)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

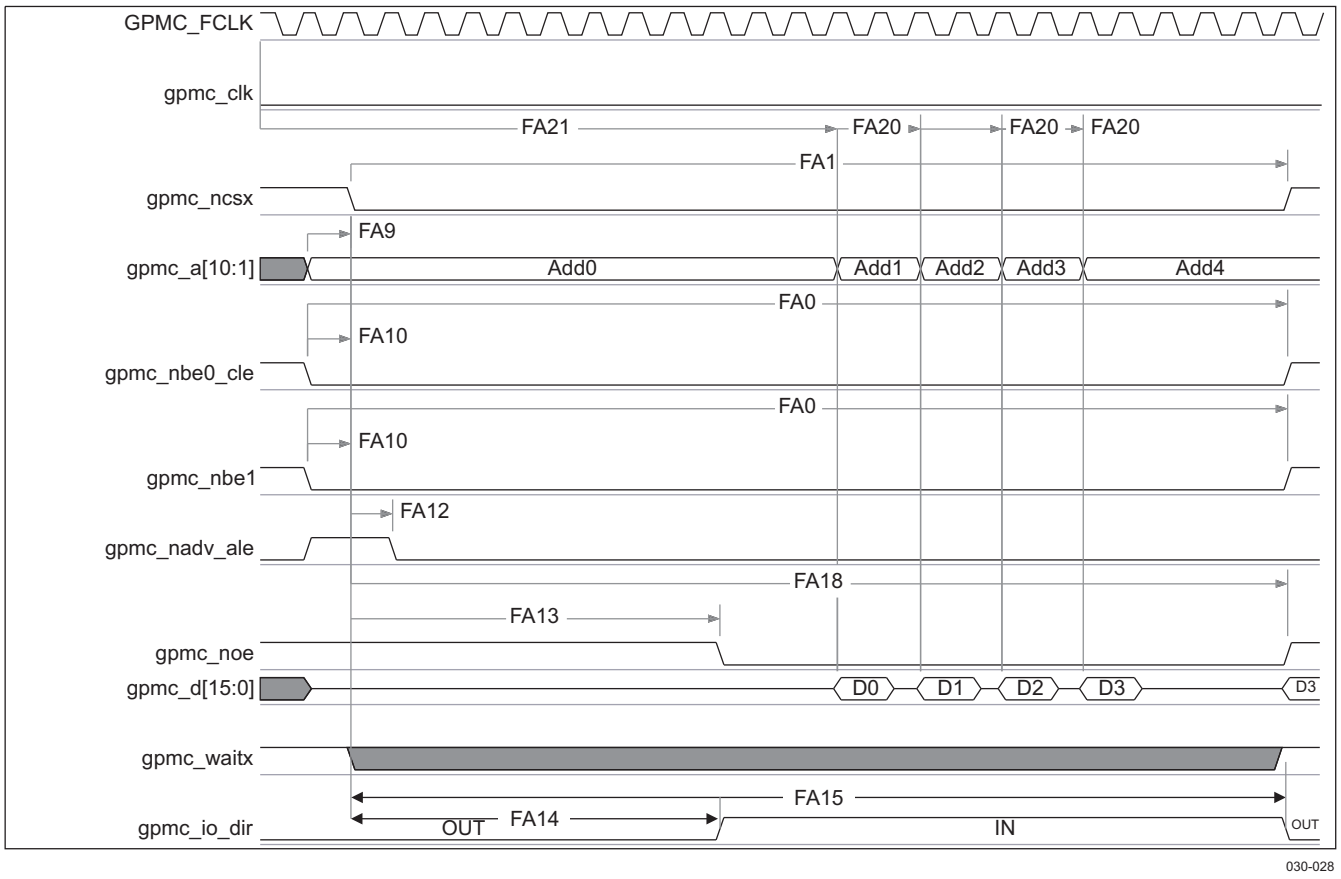


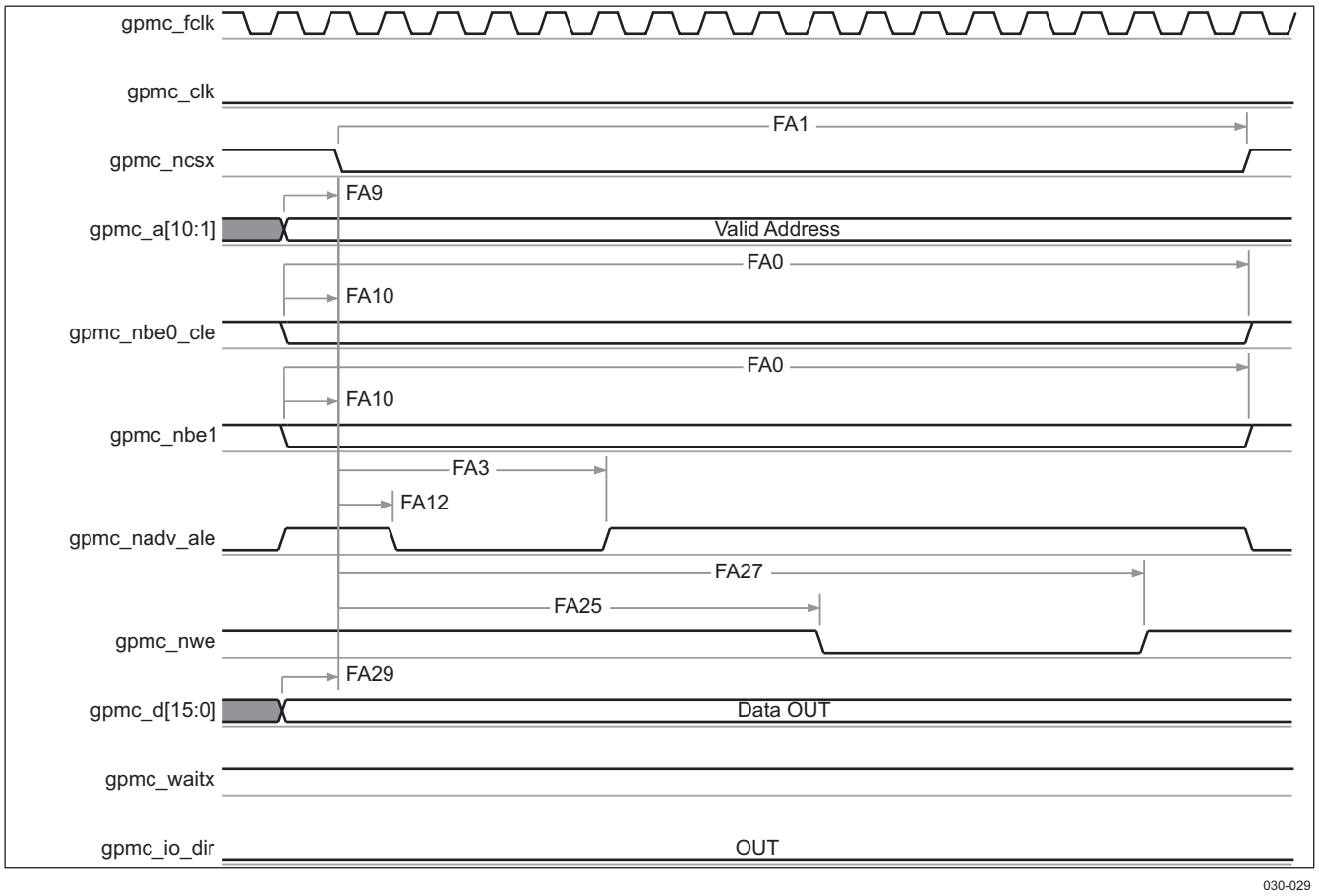
Figure 6-9. GPMC/NOR Flash – Asynchronous Read – Page Mode 4x16-bit Timing[(1)(2)(3)(4)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside AccessTime register bit field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bit field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-10. GPMC/NOR Flash – Asynchronous Write – Single Word Timing

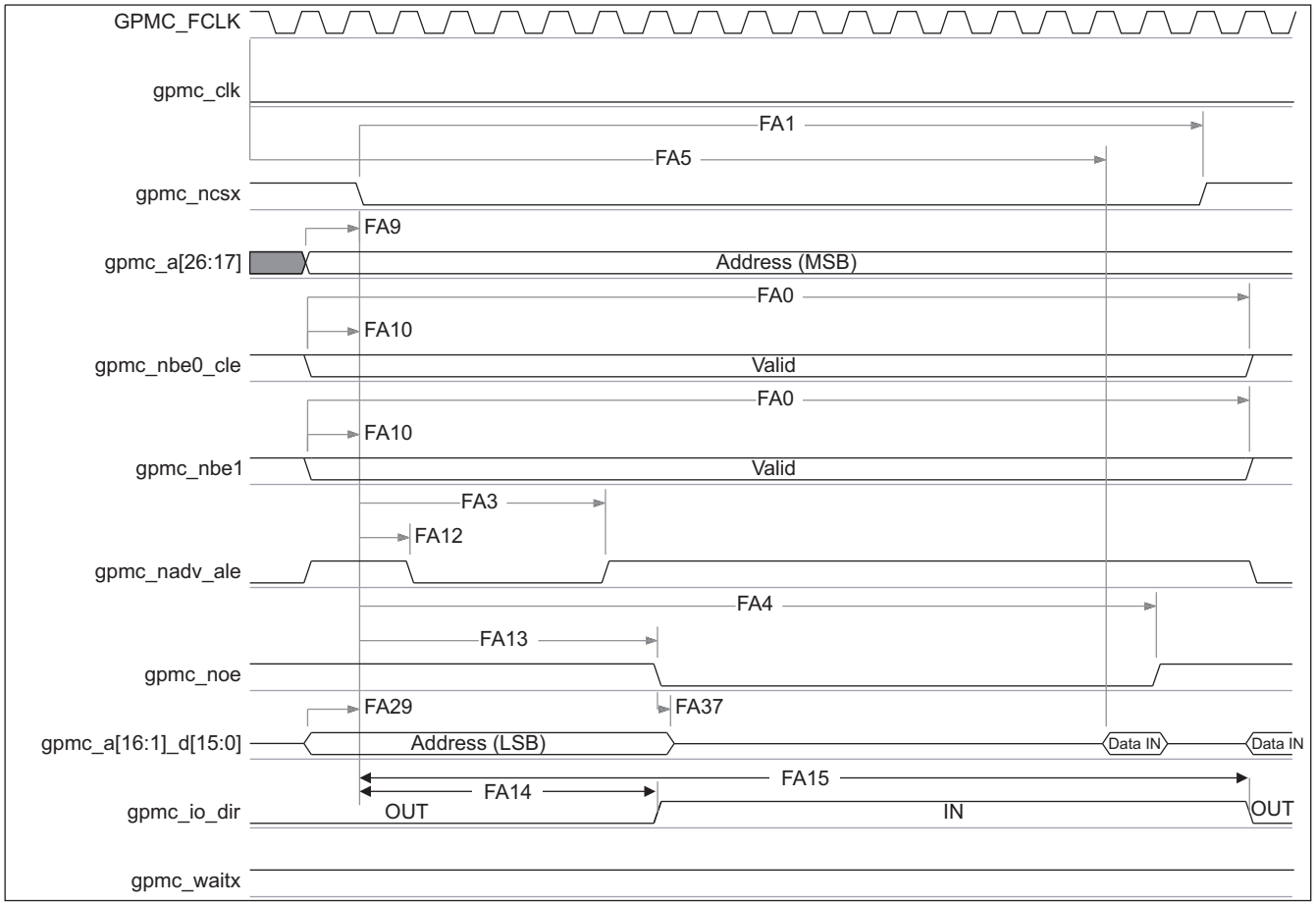


Figure 6-11. GPMC/Multiplexed NOR Flash – Asynchronous Read – Single Word Timing(1)(2)(3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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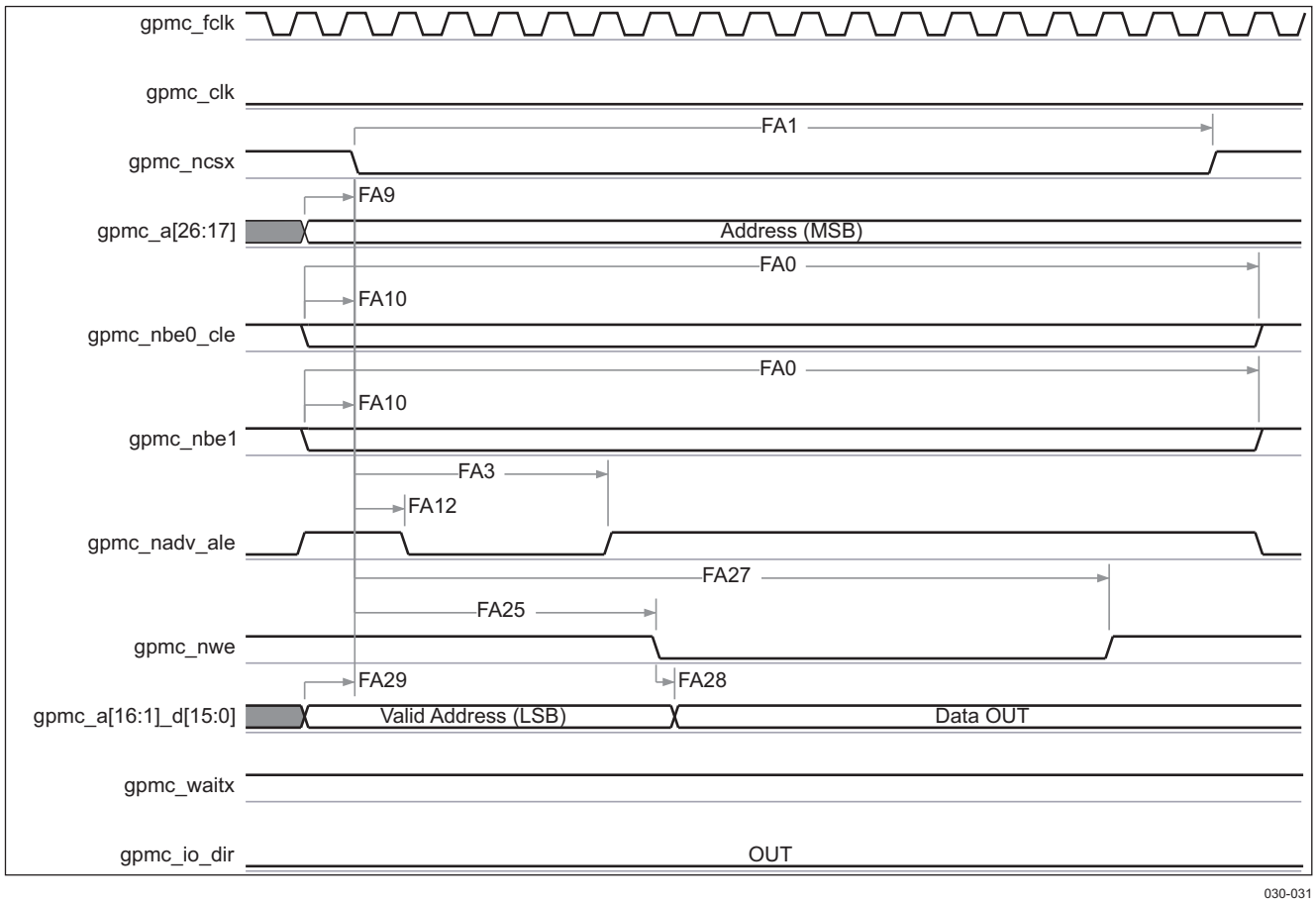

In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-12. GPMC/Multiplexed NOR Flash – Asynchronous Write – Single Word Timing

6.4.1.3 GPMC/NAND Flash Interface Timing

Table 6-10 through Table 6-12 assume testing over the recommended operating conditions (see Figure 6-13 through Figure 6-16) and electrical characteristic conditions.

Table 6-9. GPMC/NAND Flash Asynchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time		1.8	ns
t_F	Input signal fall time		1.8	ns
C_{LOAD}	Output load capacitance		55	pF

Table 6-10. GPMC/NAND Flash Interface Asynchronous Timing Internal Parameters(1)(2)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
GNFI1	Maximum output data generation delay from internal functional clock		6.5		9.1		13.7	ns

(1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.
(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

Table 6-10. GPMC/NAND Flash Interface Asynchronous Timing Internal Parameters (continued)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
GNFI2	Maximum input data capture delay by internal functional clock		4		5.6		8.1	ns
GNFI3	Maximum device select generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI4	Maximum address latch enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI5	Maximum command latch enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI6	Maximum output enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI7	Maximum write enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI8	Maximum functional clock skew		100		170		200	ps

Table 6-11. GPMC/NAND Flash Interface Timing Requirements

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
GNF12[1]	$t_{acc(DAT)}$	Data maximum access time		J[2]	GPMC_FCLK cycles

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime * (TimeParaGranularity + 1)

Table 6-12. GPMC/NAND Flash Interface Switching Characteristics

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
	$t_{R(DO)}$	Rise time, output data		2.0	ns
	$t_{F(DO)}$	Fall time, output data		2.0	ns
GNF0	$t_{w(nWEV)}$	Pulse duration, gpmc_nwe valid time	A[1]		ns
GNF1	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx[13] valid to gpmc_nwe valid	B[2] - 0.2	B[2] + 2.0	ns
GNF2	$t_{w(CLEH-nWEV)}$	Delay time, gpmc_nbe0_cle high to gpmc_nwe valid	C[3] - 0.2	C[3] + 2.0	ns
GNF3	$t_{w(nWEV-DV)}$	Delay time, gpmc_d[15:0] valid to gpmc_nwe valid	D[4] - 0.2	D[4] + 2.0	ns
GNF4	$t_{w(nWEIV-DIV)}$	Delay time, gpmc_nwe invalid to gpmc_d[15:0] invalid	E[5] - 0.2	E[5] + 2.0	ns
GNF5	$t_{w(nWEIV-CLEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nbe0_cle invalid	F[6] - 0.2	F[6] + 2.0	ns
GNF6	$t_{w(nWEIV-nCSIV)}$	Delay time, gpmc_nwe invalid to gpmc_ncsx[13] invalid	G[7] - 0.2	G[7] + 2.0	ns
GNF7	$t_{w(ALEH-nWEV)}$	Delay time, gpmc_nadv_ale High to gpmc_nwe valid	C[3] - 0.2	C[3] + 2.0	ns
GNF8	$t_{w(nWEIV-ALEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nadv_ale invalid	F[6] - 0.2	F[6] + 2.0	ns
GNF9	$t_{c(nWE)}$	Cycle time, Write cycle time	H[8]		ns
GNF10	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx[13] valid to gpmc_noe valid	I[9] - 0.2	I[9] + 2.0	ns
GNF13	$t_{w(nOEV)}$	Pulse duration, gpmc_noe valid time	K[10]		ns
GN F14	$t_{c(nOE)}$	Cycle time, Read cycle time	L[11]		ns

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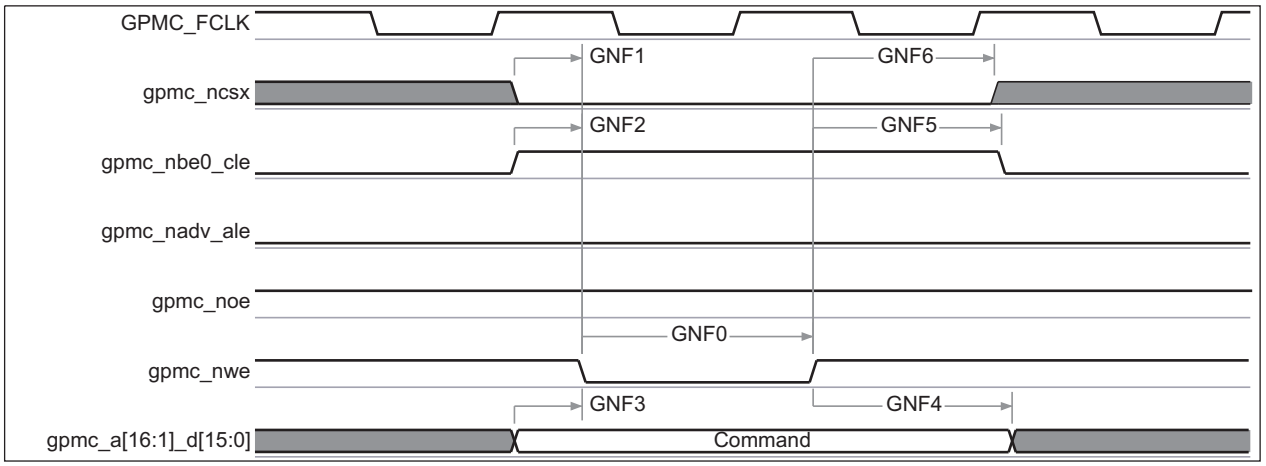
Table 6-12. GPMC/NAND Flash Interface Switching Characteristics (continued)

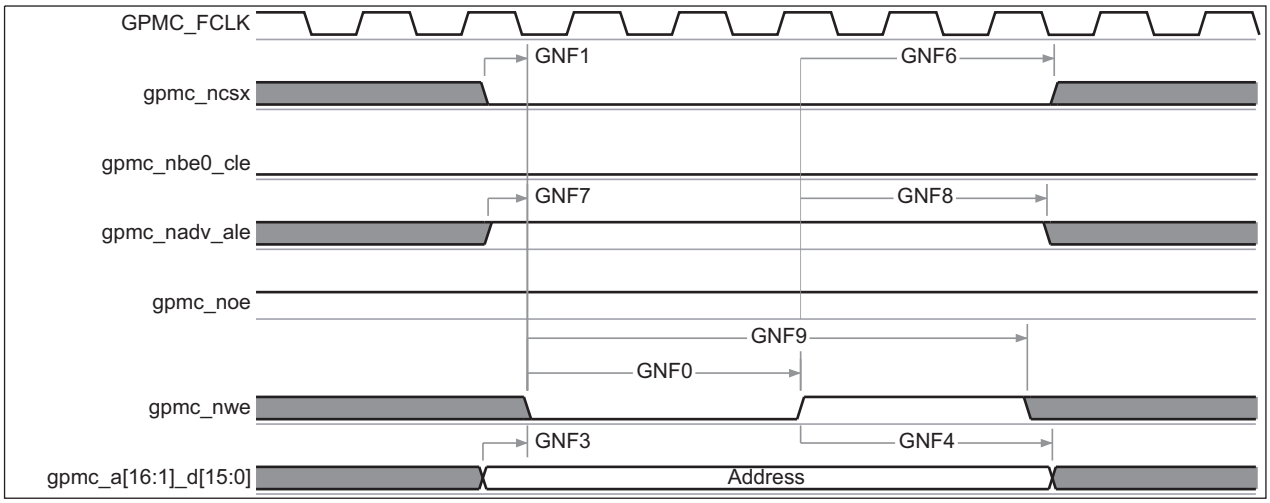
NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
GNF15	$t_{w(nOEIV-nCSIV)}$	Delay time, gpmc_noe invalid to gpmc_ncsx(13) invalid	M(12) - 0.2	M(12) + 2.0	ns

(1) A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(3) C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – ADVExtraDelay)) * GPMC_FCLK
(4) D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK
(5) E = (WrCycleTime – WEOffTime * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK
(6) F = (ADVWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay) * GPMC_FCLK
(7) G = (CSWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(12) M = (CSRdOffTime – OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – OEExtraDelay) * GPMC_FCLK
(13) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

Figure 6-13. GPMC/NAND Flash – Command Latch Cycle Timing



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

Figure 6-14. GPMC/NAND Flash – Address Latch Cycle Timing

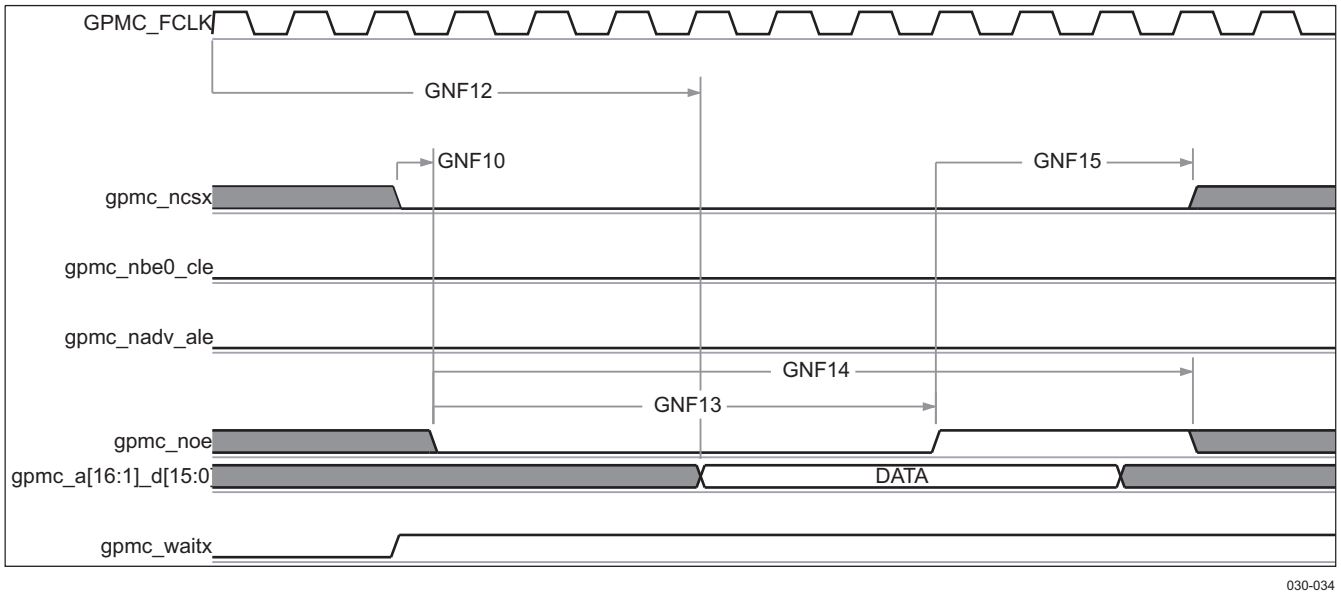
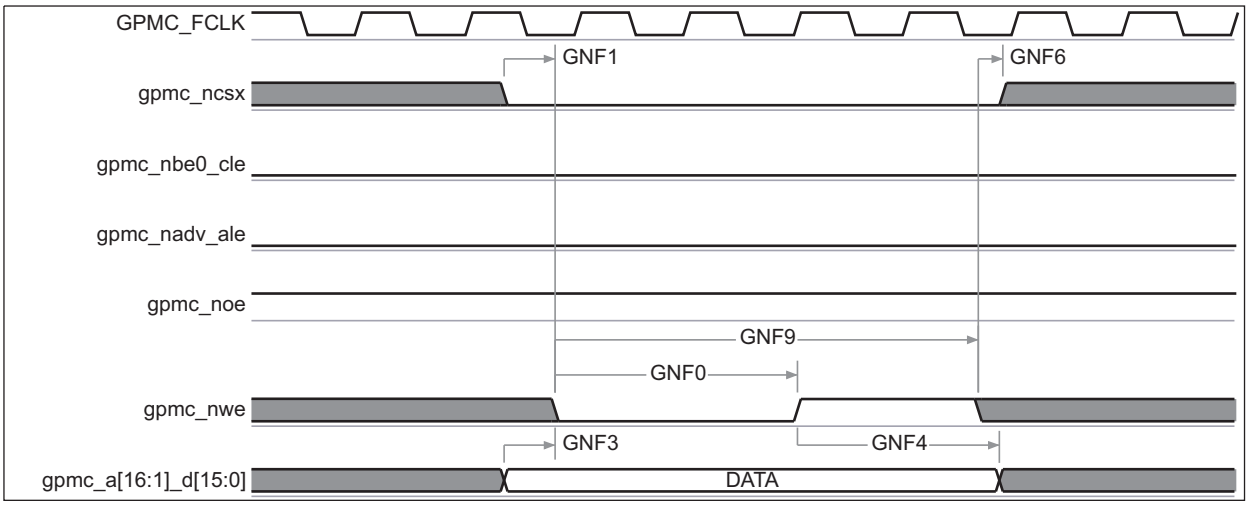


Figure 6-15. GPMC/NAND Flash – Data Read Cycle Timing(1)(2)(3)

(1) The GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data is internally sampled by active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0 ,1, 2, or 3.



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0 or 1.

Figure 6-16. GPMC/NAND Flash – Data Write Cycle Timing

6.4.2 DDR2 Memory Controller

The DDR2 Memory Controller is a dedicated interface to DDR2 SDRAM. It supports JESD79D-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices. DDR2 SDRAM plays a key role in an AM3517/05-based system. Such a system is expected to require a significant amount of high-speed external memory for all of the following functions:

- Buffering of input image data from sensors or video sources
- Intermediate buffering for processing/resizing of image data in the VPFE
- Numerous OSD display buffers
- Intermediate buffering for large raw Bayer data image files while performing image processing functions
- Buffering for intermediate data while performing video encode and decode functions
- Storage of executable code for the ARM

The DDR2 Memory Controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- Mobile DDR SDRAM
- 256 MByte memory space
- Data bus width 16 bits
- CAS latencies:
  - DDR2: 2, 3, 4, and 5
- Internal banks:
  - DDR2: 1, 2, 4, and 8
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Partial array self-refresh
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

6.4.3 DDR2 Memory Controller Electrical Data/Timing

Table 6-13. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller(1)(2)(see)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(sdrc\_clk)}$ Cycle time, sdrc_clk	333-DDR2 (supported for 216-MHz device)	90	TBD	MHz
		216-DDR2 (supported for 270-MHz device)	90	216	
		243-DDR2 (supported for 300-MHz device)	90	243	

(1) sdrc_clk cycle time = 2 x PLLC1.SYSCLK7 or 2 x PLLC2.SYSCLK3 cycle time.
(2) The PLL2 Controller ***must*** be programmed such that the resulting sdrc_nclk clock frequency is within the specified range.

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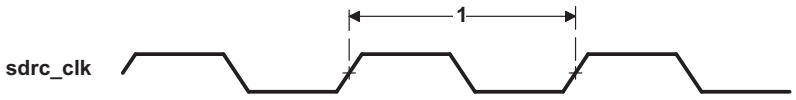

Figure 6-17. DDR2 Memory Controller Clock Timing

6.4.3.1 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2 specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

6.4.3.1.1 DDR2 Interface Schematic

Figure 6-18 shows the DDR2 interface schematic for a single-memory DDR2 system. The dual-memory system shown in Figure 6-19. Pin numbers for the AM3517/05 can be obtained from the pin description section.

6.4.3.1.2 Compatible JEDEC DDR2 Devices

Table 6-14 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2 speed grade DDR2 devices.

The AM3517/05 also supports JEDEC DDR2 x8 devices in the dual chip configuration. In this case, one chip supplies the upper byte and the second chip supplies the lower byte. Addresses and most control signals are shared just like regular dual chip memory configurations.

Table 6-14. Compatible JEDEC DDR2 Devices

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2 Device Speed Grade	DDR2-333 MHz			See Note (1)
2	JEDEC DDR2 Device Bit Width	x16	x32	Bits	
3	JEDEC DDR2 Device Count	1	2	Devices	
4	JEDEC DDR2 Device Ball Count	84	92	Balls	See Note (2)

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) 92 ball devices retained for legacy support. New designs will migrate to 84 ball DDR2 devices. Electrically, the 92 and 84 ball DDR2 devices are the same.

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6.4.3.1.3 PCB Stackup

The minimum stackup required for routing the AM3517/05 is a six layer stack as shown in Table 6-15. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.

Table 6-15. Minimum PCB Stack Up

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

Complete stack up specifications are provided in Table 6-16.

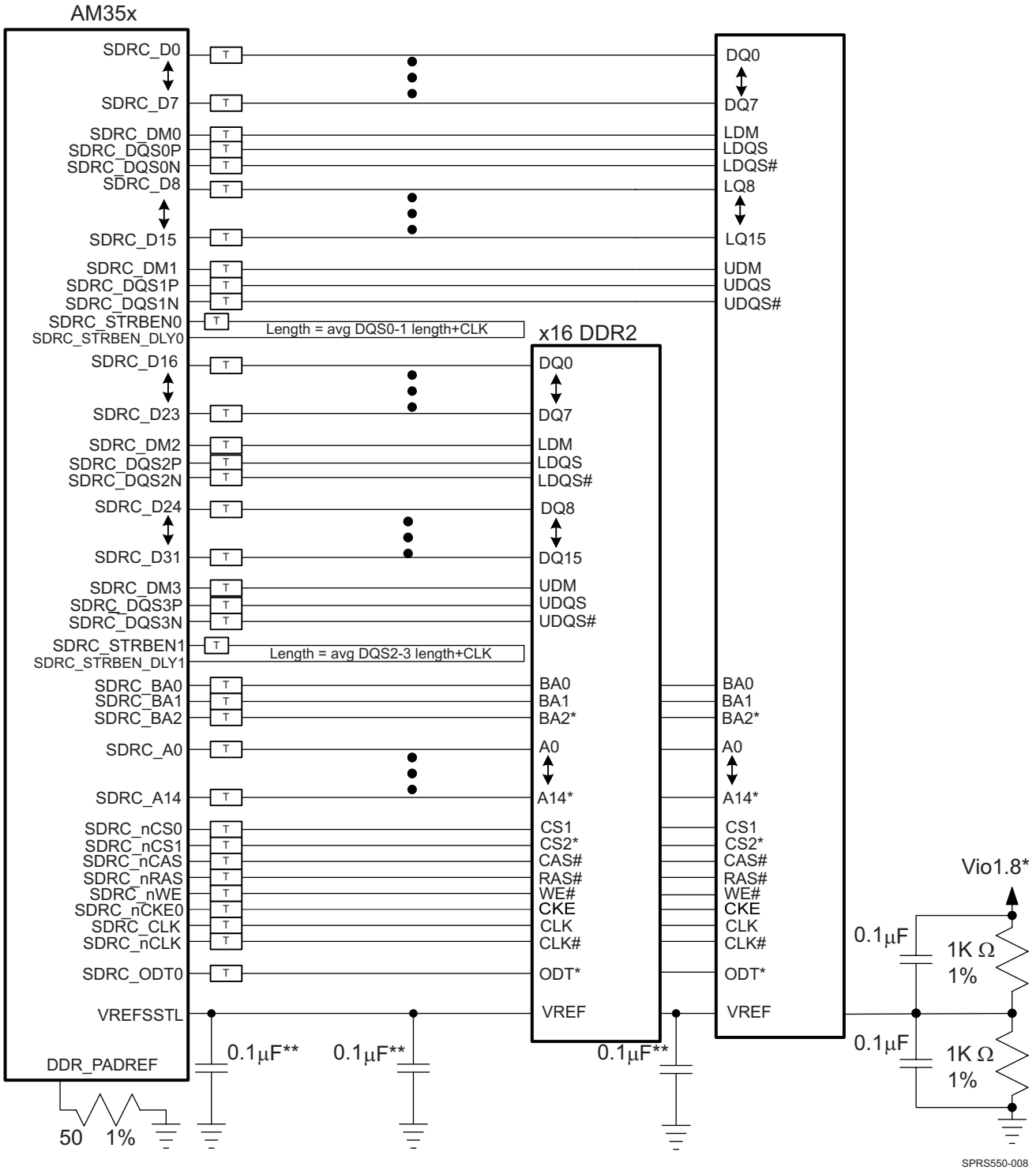

Figure 6-18. DDR2 Single-Memory High Level Schematic

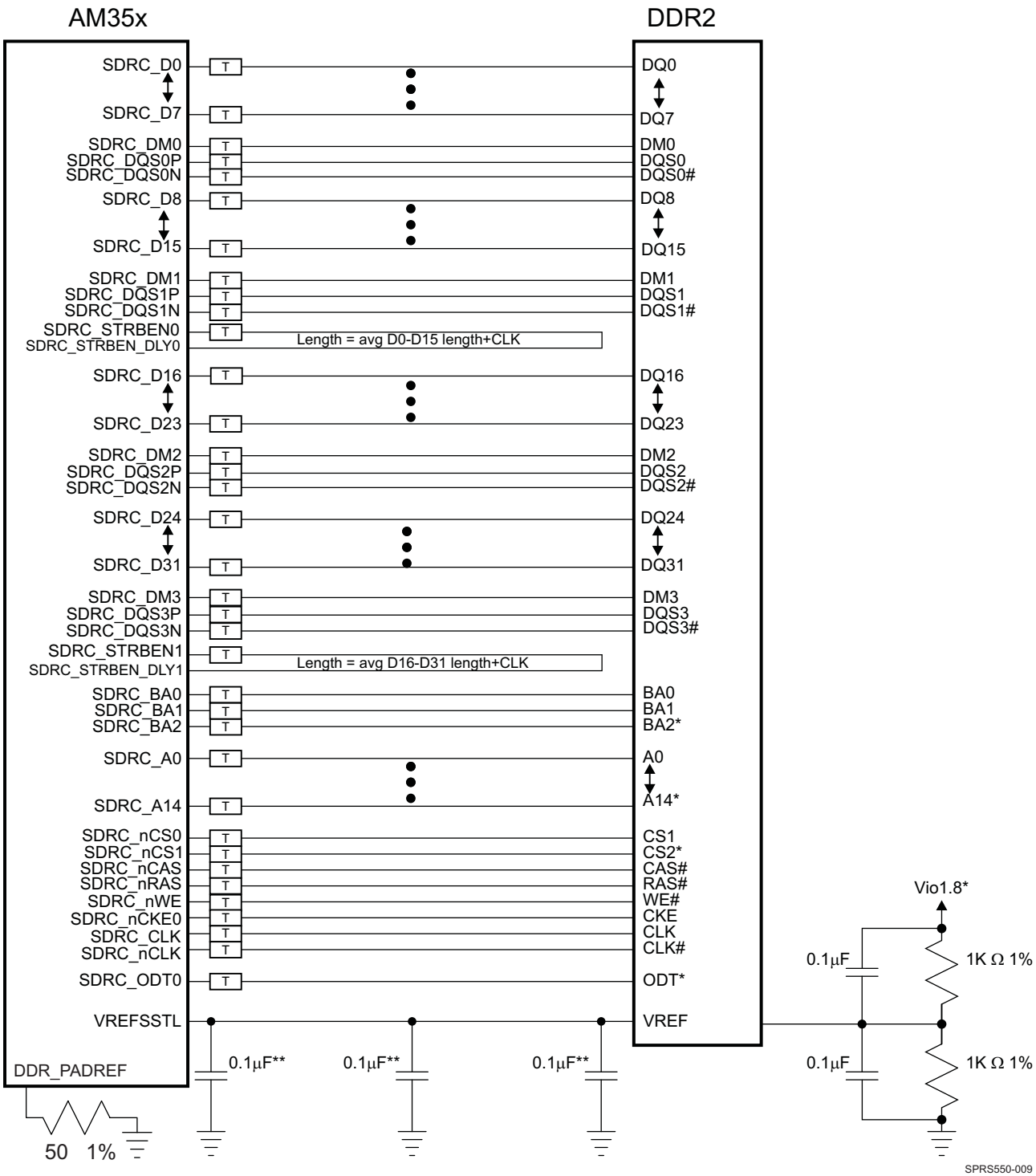

Figure 6-19. DDR2 Dual-Memory High Level Schematic

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Table 6-16. PCB Stack Up Specifications

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PCB Routing/Plane Layers	6				
2	Signal Routing Layers	3				
3	Full ground layers under DDR2 routing Region	2				
4	Number of ground plane cuts allowed within DDR routing region			0		
5	Number of ground reference planes required for each DDR2 routing layer	1				
6	Number of layers between DDR2 routing layer and ground plane			0		
7	PCB Routing Feature Size		4		Mils	
8	PCB Trace Width w		4		Mils	
9	PCB BGA escape via pad size		20		Mils	
10	PCB BGA escape via hole size		10		Mils	
11	AM3517/05 BGA pad size		12			See Note (1)
12	DDR2 Device BGA pad size					See Note (2)
13	Single Ended Impedance, Zo	50		75	Ω	
14	Impedance Control	Z-5	Z	Z+5	Ω	See Note (3)

(1) The recommended pad size is 0.3 mm per IPC-7351 specification.
(2) Please refer to IPC standard IPC-7351 or manufacturer's recommendations for correct BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

6.4.3.1.4 Placement

Figure 6-19 shows the required placement for the DDR2 devices. The dimensions for Figure 6-20 are defined in Table 6-17. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2 systems, the second DDR2 device is omitted from the placement.

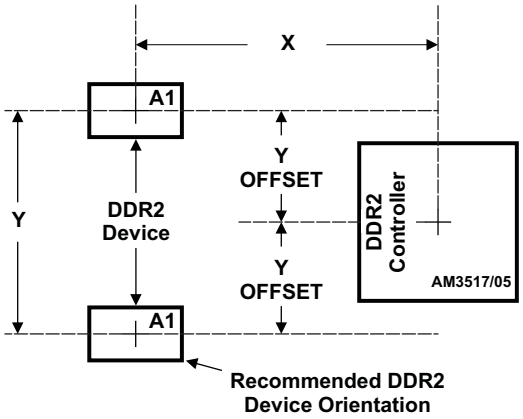


Figure 6-20. DDR2 Device Placement

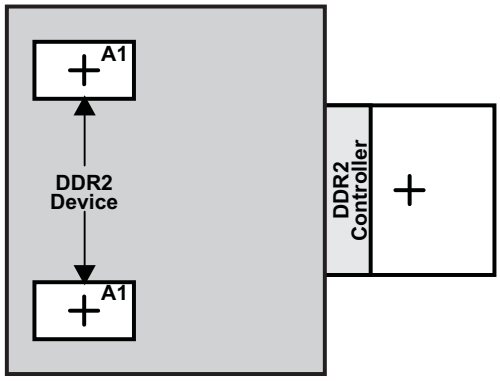
Table 6-17. Placement Specifications

No.	Parameter	Min	Max	Unit	Notes
1	X		1750	Mils	See Notes (1), (2)
2	Y		1280	Mils	See Notes (1), (2)
3	Y Offset		650	Mils	See Notes (1), (2), (3)
4	DDR2 Keepout Region				See Note (4)
5	Clearance from non-DDR2 signal to DDR2 Keepout Region	4		w	See Note (5)

(1) See Figure 6-18 for dimension definitions.
(2) Measurements from center of AM3517/05 device to center of DDR2 device.
(3) For single memory systems it is recommended that Y Offset be as small as possible.
(4) DDR2 Keepout region to encompass entire DDR2 routing area
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

6.4.3.1.5 DDR2 Keep Out Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keep out region is defined for this purpose and is shown in Figure 6-21. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 6-17.



Region should encompass all DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keep out region. Non-DDR2 signals may be routed in the region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 6-21. DDR2 Keepout Region

6.4.3.1.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 6-18 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the AM3517/05 and DDR2 interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

Table 6-18. Bulk Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	V_{DD18_DDR} Bulk Bypass Capacitor Count	3		Devices	See Note (1)
2	V_{DD18_DDR} Bulk Bypass Total Capacitance	30		uF	
3	DDR#1 Bulk Bypass Capacitor Count	1		Devices	See Note (1)
4	DDR#1 Bulk Bypass Total Capacitance	22		uF	
5	DDR#2 Bulk Bypass Capacitor Count	1		Devices	See Notes (1), (2)
6	DDR#2 Bulk Bypass Total Capacitance	22		uF	See Note (2)

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on dual-memory systems

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6.4.3.1.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, AM3517/05/DDR2 power, and AM3517/05/DDR2 ground connections. Table 6-19 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

6.4.3.1.8 Net Classes

Table 6-20 lists the clock net classes for the DDR2 interface. Table 6-21 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 6-19. High-Speed Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	HS Bypass Capacitor Package Size		0402	10 Mils	See Note (1)
2	Distance from HS bypass capacitor to device being bypassed		250	Mils	
3	Number of connection vias for each HS bypass capacitor	2		Vias	See Note (2)
4	Trace length from bypass capacitor contact to connection via	1	30	Mils	
5	Number of connection vias for each DDR2 device power or ground balls	1		Vias	
6	Trace length from DDR2 device power ball to connection via		35	Mils	
7	V_{DD18_DDR} HS Bypass Capacitor Count	20		Devices	See Note (3)
8	V_{DD18_DDR} HS Bypass Capacitor Total Capacitance	1.2		µF	
9	DDR#1 HS Bypass Capacitor Count	8		Devices	See Note (3)
10	DDR#1 HS Bypass Capacitor Total Capacitance	0.4		µF	
11	DDR#2 HS Bypass Capacitor Count	8		Devices	See Notes (3), (4)
12	DDR#2 HS Bypass Capacitor Total Capacitance	0.4		µF	See Note (4)

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on dual-memory systems

Table 6-20. Clock Net Class Definitions

Clock Net Class	AM3517/05 Device Pin Names
CK	sdrc_clk/sdrc_nclk
DQS0	sdrc_dqs0p /sdrc_dqs0n
DQS1	sdrc_dqs1p /sdrc_dqs1n

Table 6-21. Signal Net Class Definitions

Clock Net Class	Associated Clock Net Class	AM3517/05 Device Pin Names
ADDR_CTRL	CK	sdrc_ba[2:0], sdrc_a[13:0], sdrc_ncs0 , sdrc_ncas, sdrc_nras, sdrc_nwe, sdrc_cke0
DQ0	DQS0	sdrc_d[7:0], sdrc_dm0
DQ1	DQS1	sdrc_d[15:8], sdrc_dm1
SDRC_STRBENx	CK, DQS0, DQS1	sdrc_strben0, sdrc_strben_dly0

6.4.3.1.9 DDR2 Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-22 shows the specifications for the series terminators.

Table 6-22. DDR2 Signal Terminations

No.	Parameter	Min	Typ	Max	Unit	Notes
1	CLK Net Class	0		10	Ω	See Note (1)
2	ADDR_CTRL Net Class	0	22	Zo	Ω	See Notes (1), (2), (3)
3	Data Byte Net Classes (DQS0-DQS1, D0-D31)	0	22	Zo	Ω	See Notes (1), (2), (3), (4)
4	SDRC_STRBENx Net Class (SDRC_STRBENx)	0	10	Zo	Ω	See Notes (1), (2), (3)

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ωs), the DDR2 devices must be programmed to operate in 60% strength mode.

6.4.3.1.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2 memories as well as the AM3517/05. VREF is intended to be = the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 6-18. Other methods of creating VREF are not recommended. Figure 6-22 shows the layout guidelines for VREF.

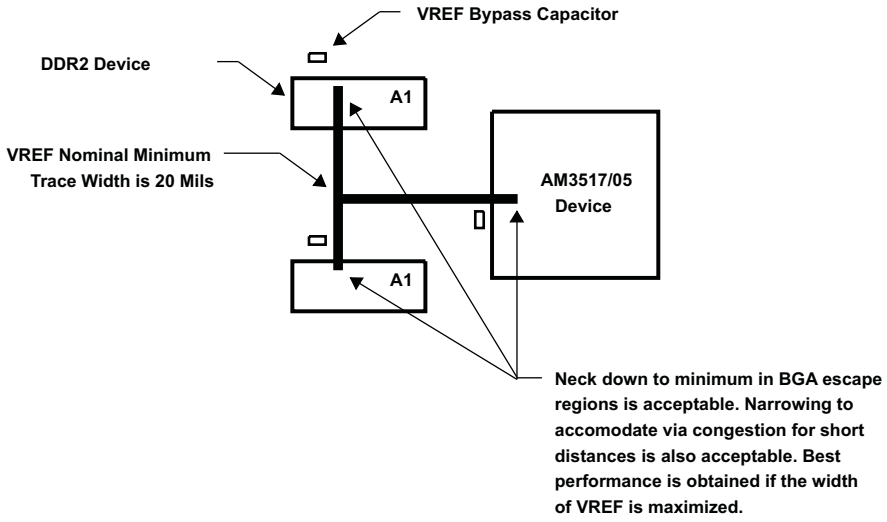

Figure 6-22. VREF Routing and Topology

6.4.3.1.11 DDR2 CLK and ADDR_CTRL Routing

Figure 6-23 shows the topology of the routing for the CLK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

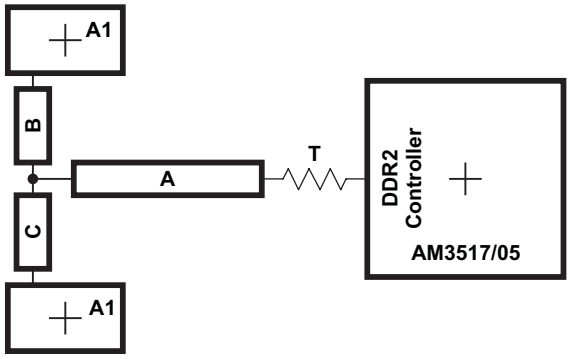

Figure 6-23. CLKand ADDR_CTRL Routing and Topology

PRODUCT PREVIEW

Table 6-23. CLKand ADDR_CTRL Routing Specification (1)

No	Parameter	Min	Typ	Max	Unit	Notes
1	Center to center DQS-DQSN spacing			2w		
2	CLKA to B/A to C Skew Length Mismatch			25	Mils	See Note (1)
3	CLKB to C Skew Length Mismatch			25	Mils	
4	Center to center CLKto other DDR2 trace spacing	4w				See Note (2)
5	CK/ADDR_CTRL nominal trace length	CACLM-50	CACLM	CACLM+50	Mils	See Note (3)
6	ADDR_CTRL to CLKSkew Length Mismatch			100	Mils	
7	ADDR_CTRL to ADDR_CTRL Skew Length Mismatch			100	Mils	
8	Center to center ADDR_CTRL to other DDR2 trace spacing	4w				See Note (2)
9	Center to center ADDR_CTRL to other ADDR_CTRL trace spacing	3w				See Note (2)
10	ADDR_CTRL A to B/A to C Skew Length Mismatch			100	Mils	See Note (1)
11	ADDR_CTRL B to C Skew Length Mismatch			100	Mils	

(1) Series terminator, if used, should be located closest to AM3517/05.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CLKand ADDR_CTRL net classes.

Figure 6-24 shows the topology and routing for the DQS and Dx net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

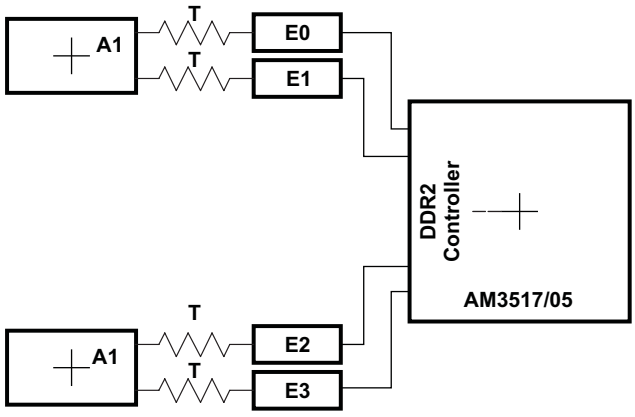

Figure 6-24. DQS and Dx Routing and Topology

Table 6-24. DQS and Dx Routing Specification(1) (2)

No.	Parameter	Min	Typ	Max	Unit	Notes
1	Center to center DQS-DQSN spacing			2w		
2	DQS E Skew Length Mismatch			25	Mils	
3	Center to center DQS to other DDR2 trace spacing	4w				See Note (3)
4	DQS/Dx nominal trace length	DQLM-50	DQLM	DQLM+ 50	Mils	See Notes (2), (4)
5	Dx to DQS Skew Length Mismatch			100	Mils	See Note (4)
6	Dx to Dx Skew Length Mismatch			100	Mils	See Note (4)
7	Center to center Dx to other DDR2 trace spacing	4w				See Notes (3), (5)
8	Center to Center Dx to other Dx trace spacing	3w				See Notes (6), (3)
9	Dx/DQS E Skew Length Mismatch			100	Mils	See Note (4)

(1) "Dx" indicates a data line.
(2) Series terminator, if used, should be located closest to DDR.
(3) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(4) There is no need and it is not recommended to skew match across data bytes, i.e., from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) Dx's from other DQS domains are considered *other DDR2 trace*.
(6) DQLM is the longest Manhattan distance of each of the DQS and Dx net classes.

Figure 6-25 shows the routing for the SDRC_STRBENx net classes. Table 6-25 contains the routing specification.

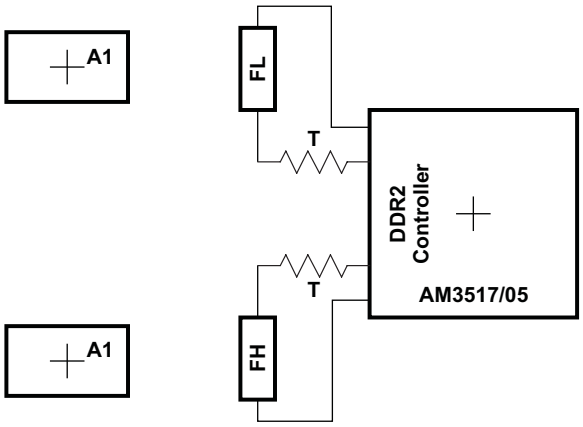

Figure 6-25. SDRC_STRBENx Routing

Table 6-25. SDRC_STRBENx Routing Specification

No.	Parameter	Min	Typ	Max	Unit	Notes
1	SDRC_STRBEN0 Length F		CKB0B1			See Note (1)
	SDRC_STRBEN1 Length F		CKB0B2			See Note (2)
3	Center to center SDRC_STRBENx to any other trace spacing	4w				
4	DQS/Dx nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	
5	SDRC_STRBENx Skew			100	Mils	See Note (3)

(1) CKB0B1 is the sum of the length of the CLK net plus the average length of the DQS0 and DQS1 nets.
(2) CKB0B2 is the sum of the length of the CLK net plus the average length of the DQS2 and DQS3 nets.
(3) Skew from CKB0B1 or CKB0B2.

6.5 Video Interfaces

6.5.1 Video Processing Subsystem (VPSS)

The Video Processing Sub-System (VPSS) provides a Video Processing Front End (VPFE) input interface for external imaging peripherals (i.e., image sensors, video decoders, etc.).

6.5.1.1 Video Processing Front End (VPFE)

The Video Processing Front-End (VPFE) controller receives input video/image data from external capture devices and stores it to external memory which is transferred into the external memory via a built in DMA engine. An internal buffer block provides a high bandwidth path between the VPSS module and the external memory. The Cortex-A8 will process the image data based on application requirements.

6.5.1.1.1 Video Processing Front End (VPFE) Timing

Table 6-26, , and Table 6-27 assume testing over recommended operating conditions (see Figure 6-26 through Figure 6-28).

Table 6-26. VPFE Timing Requirements

NO.	PARAMETER		1.8-V, 3.3-V		
			MIN	MAX	UNIT
VF1	$t_{c(VDIN\_CLK)}$	Cycle time, pixel clock input, VDIN_CLK	13.33	100	ns
VF2	$t_{su(VDIN\_D-VDIN\_CLK)}$	Setup time, VDIN_D to VDIN_CLK rising edge	TBD		ns
VF3	$t_{su(VDIN\_HD-VDIN\_CLK)}$	Setup time, VDIN_HD to VDIN_CLK rising edge	TBD		ns
VF4	$t_{su(VDIN\_VD-VDIN\_CLK)}$	Setup time, VDIN_VD to VDIN_CLK rising edge	TBD		ns
VF5	$t_{su(VDIN\_WEN-VDIN\_CLK)}$	Setup time, VDIN_WEN to VDIN_CLK rising edge	TBD		ns
VF6	$t_{su(C\_FLD-VDIN\_CLK)}$	Setup time, VDIN_FIELD to VDIN_CLK rising edge	TBD		ns
VF7	$t_{h(VDIN\_CLK-VDIN\_D)}$	Hold time, VDIN_D valid after VDIN_CLK rising edge	TBD		ns
VF8	$t_{h(VDIN-HD-VDIN\_CLK)}$	Hold time, VDIN_HD to VDIN_CLK rising edge	TBD		ns
VF9	$t_{h(VDIN\_VD-VDIN\_CLK)}$	Hold time, VDIN_VD to VDIN_CLK rising edge	TBD		ns
VF10	$t_{h(VDIN\_WEN-VDIN\_CLK)}$	Hold time, VDIN_WEN to VDIN_CLK rising edge	TBD		ns
VF11	$t_{h(C\_FLD-VDIN\_CLK)}$	Hold time, VDIN_FIELD to VDIN_CLK rising edge	TBD		ns

Table 6-27. VPFE Output Switching Characteristics

NO.	PARAMETER		1.8-V, 3.3-V		
			MIN	MAX	UNIT
VF12	$t_{d(VDIN\_HD-VDIN\_CLK)}$	Output delay time, VDIN_HD to CLK rising edge		TBD	ns
VF13	$t_{d(VDIN\_VD-VDIN\_CLK)}$	Output delay time, VDIN_VD to CLK rising edge		TBD	ns
VF14	$t_{d(VDIN\_WEN-VDIN\_CLK)}$	Output delay time, VDIN_WEN to CLK rising edge		TBD	ns
VF15	$t_{oh(VDIN\_HD-VDIN\_CLK)}$	Output hold time, VDIN_HD to CLK rising edge	TBD		ns
VF16	$t_{oh(VDIN\_VD-VDIN\_CLK)}$	Output hold time, VDIN_VD to CLK rising edge	TBD		ns
VF17	$t_{oh(C\_FLD-VDIN\_CLK)}$	Output hold time, VDIN_FLD to CLK rising edge	TBD		ns

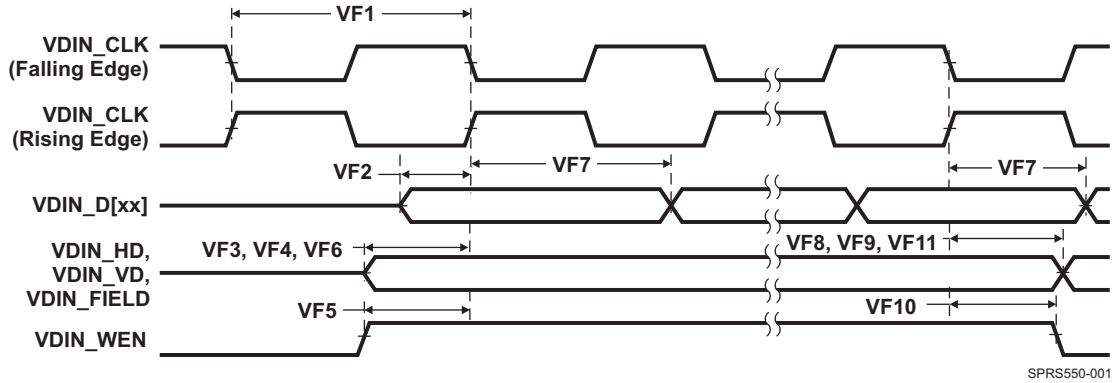

Figure 6-26. VPFE0 Input Timings

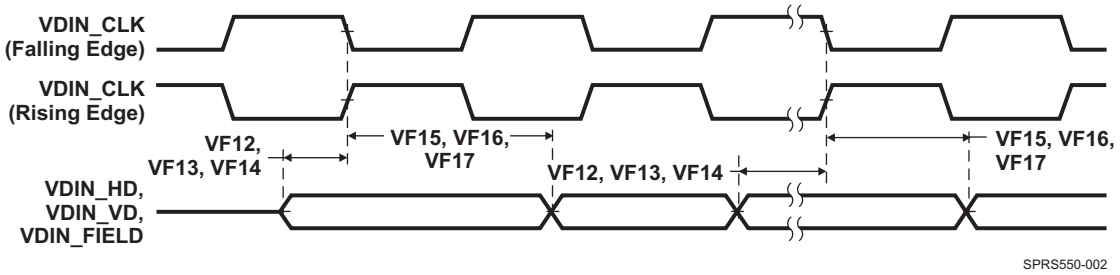

Figure 6-27. VPFE Output Timings

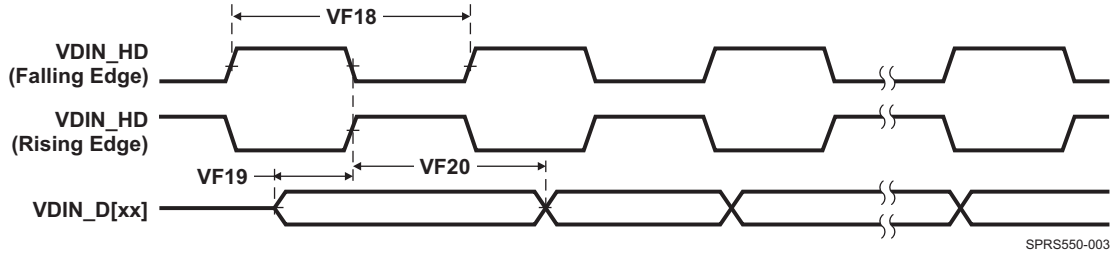

Figure 6-28. VPFE Input Timings With VDIN0_HD as Pixel Clock

6.5.2 Display Subsystem (DSS)

The display subsystem (DSS) provides the logic to display the video frame from external (SDRAM) or internal (SRAM) memory on an LCD panel or a TV set. The DSS integrates a display controller. It can be used in two configurations:

- LCD display support in:
  - Bypass mode (RFBI module bypassed)
  - RFBI mode (through RFBI module)
- TV display support (not discussed in this document because of its analog IO signals)

The two display supports can be active at the same time.

6.5.2.1 LCD Display Support in Bypass Mode

Two types of LCD panel are supported:

- Thin film transistor (TFT) or active matrix technology
- Supertwisted nematic (STN) or passive matrix technology

Both configurations are discussed in the following paragraphs.

6.5.2.1.1 LCD Display in TFT Mode

Table 6-28 assumes testing over the recommended operating conditions (see Figure 6-29).

Table 6-28. LCD Display Interface Switching Characteristics in TFT Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
DL0	$t_{d(PCLKA-HSYNCT)}$	Delay time, dss_pclk active edge to dss_hsync transition	TBD	TBD	ns
DL1	$t_{d(PCLKA-VSYNCT)}$	Delay time, dss_pclk active edge to dss_vsync transition	TBD	TBD	ns
DL2	$t_{d(PCLKA-ACBIASA)}$	Delay time, dss_pclk active edge to dss_acbias active level	TBD	TBD	ns
DL3	$t_{d(PCLKA-DATAV)}$	Delay time, dss_pclk active edge to dss_data bus valid	TBD	TBD	ns

(1) The capacitive load is equivalent to 25 pF.

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Table 6-28. LCD Display Interface Switching Characteristics in TFT Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
DL4	$t_{c(PCLK)}$	Cycle time(2), dss_pclk	TBD		ns
DL5	$t_{w(PCLK)}$	Pulse duration, dss_pclk low or high	TBD	TBD	ns
	c_{load}	Load capacitance		TBD	pF

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

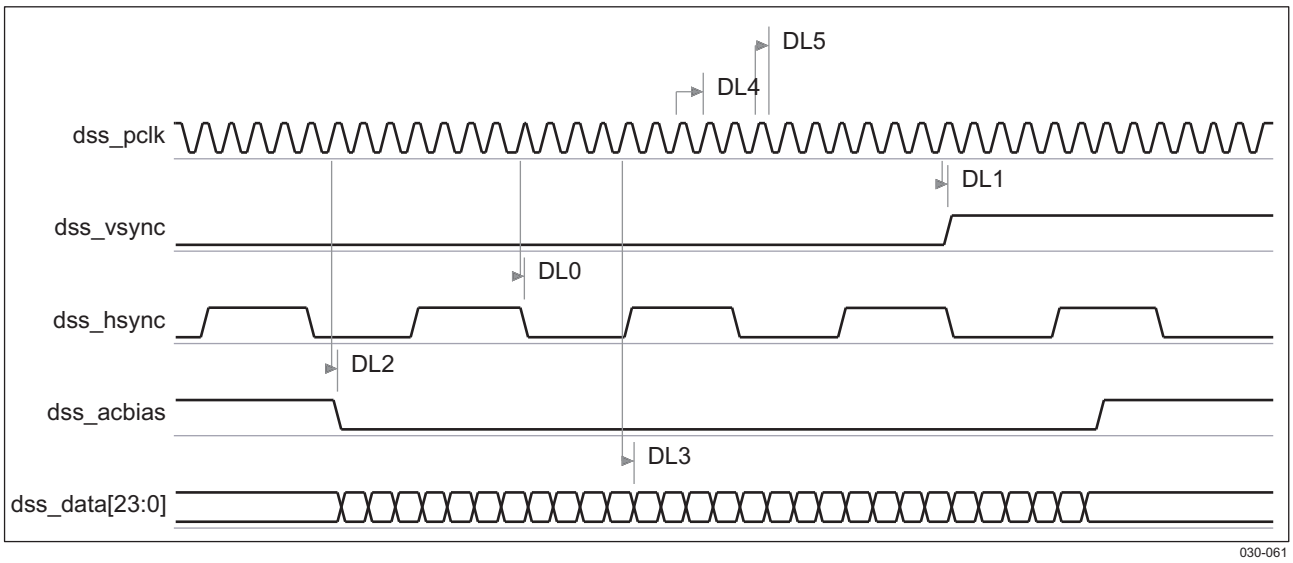

Figure 6-29. LCD Display in TFT ModeStep 1Step 2Step 3

(1) The pixel data bus depends on the use of 8-, 9-, 12-, 16-, 18-, or 24-bit per pixel data output pins.
(2) The pixel clock frequency is programmable.
(3) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss_pclk.

6.5.2.1.2 LCD Display in STN Mode

Table 6-29 assumes testing over the recommended operating conditions (see Figure 6-30).

Table 6-29. LCD Display Interface Switching Characteristics in STN Mode(1)(2)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
DL3	$t_{d(PCLKA-DATAV)}$	Delay time, dss_pclk active edge to dss_data bus valid	TBD	TBD	ns
DL4	$t_{c(PCLK)}$	Cycle time(3), dss_pclk	TBD		ns
DL5	$t_{w(PCLK)}$	Pulse duration, dss_pclk low or high	TBD	TBD	ns
	c_{load}	Load capacitance		TBD	pF

(1) The DSS in STN mode is used with 4 or 8 pins only; unused pixel data bits always remain low.
(2) The capacitive load is equivalent to 40 pF.
(3) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

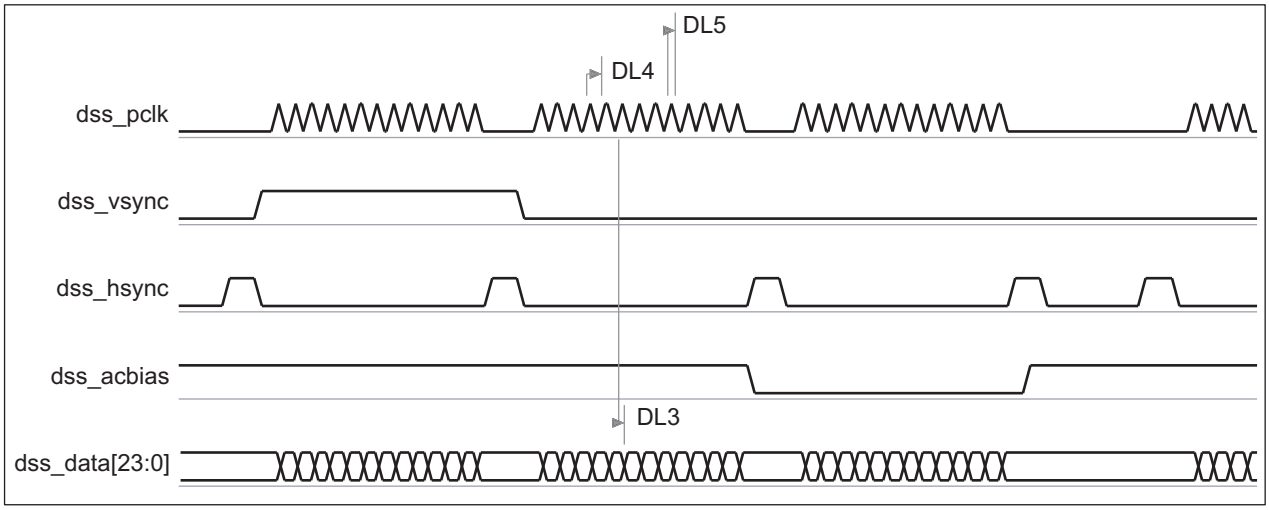

Figure 6-30. LCD Display in STN Mode(1)(2)(3)(4)

(1) The pixel data bus depends on the use 4-, 8-, 12-, 16-, 18-, or 24-bit per pixel data output pins.
(2) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss_pclk.
(3) dss_vsync width must be programmed to be as small as possible.
(4) The pixel clock frequency is programmable.

6.6 Serial Communications Interfaces

6.6.1 Multichannel Buffered Serial Port (McBSP) Timing

There are five McBSP modules called McBSP1 through McBSP5. McBSP provides a full-duplex, direct serial interface between the AM3517/05 device and other devices in a system such as other application devices or codecs. It can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, and TDM) due to its high level of versatility.

The McBSP1-5 modules may support two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half-cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time.

The interface clock (CLKX/CLKR) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

The AM3517/05 McBSP1-5 timing characteristics are described for both rising and falling activation edges. McBSP1 supports:

- 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
- 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back via software configuration, respectively, to the clkr and fsr internal signals for data receive.

McBSP2, 3, 4, and 5 support only the 4-pin mode.

The following sections describe the timing characteristics for applications in normal mode (that is, AM3517/05 McBSPx connected to one peripheral) and TDM applications in multipoint mode.

6.6.1.1 McBSP in Normal Mode

Table 6-30. McBSP Timing Conditions (Normal Mode)

TIMING CONDITION PARAMETER		1.8V, 3.3 V		UNIT
Input Conditions		**MIN**	**MAX**	
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance		TBD	pF

Table 6-31. McBSP Output Clock Pulse Duration

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	**MAX**	**MIN**	**MAX**	
	$t_{W(CLKH)}$	Typical pulse duration, mcbsp1_clkr / mcbspx_clkx high(1)	TBD		TBD		ns
	$t_{W(CLKL)}$	Typical pulse duration, mcbsp1_clkr / mcbspx_clkx low(1)	TBD		TBD		ns
	$t_{dc(CLK)}$	Duty cycle error, mcbsp1_clkr / mcbspx_clkx(1)	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

6.6.1.1.1 Receive Timing with Rising Edge as Activation Edge

Table 6-32 through Table 6-37 assume testing over the recommended operating conditions (see Figure 6-31 through Figure 6-32).

Table 6-32. McBSP1, 2, and 3 (Sets #1 and #2) Timing Requirements Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.8V		3.3V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKAE)}$	Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKAE-DRV)}$	Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr / mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr / mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-33. McBSP1, 2, and 3 (Sets #1 and #2) Switching Characteristics Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.8V		3.3V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKAE-FSV)}$	Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-34. McBSP4 (Set #3) Timing Requirements Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time mcbspx_fsx valid before mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold Time mcbspx_fsx valid after mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-36 and Table 6-37

Table 6-35. McBSP4 (Set #3) Switching Characteristics Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-36 and Table 6-37

Table 6-36. McBSP3 (Set #3), 4 (Set #1), and 5 Timing Requirements Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-34 and Table 6-35.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Table 6-37. McBSP3 (Set #3), 4 (Set #1), and 5 Switching Requirements Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

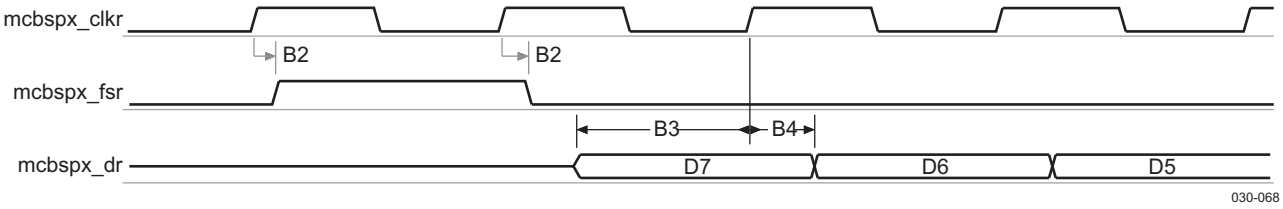

Figure 6-31. McBSP Rising Edge Receive Timing in Master Mode

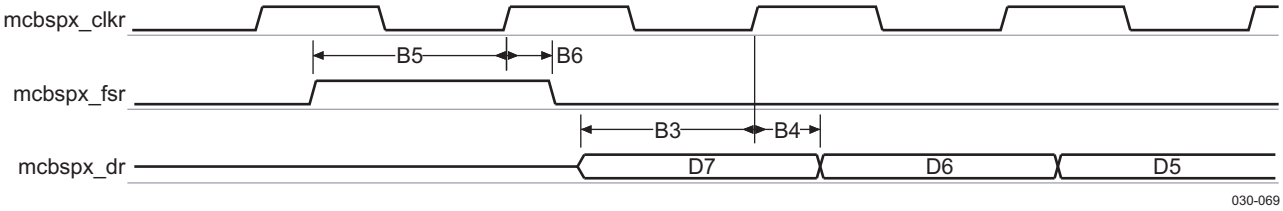

Figure 6-32. McBSP Rising Edge Receive Timing in Slave Mode

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-34 and Table 6-35.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

6.6.1.1.2 Transmit Timing with Rising Edge as Activation Edge

Table 6-38 through Table 6-43 assume testing over the recommended operating conditions (see Figure 6-33 and Figure 6-34).

Table 6-38. McBSP1, 2, and 3 (Sets #1 and #2) Timing Requirements Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.8V		3.3V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-38. McBSP1, 2, and 3 (Sets #1 and #2) Timing Requirements Rising Edge and Transmit Mode (continued)

NO.	PARAMETER		1.8V		3.3V		UNIT
			MIN	MAX	MIN	MAX	
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	TBD		TBD		ns

Table 6-39. McBSP1, 2, and 3 (Sets #1 and #2) Switching Characteristics Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.8V		3.3V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		TBD	TBD	TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	TBD	TBD	TBD	TBD	ns
			Slave	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-40. McBSP4 (Set #3) Timing Requirements Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.8V		3.3V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-42.

Table 6-41. McBSP4 (Set #3) Switching Characteristics Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.8V		3.3V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		TBD	TBD	TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	TBD	TBD	TBD	TBD	ns
			Slave	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-42.

Table 6-42. McBSP3 (Set #3), 4 (Set #1), and 5 Timing Requirements Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.8V		3.3V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-42.

Table 6-43. McBSP 3 (Set #3), 4 (Set #1), and 5 Switching Requirements Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.8V		3.3V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		TBD	TBD	TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	TBD	TBD	TBD	TBD	ns
			Slave	TBD	TBD	TBD	TBD	ns

Figure 6-33. McBSP Rising Edge Transmit Timing in Master Mode

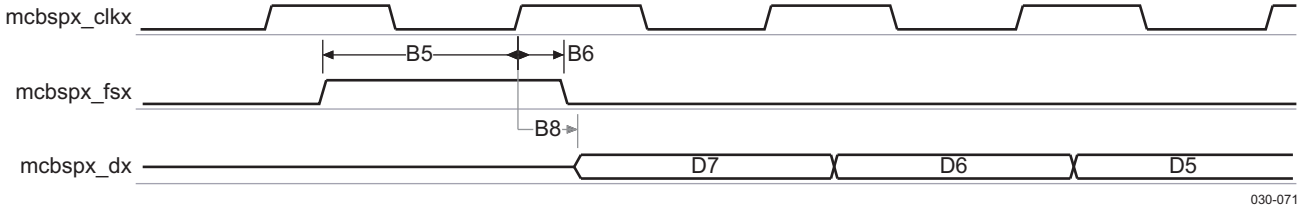

Figure 6-34. McBSP Rising Edge Transmit Timing in Slave Mode

(1) In mcbspx, x identifies the McBSP number: 3, 4 or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

6.6.1.1.3 Receive Timing with Falling Edge as Activation Edge

Table 6-44 through Table 6-49 assume testing over the recommended operating conditions (see Figure 6-35 and Figure 6-36).

Table 6-44. McBSP1, 2, and 3 (Sets #1 and #2) Timing Requirements Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.8V		3.3V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKAE)}$	Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKAE-DRV)}$	Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr /mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr /mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-45. McBSP1, 2, and 3 (Sets #1 and #2) Switching Characteristics Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKAE-FSV)}$	Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-46. McBSP4 (Set #3) Timing Requirements Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time mcbspx_fsx valid before mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time mcbspx_fsx valid after mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-48

Table 6-47. McBSP4 (Set #3) Switching Characteristics Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-48

Table 6-48. McBSP3 (Set #3), 4 (Set #1), and 5 Timing Requirements Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	TBD		TBD		ns
			Slave	TBD		TBD		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge		TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge		TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Table 6-49. McBSP3 (Set #3), 4 (Set #1), and 5 Switching Requirements Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

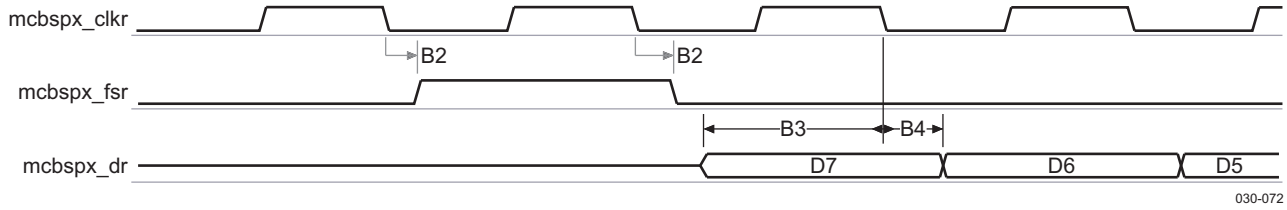

Figure 6-35. McBSP Falling Edge Receive Timing in Master Mode

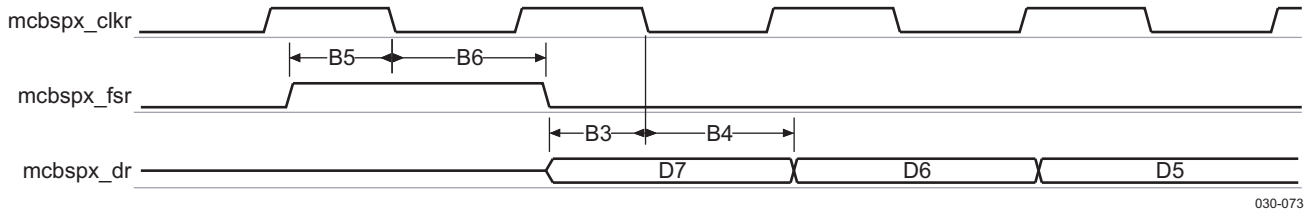

Figure 6-36. McBSP Falling Edge Receive Timing in Slave Mode

6.6.1.1.4 Transmit Timing with Falling Edge as Activation Edge

Table 6-50 through Table 6-55 assume testing over the recommended operating conditions (see Figure 6-37 and Figure 6-38).

Table 6-50. McBSP1, 2, and 3 (Sets #1 and #2) Timing Requirements Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge			TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge			TBD		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-51. McBSP1, 2, and 3 (Sets #1 and #2) Switching Characteristics Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid				TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master			TBD	TBD	ns
			Slave			TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-52. McBSP4 (Set #3) Timing Requirements Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	TBD		TBD		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	TBD		TBD		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-54.

Table 6-53. McBSP4 (Set #3) Switching Characteristics Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		TBD	TBD	TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	TBD	TBD	TBD	TBD	ns
			Slave	0.6	17.3	0.6	33.1	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-54.

Table 6-54. McBSP3 (Set #3), 4 (Set #1), and 5 Timing Requirements Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	5.8		12.2		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-54. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Table 6-55. McBSP3 (Set #3), 4 (Set #1), and 5 Switching Requirements Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		TBD	TBD	TBD	TBD	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	TBD	TBD	TBD	TBD	ns
			Slave	TBD	TBD	TBD	TBD	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-54. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

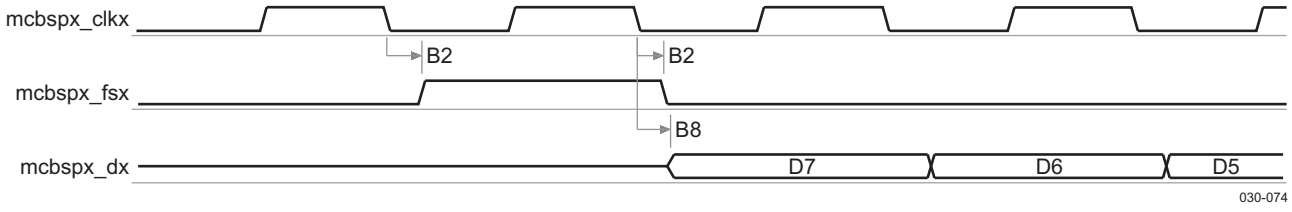

Figure 6-37. McBSP Falling Edge Transmit Timing in Master Mode

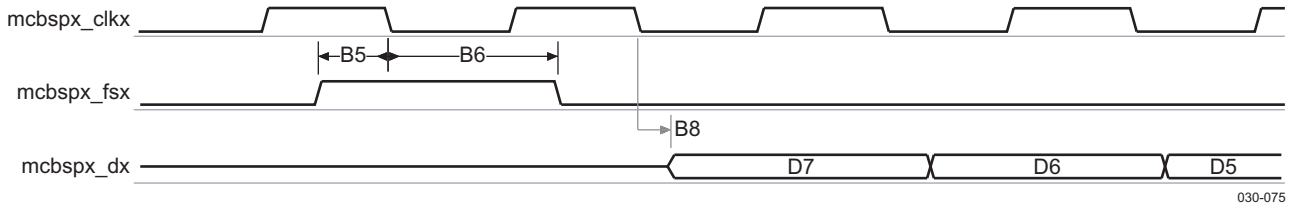

Figure 6-38. McBSP Falling Edge Transmit Timing in Slave Mode

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6.6.1.2 McBSP in TDMMultipoint Mode (McBSP3)

For TDM application in multipoint mode, AM3517/05 is considered as a slave. Table 6-57 and Table 6-58 assume testing over the operating conditions and electrical characteristic conditions described below.

Table 6-56. McBSP3 Timing ConditionsTDM in Multipoint Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rising time	TBD	TBD	ns
t_F	Input signal falling time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output Load Capacitance		TBD	pF

Table 6-57. McBSP3 Timing RequirementsTDM in Multipoint Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
	$t_{W(CLKH)}$	Cycle Time, mcbsp3_clkx	TBD		TBD		ns
	$t_{W(CLKH)}$	Typical Pulse duration, mcbsp3_clkx high	TBD		TBD		ns
	$t_{W(CLKL)}$	Typical Pulse duration, mcbsp3_clkx low	TBD		TBD		ns
	$t_{dc(CLK)}$	Duty cycle error, mcbsp3_clkx	TBD	TBD	TBD	TBD	ns
B3(2)	$t_{su(DRV-CLKAE)}$	Setup time, mcbsp3_dr valid before mcbsp3_clkx active edge	TBD		TBD		ns
B4(2)	$t_{h(CLKAE-DRV)}$	Hold time, mcbsp3_dr valid after mcbsp3_clkx active edge	TBD		TBD		ns
B5(2)	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp3_fsx valid before mcbsp3_clkx active edge	TBD		TBD		ns
B6(2)	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp3_fsx valid after mcbsp3_clkx active edge	TBD		TBD		ns

(1) For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).
(2) See Section 6.6.1.1, *McBSP in Normal Mode* for corresponding figures.

Table 6-58. McBSP3 Switching CharacteristicsTDM in Multipoint Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
B8(2)	$t_{d(CLKXAE-DXV)}$	Delay time, mcbsp3_clkx active edge to mcbsp3_dx valid	TBD	TBD	TBD	TBD	ns

(1) For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).
(2) See Section 6.6.1.1, *McBSP in Normal Mode* for corresponding figures.

6.6.2 *Multichannel Serial Port Interface (McSPI) Timing*

The multichannel SPI is a master/slave synchronous serial bus. The McSPI1 module supports up to four peripherals and the others (McSPI2, McSPI3, and McSPI4) support up to two peripherals. The following timings are applicable to the different configurations of McSPI in master/slave mode for any McSPI and any channel (n).

6.6.2.1 McSPI in Slave Mode

Table 6-59 and Table 6-60 assume testing over the recommended operating conditions (see Figure 6-39).

Table 6-59. McSPI Interface Timing Requirements – Slave Mode(1)(2)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
SS0	$t_{c(CLK)}$	Cycle time, mcspix_clk	TBD		TBD		ns
SS1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low	TBD		TBD		ns
SS2	$t_{su(SIMOV-CLKAE)}$	Setup time, mcspix_simo valid before mcspix_clk active edge	TBD		TBD		ns
SS3	$t_{h(SIMOV-CLKAE)}$	Hold time, mcspix_simo valid after mcspix_clk active edge	TBD		TBD		ns
SS4	$t_{su(CS0V-CLKFE)}$	Setup time, mcspix_cs0 valid before mcspix_clk first edge	TBD		TBD		ns
SS5	$t_{h(CS0I-CLKLE)}$	Hold time, mcspix_cs0 invalid after mcspix_clk last edge	TBD		TBD		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspix, x is equal to 1, 2, 3, or 4.

Table 6-60. McSPI Interface Switching Requirements(1)(2)(3)(4)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
SS6	$t_{d(CLKAE-SOMIV)}$	Delay time, mcspix_clk active edge to mcspix_somi shifted		TBD	TBD	TBD	TBD	ns
SS7	$t_{d(CS0AE-SOMIV)}$	Delay time, mcspix_cs0 active edge to mcspix_somi shifted	Modes 0 and 2		TBD		TBD	ns

(1) The capacitive load is equivalent to 20 pF.
(2) In mcspix, x is equal to 1, 2, 3, or 4.
(3) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable.
(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

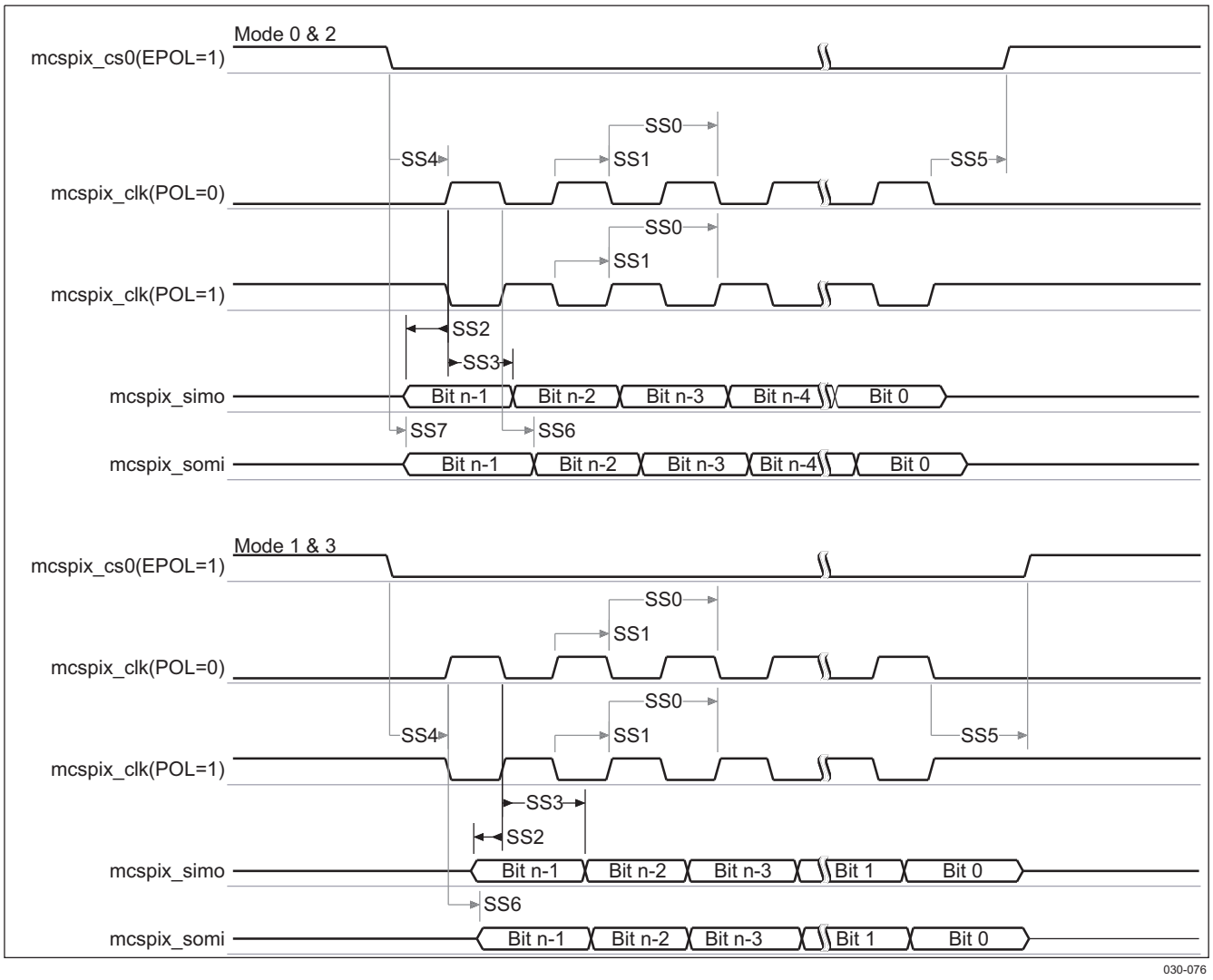

Figure 6-39. McSPI Interface Transmit and Receive in Slave Mode[(1)(2)]

(1) The active clock edge (rising or falling) on which mcspi_somi is driven and mcspi_simo data is latched is software configurable with the bit MSPI_CHCONFx[0] = PHA and the bit MSPI_CHCONFx[1] = POL.

(2) The polarity of mcspix_csi is software configurable with the bit MSPI_CHCONFx[6] = EPOL In mcspix, x is equal to 1, 2, 3, or 4.

6.6.2.2 McSPI in Master Mode

Table 6-61 and Table 6-62 assume testing over the recommended operating conditions (see Figure 6-40).

Table 6-61. McSPI1, 2, and 4 Interface Timing Requirements – Master Mode[(1)(2)]

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
SM2	$t_{su(SOMIV-CLKAE)}$	Setup time, mcspix_somi valid before mcspix_clk active edge	TBD		TBD		ns
SM3	$t_{h(SOMIV-CLKAE)}$	Hold time, mcspix_somi valid after mcspix_clk active edge	TBD		TBD		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspix, x is equal to 1, 2, 3, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 3. n is equal to 0 for x equal to 4.

Table 6-62. McSPI1, 2, and 4 Interface Switching Characteristics – Master Mode(1)(2)(3)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
SM0	$t_{c(CLK)}$	Cycle time, mcspix_clk		TBD		TBD		ns
SM1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low		TBD	TBD	TBD		ns
SM4	$t_{d(CLKAE-SIMOV)}$	Delay time, mcspix_clk active edge to mcspix_simo shifted		TBD	TBD	TBD	TBD	ns
SM5	$t_{d(CSnA-CLKFE)}$	Delay time, mcspix_csi active to mcspix_clk first edge	Modes 1 and 3	TBD		TBD	TBD	ns
			Modes 0 and 2	TBD		TBD	TBD	ns
SM6	$t_{d(CLKLE-CSnI)}$	Delay time, mcspix_clk last edge to mcspix_csi inactive	Modes 1 and 3	TBD		TBD		ns
			Modes 0 and 2	TBD				ns
SM7	$t_{d(CSnAE-SIMOV)}$	Delay time, mcspix_csi active edge to mcspix_simo shifted	Modes 0 and 2		TBD		TBD	ns

(1) Timings are given for a maximum load capacitance of 20 pF for spix_csn signals, 30 pF for spix_clk and spix_simo signals with x = 1 or 2, and 20 pF for spi4_clk and spi4_simo signals.
(2) In mcspix, x is equal to 1, 2, 3, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 3. n is equal to 0 for x equal to 4.
(3) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable.

Table 6-63 and Table 6-64 assume testing over the recommended operating conditions (see Figure 6-40).

Table 6-63. McSPI 3 Interface Timing Requirements – Master Mode(1)(2)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
SM2	$t_{su(SOMIV-CLKAE)}$	Setup time, mcspi3_somi valid before mcspi3_clk active edge	TBD		TBD		ns
SM3	$t_{h(SOMIV-CLKAE)}$	Hold time, mcspi3_somi valid after mcspi3_clk active edge	TB		TBD		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspi3_csn, n is equal to 0 or 1. The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable.

Table 6-64. McSPI3 Interface Switching Requirements – Master Mode(1)(2)(3)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
SM0	$t_{c(CLK)}$	Cycle time, mcspix_clk		TBD		TBD		ns
SM1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low		TBD	TBD	TBD	TBD	ns
SM4	$t_{d(CLKAE-SIMOV)}$	Delay time, mcspix_clk active edge to mcspix_simo shifted		TBD	TBD	TBD	TBD	ns
SM5	$t_{d(CSnA-CLKFE)}$	Delay time, mcspix_csi active to mcspix_clk first edge	Modes 1 and 3	TBD		TBD		ns
			Modes 0 and 2	TBD		TBD		ns

(1) The capacitive load is equivalent to 20 pF.
(2) In mcspi3_csn, n is equal to 0 or 1. The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable.
(3) This timing applies to all configurations regardless of McSPI3_CLK polarity and which clock edges are used to drive output data and capture input data.

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Table 6-64. McSPI3 Interface Switching Requirements – Master Mode (continued)

NO.	PARAMETER			1.8 V		3.3 V		UNIT
				MIN	MAX	MIN	MAX	
SM6	$t_{d(CLKLE-CSnI)}$	Delay time, mcspix_clk last edge to mcspix_csi inactive	Modes 1 and 3	TBD		TBD		ns
			Modes 0 and 2	TBD		TBD		ns
SM7	$t_{d(CSnAE-SIMOV)}$	Delay time, mcspix_csi active edge to mcspix_simo shifted	Modes 0 and 2		TBD		TBDD	ns

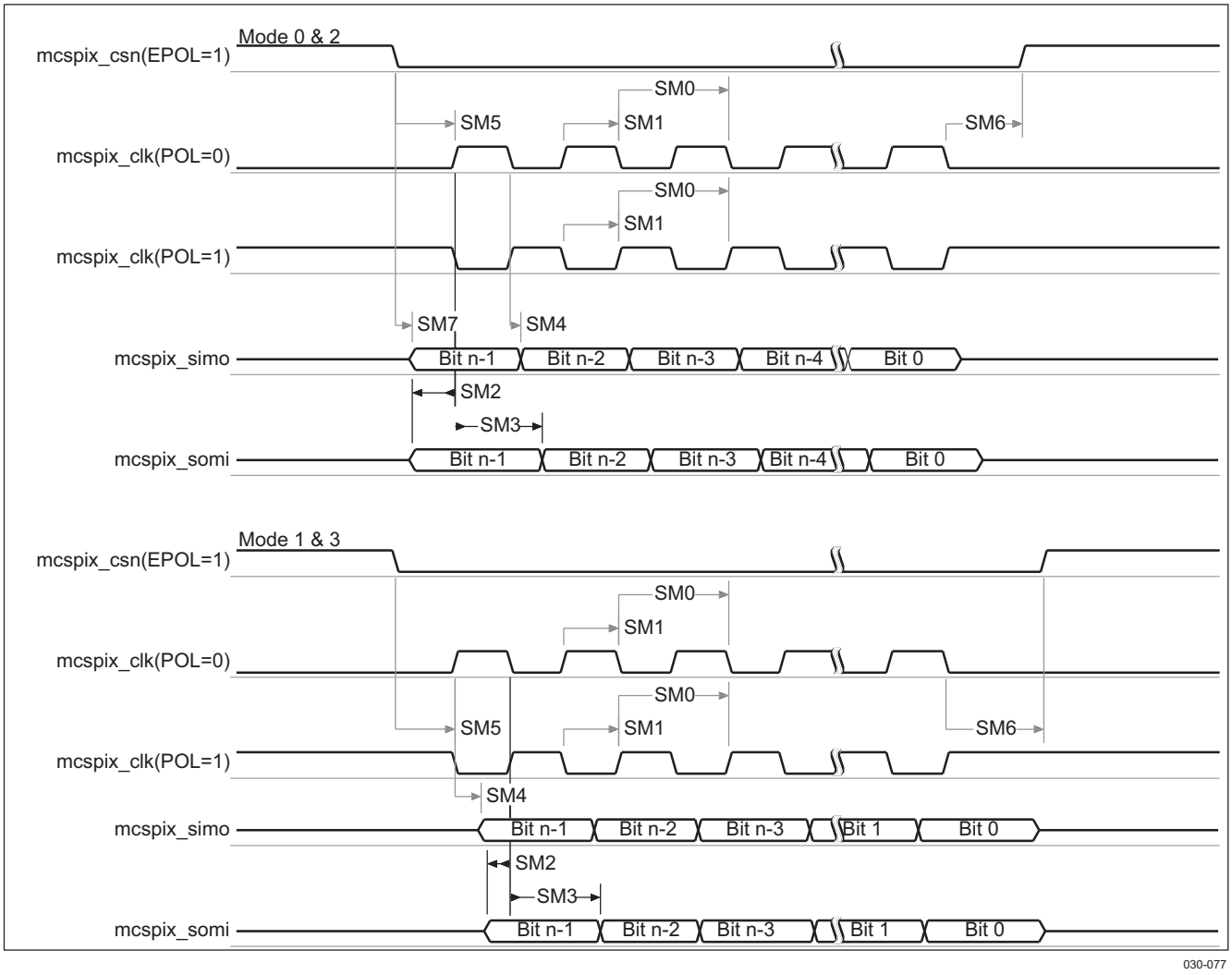

Figure 6-40. McSPI Interface Transmit and Receive in Master Mode[(1)(2)(3)]

(1) The active clock edge (rising or falling) on which mcspix_simo is driven and mcspi_somi data is latched is software configurable with the bit MSPI_CHCONFx[0] = PHA and the bit MSPI_CHCONFx[1] = POL.

(2) The polarity of mcspix_csi is software configurable with the bit MSPI_CHCONFx[6] = EPOL.

(3) In mcspix, x is equal to 1. In mcspix_csn, n is equal to 0, 1, 2, or 3.

6.6.3 Multiport Full-Speed Universal Serial Bus (USB) Interface

The AM3517/05 processor provides three USB ports working in full- and low-speed data transactions (up to 12Mbit/s).

Connected to either a serial link controller (TLL modes) or a serial PHY (PHY interface modes) it supports:

- 6-pin (Tx: Dat/Se0 or Tx: Dp/Dm) unidirectional mode
- 4-pin bidirectional mode
- 3-pin bidirectional mode

6.6.3.1 Multiport Full-Speed Universal Serial Bus (USB) – Unidirectional Standard 6-pin Mode

Table 6-66 and Table 6-67 assume testing over the recommended operating conditions (see Figure 6-41).

Table 6-65. Low-/Full-Speed USB Timing Conditions Unidirectional Standard 6-pin Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-66. Low-/Full-Speed USB Timing Requirements Unidirectional Standard 6-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU1	$t_{d(Vp,Vm)}$	Time duration, mmx_rxdp and mmx_rxdm low together during transition		14.0	ns
FSU2	$t_{d(Vp,Vm)}$	Time duration, mmx_rxdp and mmx_rxdm high together during transition		8.0	ns
FSU3	$t_{d(RCVU0)}$	Time duration, mmx_rrxcv undefine during a single end 0 (mmx_rxdp and mmx_rxdm low together)		14.0	ns
FSU4	$t_{d(RCVU1)}$	Time duration, mmx_rxrcv undefine during a single end 1 (mmx_rxdp and mmx_rxdm high together)		8.0	ns

Table 6-67. Low-/Full-Speed USB Switching Characteristics Unidirectional Standard 6-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU5	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	ns
FSU6	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	ns
FSU7	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5	ns
FSU8	$t_{d(DATI-TXENH)}$	Delay time, mmx_txdat invalid to mmx_txen_n high	81.8		ns
FSU9	$t_{d(SE0I-TXENH)}$	Delay time, mmx_txse0 invalid to mmx_txen_n high	81.8		ns
	$t_{R(do)}$	Rise time, mmx_txen_n		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txen_n		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txdat		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txdat		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txse0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txse0		4.0	ns

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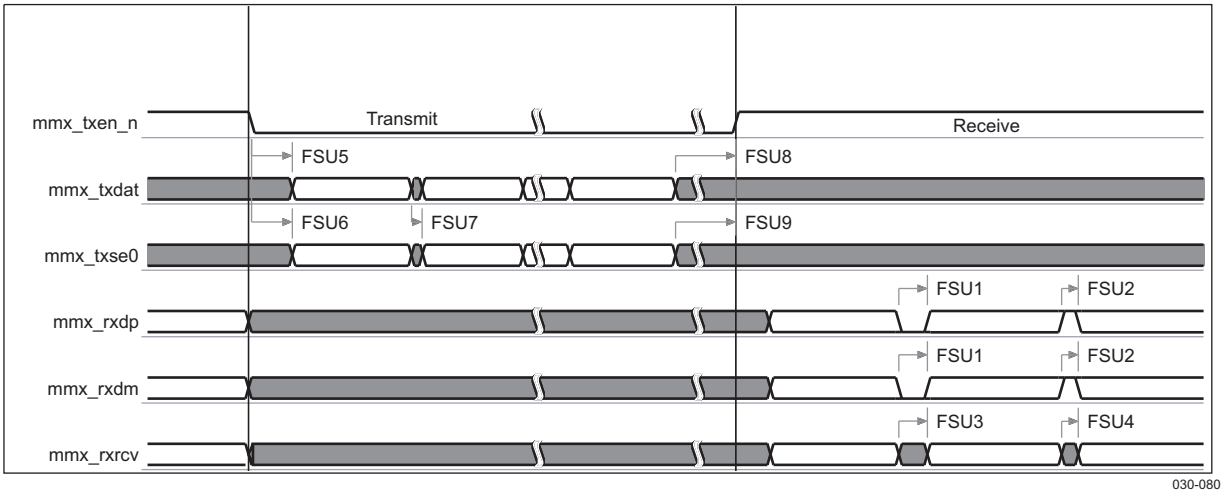


In mmx, x is equal to 0, 1, or 2.

Figure 6-41. Low-/Full-Speed USB Unidirectional Standard 6-pin Mode

6.6.3.2 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 4-pin Mode

Table 6-69 and Table 6-70 assume testing over the recommended operating conditions (see Figure 6-42).

Table 6-68. Low-/Full-Speed USB Timing Conditions Bidirectional Standard 4-pin Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-69. Low-/Full-Speed USB Timing Requirements Bidirectional Standard 4-pin Mode

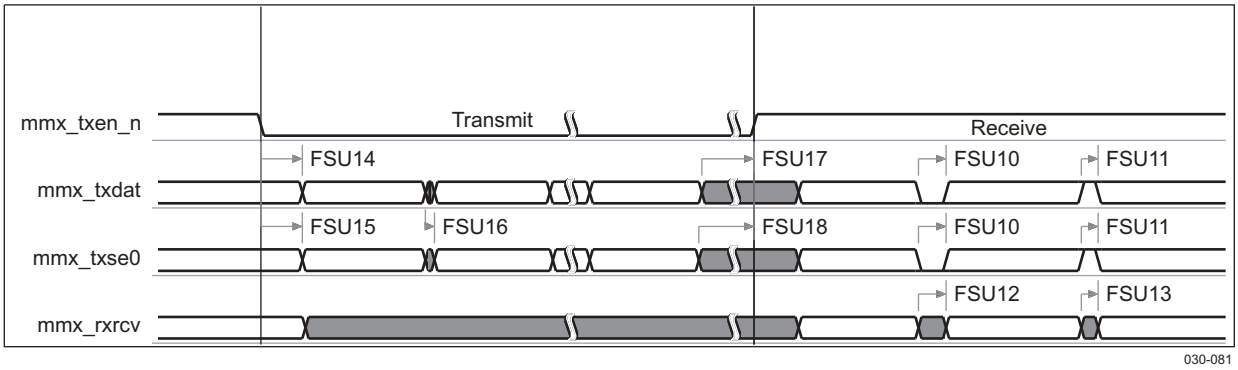
NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU10	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14.0	ns
FSU11	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 high together during transition		8.0	ns
FSU12	$t_{d(RCVU0)}$	Time duration, mmx_rrxcv undefine during a single end 0 (mmx_txdat and mmx_txse0 low together)		14.0	ns
FSU13	$t_{d(RCVU1)}$	Time duration, mmx_rxrcv undefine during a single end 1 (mmx_txdat and mmx_txse0 high together)		8.0	ns

Table 6-70. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 4-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU14	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	ns
FSU15	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	ns
FSU16	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5	ns
FSU17	$t_{d(DATV-TXENH)}$	Delay time, mmx_txdat invalid before mmx_txen_n high	81.8		ns
FSU18	$t_{d(SE0V-TXENH)}$	Delay time, mmx_txse0 invalid before mmx_txen_n high	81.8		ns
	$t_{R(txen)}$	Rise time, mmx_txen_n		4.0	ns

Table 6-70. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 4-pin Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
	$t_{F(txen)}$	Fall time, mmx_txen_n		4.0	ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4.0	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4.0	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4.0	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4.0	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-42. Low-/Full-Speed USB Bidirectional Standard 4-pin Mode

6.6.3.3 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 3-pin Mode

Table 6-72 and Table 6-73 assume testing over the recommended operating conditions below (see Figure 6-43).

Table 6-71. Low-/Full-Speed USB Timing Conditions Bidirectional Standard 3-pin Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-72. Low-/Full-Speed USB Timing Requirements Bidirectional Standard 3-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU19	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14.0	ns
FSU20	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8.0	ns

Table 6-73. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 3-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU21	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	ns
FSU22	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	ns

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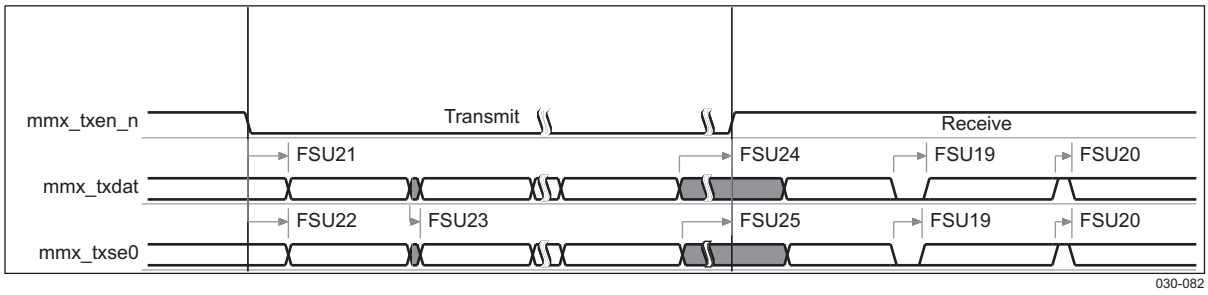
Table 6-73. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 3-pin Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSU23	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5	ns
FSU24	$t_{d(DATI-TXENH)}$	Delay time, mmx_txdat invalid to mmx_txen_n high	81.8		ns
FSU25	$t_{d(SE0I-TXENH)}$	Delay time, mmx_txse0 invalid to mmx_txen_n high	81.8		ns
	$t_{R(do)}$	Rise time, mmx_txen_n		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txen_n		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txdat		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txdat		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txse0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txse0		4.0	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-43. Low-/Full-Speed USB Bidirectional Standard 3-pin Mode

6.6.3.4 Multiport Full-Speed Universal Serial Bus (USB) – Unidirectional TLL 6-pin Mode

Table 6-75 and Table 6-76 assume testing over the recommended operating conditions (see Figure 6-44).

Table 6-74. Low-/Full-Speed USB Timing Conditions Unidirectional TLL 6-pin Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15	pF

Table 6-75. Low-/Full-Speed USB Timing Requirements Unidirectional TLL 6-pin Mode

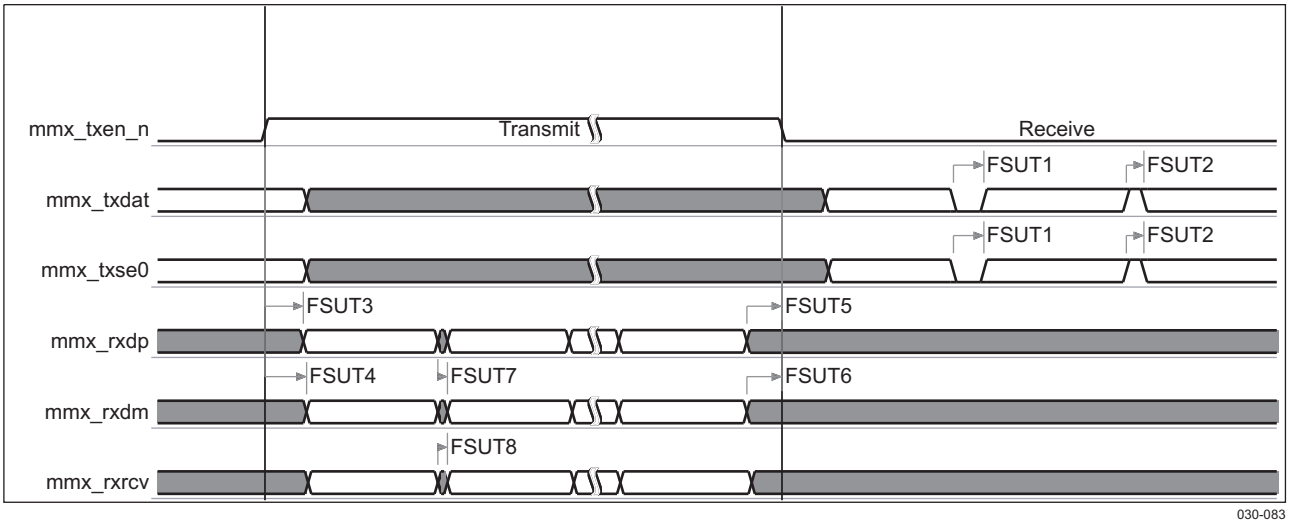
NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT1	$t_{d(SE0,DAT)}$	Time duration, mmx_txse0 and mmx_txdat low together during transition		14	ns
FSUT2	$t_{d(SE0,DAT)}$	Time duration, mmx_txse0 and mmx_txdat high together during transition		8	ns

Table 6-76. Low-/Full-Speed USB Switching Characteristics Unidirectional TLL 6-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT3	$t_{d(TXENH-DPV)}$	Delay time, mmx_txen_n high to mmx_rxdp valid	81.8	84.8	ns

Table 6-76. Low-/Full-Speed USB Switching Characteristics Unidirectional TLL 6-pin Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT4	$t_{d(TXENH-DMV)}$	Delay time, mmx_txen_n high to mmx_rxdm valid	81.8	84.8	ns
FSUT5	$t_{d(DPI-TXENL)}$	Delay time, mmx_rxdp invalid mmx_txen_n low	81.8		ns
FSUT6	$t_{d(DMI-TXENL)}$	Delay time, mmx_rxdm invalid mmx_txen_n low	81.8		ns
FSUT7	$t_{s(DP-DM)}$	Skew between mmx_rxdp and mmx_rxdm transition		1.5	ns
FSUT8	$t_{s(DP,DM-RCV)}$	Skew between mmx_rxdp, mmx_rxdm, and mmx_rxrcv transition		1.5	ns
	$t_{R(rxrcv)}$	Rise time, mmx_rxrcv		4	ns
	$t_{F(rxrcv)}$	Fall time, mmx_rxrcv		4	ns
	$t_{R(dp)}$	Rise time, mmx_rxdp		4	ns
	$t_{F(dp)}$	Fall time, mmx_rxdp		4	ns
	$t_{R(dm)}$	Rise time, mmx_rxdm		4	ns
	$t_{F(dm)}$	Fall time, mmx_rxdm		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-44. Low-/Full-Speed USB Unidirectional TLL 6-pin Mode

6.6.3.5 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional TLL 4-pin Mode

Table 6-78 and Table 6-79 assume testing over the recommended operating conditions (see Figure 6-45).

Table 6-77. Low-/Full-Speed USB Timing Conditions Bidirectional TLL 4-pin Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15	pF

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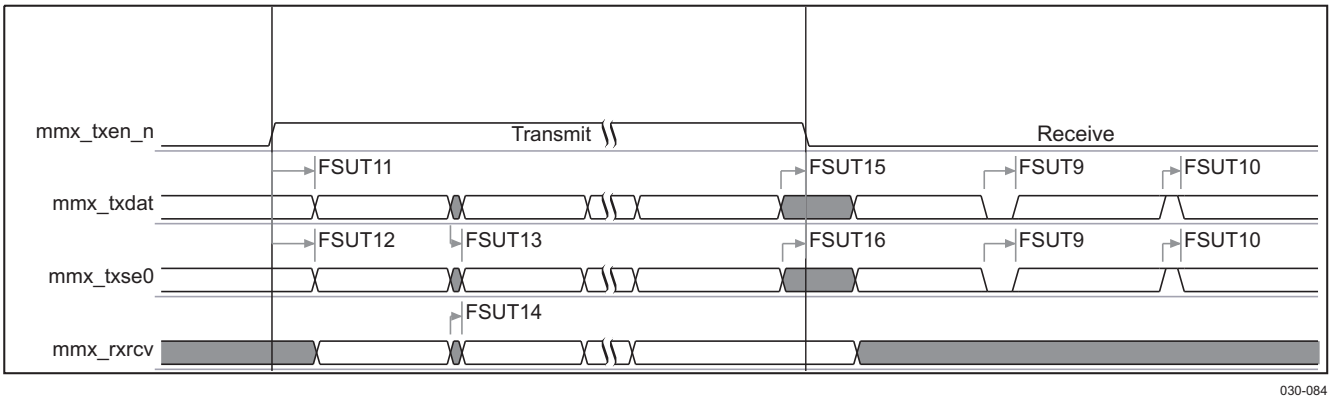
Table 6-78. Low-/Full-Speed USB Timing Requirements Bidirectional TLL 4-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT9	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14	ns
FSUT10	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8	ns

Table 6-79. Low-/Full-Speed USB Switching Characteristics Bidirectional TLL 4-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT11	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n active to mmx_txdat valid	81.8	84.8	ns
FSUT12	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n active to mmx_txse0 valid	81.8	84.8	ns
FSUT13	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5	ns
FSUT14	$t_{s(DP,DM-RCV)}$	Skew between mmx_rxdp, mmx_rxdm, and mmx_rxrcv transition		1.5	ns
FSUT15	$t_{d(DATI-TXENL)}$	Delay time, mmx_txse0 invalid to mmx_txen_n Low	81.8		ns
FSUT16	$t_{d(SE0I-TXENL)}$	Delay time, mmx_txdat invalid to mmx_txen_n Low	81.8		ns
	$t_{R(rcv)}$	Rise time, mmx_rxrcv		4	ns
	$t_{F(rcv)}$	Fall time, mmx_rxrcv		4	ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-45. Low-/Full-Speed USB Bidirectional TLL 4-pin Mode

6.6.3.6 Multiport Full-Speed Universal Serial Bus (USB) Bidirectional TLL 3-pin Mode

Table 6-81 and Table 6-82 assume testing over the recommended operating conditions (see Figure 6-46).

Table 6-80. Low-/Full-Speed USB Timing Conditions Bidirectional TLL 3-pin Mode

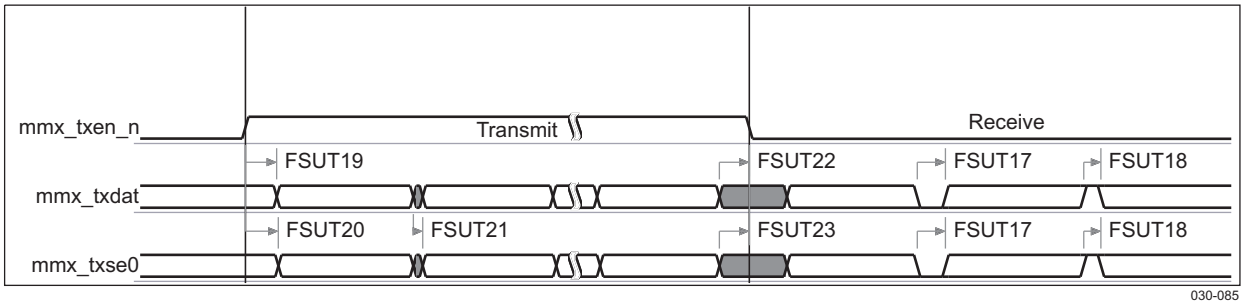
TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15	pF

Table 6-81. Low-/Full-Speed USB Timing Requirements Bidirectional TLL 3-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT17	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14	ns
FSUT18	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8	ns

Table 6-82. Low-/Full-Speed USB Switching Characteristics Bidirectional TLL 3-pin Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
FSUT19	$t_{d(TXENH-DATV)}$	Delay time, mmx_txen_n high to mmx_txdat valid	81.8	84.8	ns
FSUT20	$t_{d(TXENH-SE0V)}$	Delay time, mmx_txen_n high to mmx_txse0 valid	81.8	84.8	ns
FSUT21	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5	ns
FSUT22	$t_{d(DATI-TXENL)}$	Delay time, mmx_txdat invalid mmx_txen_n low	81.8		ns
FSUT23	$t_{d(SE0I-TXENL)}$	Delay time, mmx_txse0 invalid mmx_txen_n low	81.8		ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-46. Low-/Full-Speed USB Bidirectional TLL 3-pin Mode

6.6.4 Multiport High-Speed Universal Serial Bus (USB) Timing

In addition to the full-speed USB controller, a high-speed (HS) USB controller is instantiated inside AM3517/05. It allows high-speed transactions (up to 480 Mbit/s) on the USB ports 1 and 2.

- Port 1 and port 2:
  - 12-bit master mode (SDR)
  - 12-bit TLL master mode (SDR)
  - 8-bit TLL master mode (DDR)

Note: TLL is not available in 3.3V mode

6.6.4.1 High-Speed Universal Serial Bus (USB) on Ports 1 and 2 12-bit Master Mode

Table 6-84 and Table 6-85 assume testing over the recommended operating conditions (see Figure 6-47).

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Table 6-83. High-Speed USB Timing Conditions 12-bit Master Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-84. High-Speed USB Timing Requirements 12-bit Master Mode(1)

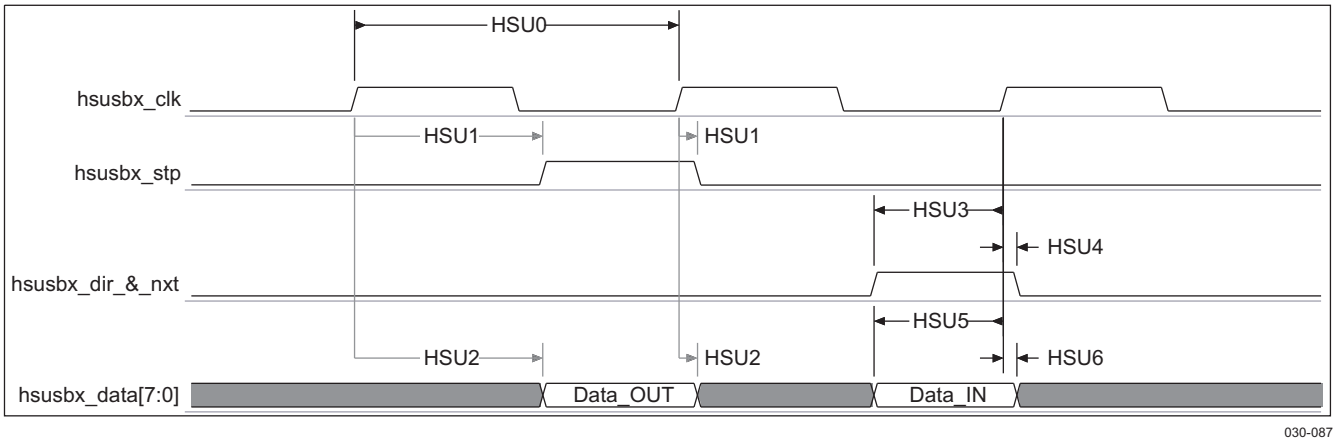
NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU3	$t_{s(DIRV-CLKH)}$	Setup time, hsusbx_dir valid before hsusbx_clk rising edge	9.3		ns
	$t_{s(NXTV-CLKH)}$	Setup time, hsusbx_nxt valid before hsusbx_clk rising edge	9.3		ns
HSU4	$t_{h(CLKH-DIRIV)}$	Hold time, hsusbx_dir valid after hsusbx_clk rising edge	0.2		ns
	$t_{h(CLKH-NXT/IV)}$	Hold time, hsusbx_nxt valid after hsusbx_clk rising edge	0.2		ns
HSU5	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_data[0:7] valid before hsusbx_clk rising edge	9.3		ns
HSU6	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_data[0:7] valid after hsusbx_clk rising edge	0.2		ns

(1) In hsusbx, x is equal to 1 or 2.

Table 6-85. High-Speed USB Switching Characteristics 12-bit Master Mode(1)

N O.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_clk clock frequency		60	MHz
	$t_{j(CLK)}$	Jitter standard deviation(2), hsusbx_clk		200	ps
HSU1	$t_{d(clkL-STPV)}$	Delay time, hsusbx_clk high to output hsusbx_stp valid		13	ns
	$t_{d(clkL-STPIV)}$	Delay time, hsusbx_clk high to output hsusbx_stp invalid	2		ns
HSU2	$t_{d(clkL-DV)}$	Delay time, hsusbx_clk high to output hsusbx_data[0:7] valid		13	ns
	$t_{d(clkL-DIV)}$	Delay time, hsusbx_clk high to output hsusbx_data[0:7] invalid	2		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns

(1) In hsusbx, x is equal to 1 or 2.
(2) The jitter probability density can be approximated by a Gaussian function.



In hsusbx, x is equal to 1 or 2.

Figure 6-47. High-Speed USB 12-bit Master Mode

6.6.4.2 High-Speed Universal Serial Bus (USB) on Ports 1 and 2 12-bit TLL Master Mode

Table 6-87 and Table 6-88 assume testing over the recommended operating conditions (see Figure 6-48).

Table 6-86. High-Speed USB Timing Conditions 12-bit TLL Master Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-87. High-Speed USB Timing Requirements 12-bit TLL Master Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU2	$t_{s(STPV-CLKH)}$	Setup time, hsusbx_tll_stp valid before hsusbx_tll_clk rising edge	6		ns
HSU3	$t_{s(CLKH-STPIV)}$	Hold time, hsusbx_tll_stp valid after hsusbx_tll_clk rising edge	0		ns
HSU4	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_tll_data[7:0] valid before hsusbx_tll_clk rising edge	6		ns
HSU5	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_tll_data[7:0] valid after hsusbx_tll_clk rising edge	0		ns

(1) In hsusbx, x is equal to 1, 2, or 3.

Table 6-88. High-Speed USB Switching Characteristics 12-bit TLL Master Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_tll_clk clock frequency		60	MHz
	$t_{j(CLK)}$	Jitter standard deviation(2), hsusbx_tll_clk		200	ps
HSU6	$t_{d(CLKL-DIRV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir valid		9	ns
	$t_{d(CLKL-DIRIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir invalid	0		ns
	$t_{d(CLKL-NXTV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt valid		9	ns
	$t_{d(CLKL-NXTIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt invalid	0		ns
HSU7	$t_{d(CLKL-DV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[7:0] valid		9	ns
	$t_{d(CLKL-DIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[7:0] invalid	0		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns

(1) In hsusbx, x is equal to 1, 2, or 3.
(2) The jitter probability density can be approximated by a Gaussian function.

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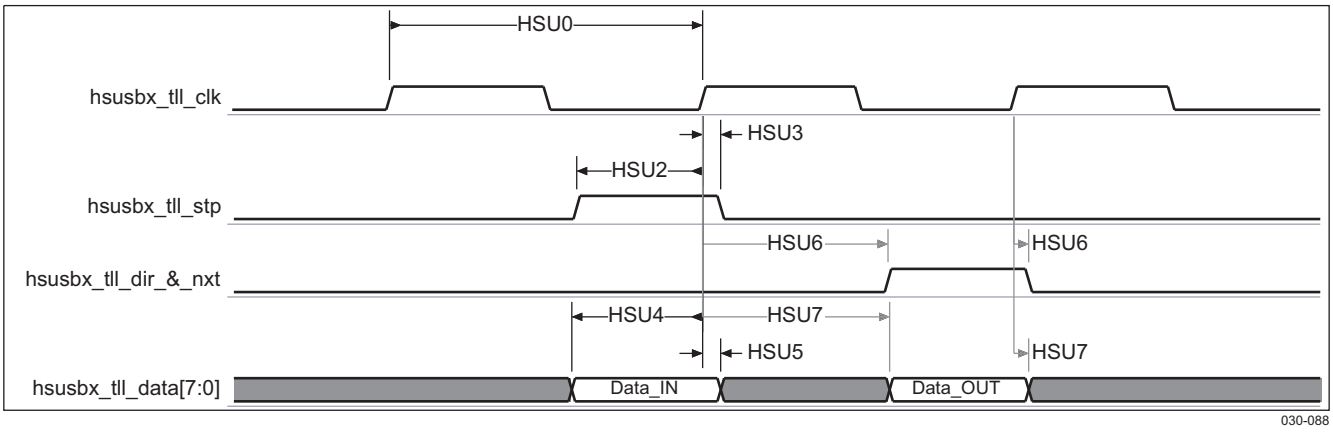


In hsusbx, x is equal to 1, 2, or 3.

Figure 6-48. High-Speed USB 12-bit TLL Master Mode

6.6.4.3 High-Speed Universal Serial Bus (USB) on Ports 1 and 2 8-bit TLL Master Mode

Table 6-90 and Table 6-91 assume testing over the recommended operating conditions (see Figure 6-49).

Table 6-89. High-Speed USB Timing Conditions 8-bit TLL Master Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-90. High-Speed USB Timing Requirements 8-bit TLL Master Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU2	$t_{s(STPV-CLKH)}$	Setup time, hsusbx_tll_stp valid before hsusbx_tll_clk rising edge	6		ns
HSU3	$t_{s(CLKH-STPIV)}$	Hold time, hsusbx_tll_stp valid after hsusbx_tll_clk rising edge	0		ns
HSU4	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_tll_data[3:0] valid before hsusbx_tll_clk rising edge	3		ns
HSU5	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_tll_data[3:0] valid after hsusbx_tll_clk rising edge	-0.1		ns

(1) In hsusbx, x is equal to 1, 2, or 3.

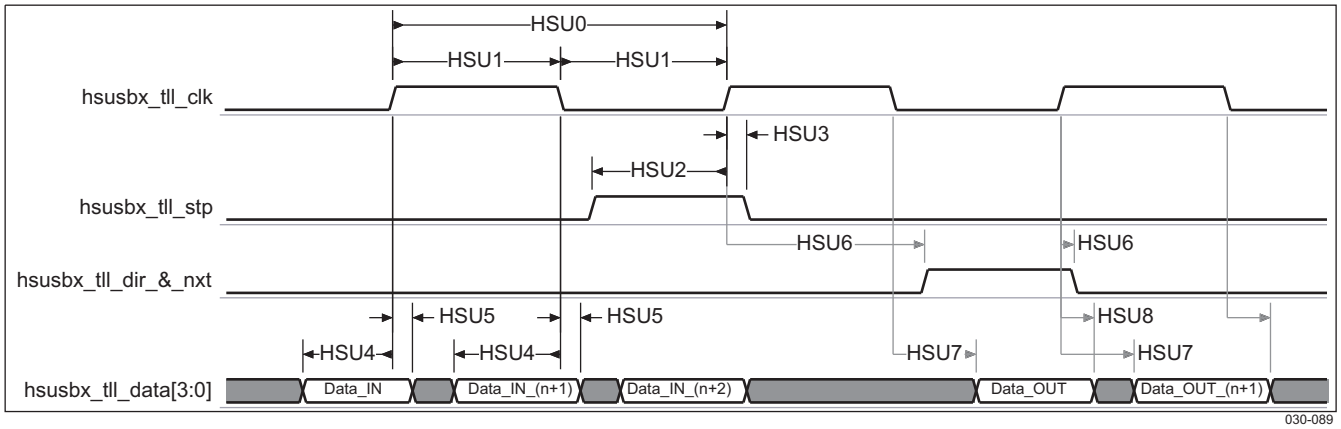
Table 6-91. High-Speed USB Switching Characteristics 8-bit TLL Master Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_tll_clk clock frequency		60	MHz
	$t_{j(CLK)}$	Jitter standard deviation(2), hsusbx_tll_clk		200	ps
HSU1	$t_{j(CLK)}$	Duty cycle, hsusbx_tll_clk pulse duration (low and high)	47.6%	52.4%	
HSU6	$t_{d(CLKL-DIRV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir valid		9	ns
	$t_{d(CLKL-DIRIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir invalid	0		ns
	$t_{d(CLKL-NXTV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt valid		9	ns
	$t_{d(CLKL-NXTIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt invalid	0		ns
HSU7	$t_{d(CLKL-DV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[3:0] valid		4	ns

(1) In hsusbx, x is equal to 1, 2, or 3.
(2) The jitter probability density can be approximated by a Gaussian function.

Table 6-91. High-Speed USB Switching Characteristics 8-bit TLL Master Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSU8	$t_{d(CLKL-DIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[3:0] invalid	0		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns



In hsusbx, x is equal to 1, 2, or 3.

Figure 6-49. High-Speed USB 8-bit TLL Master Mode

6.6.5 USB0 OTG (USB2.0 OTG)

The AM3517/05 USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 16 Transmit (TX) and 16 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 32K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

6.6.5.1 USB2.0 Electrical Data/Timing

Table 6-92. USB2.0 (OTG) Switching Characteristics (1)

NO.	PARAMETER		1.8V,3.3V						UNIT
			HIGH SPEED		FULL SPEED		LOW SPEED		
			MIN	MAX	MIN	MAX	MIN	MAX	
USB 1	V_{CRS}	Output signal cross-over voltage	TBD	TBD	TBD	TBD	TBD	TBD	V
USB 2	Z_{DRV}	Driver Output Impedance	TBD	TBD	TBD	TBD			Ω
USB 3	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals	TBD	TBD	TBD	TBD	TBD	TBD	ns

(1) In hsusbx, x is equal to 1, 2, or 3.

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Table 6-92. USB2.0 (OTG) Switching Characteristics (continued)

NO.	PARAMETER		1.8V,3.3V						UNIT
			HIGH SPEED		FULL SPEED		LOW SPEED		
			MIN	MAX	MIN	MAX	MIN	MAX	
USB 4	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals	TBD	TBD	TBD	TBD	TBD	TBD	ns
USB 5	t_{RFM}	Rise/Fall time, matching			TBD	TBD	TBD	TBD	%
USB 6	$t_{w(EOPT)}$	Pulse duration, EOP transmitter			TBD	TBD	TBD	TBD	ns
USB 7	$t_{w(EOPR)}$	Pulse duration, EOP receiver				TBD	TBD		ns
USB 8	$t_{(cjr)}$	Consecutive jitter		TBD		TBD		TBD	ns
USB 9	$t_{(pjkjr)}$	Paired JK jitter		TBD		TBD		TBD	ns
USB 10	$t_{(jpkjr)}$	Paired KJ jitter		TBD		TBD		TBD	ns
USB 11	$f_{(op)}$	Operating frequency		TBD	TBD	TBD	TBD	TBD	Mb/s

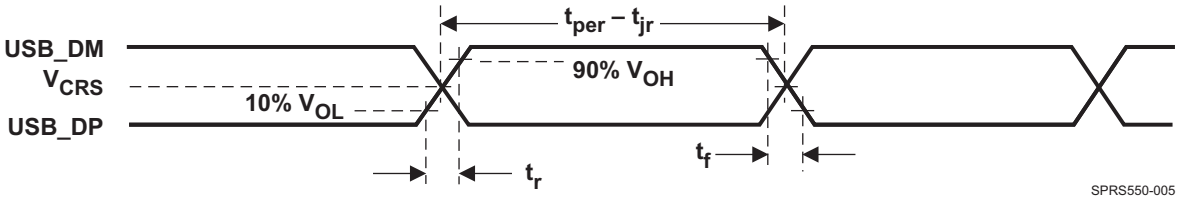

Figure 6-50. USB 2.0 Integrated Transceiver Interface Timing

6.6.6 High-End Controller Area Network Controller (HECC) Timing

The AM3517/05 device has a High-End Controller Area Network Controller (HECC). The HECC uses established protocol to communicate serially with other controllers in harsh environments. The HECC is fully compliant with the Controller Area Network (CAN) protocol, version 2.0B.

Key features of the HECC include the following:

- CAN, version 2.0B compliant
- 32 RX/TX message objects
- 32 receive identifier masks
- Programmable wake-up on bus activity
- Programmable interrupt scheme
- Automatic reply to a remote request
- Automatic re-transmission in case of error or loss of arbitration
- Protection against reception of a new message
- 32-bit time stamp
- Local network time counter
- Programmable priority register for each message
- Programmable transmission and reception time-out
- HECC/SCC mode of operation
- Standard-Extended Identifier
- Self-test mode

6.6.6.1 HECC Timing Requirements

Table 6-93. Timing Requirements for HECC Receive (see Figure 6-51)

NO.			1.8 V, 3.3 V		UNIT
			MIN	MAX	
1	$f_{(baud)}$	Maximum programmable baud rate		1	Mbps
2	$t_{w(HECC\_RX)}$	Pulse duration, receive data bit	-1	3	ns

6.6.6.2 HECC Switching Characteristics

Table 6-94. Switching Characteristics Over Recommended Operating Conditions for HECC Transmit (see Figure 6-51)

NO.	PARAMETER		1.8 V, 3.3 V		UNIT
			MIN	MAX	
3	$f_{(baud)}$	Maximum programmable baud rate		1	Mbps
4	$t_{w(HECC\_TX)}$	Pulse duration, transmit data bit	-1	3	ns

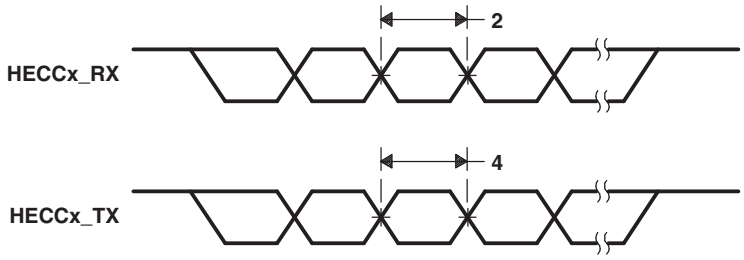

Figure 6-51. HECC Transmit/Receive Timing

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6.6.7 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between AM3517/05 and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the AM3517/05 device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the AM3517/05 device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

6.6.7.1 EMAC Electrical Data/ Timing

Table 6-95. RMII Input Timing Requirements

NO.	PARAMETER		1.8V, 3.3V			
			MIN	TYP	MAX	UNIT
1	tc(REFCLK)	Cycle Time, REF_CLK		TBD		ns
2	tw(REFCLKH)	Pulse Width, REF_CLK High	TBD		TBD	ns
3	tw(REFCLKL)	Pulse Width, REF_CLK Low	TBD		TBD	ns
6	tsu(RXD-REFCLK)	Input Setup Time, RXD Valid before REF_CLK High	TBD			ns
7	th(REFCLK-RXD)	Input Hold Time, RXD Valid after REF_CLK High	TBD			ns
8	tsu(CRSDV-REFCLK)	Input Setup Time, CRSDV Valid before REF_CLK High	TBD			ns
9	th(REFCLK-CRSDV)	Input Hold Time, CRSDV Valid after REF_CLK High	TBD			ns
10	tsu(RXER-REFCLK)	Input Setup Time, RXER Valid before REF_CLK High	TBD			ns
11	th(REFCLKR-RXER)	Input Hold Time, RXER Valid after REF_CLK High	TBD			ns

Table 6-96. RMII Output Timing Requirements

NO.	PARAMETER		1.8V, 3.3V			
			MIN	TYP	MAX	UNIT
4	td(REFCLK-TXD)	Output Delay Time, REF_CLK High to TXD Valid	TBD		TBD	ns
5	td(REFCLK-TXEN)	Output Delay Time, REF_CLK High to TXEN Valid	TBD		TBD	ns

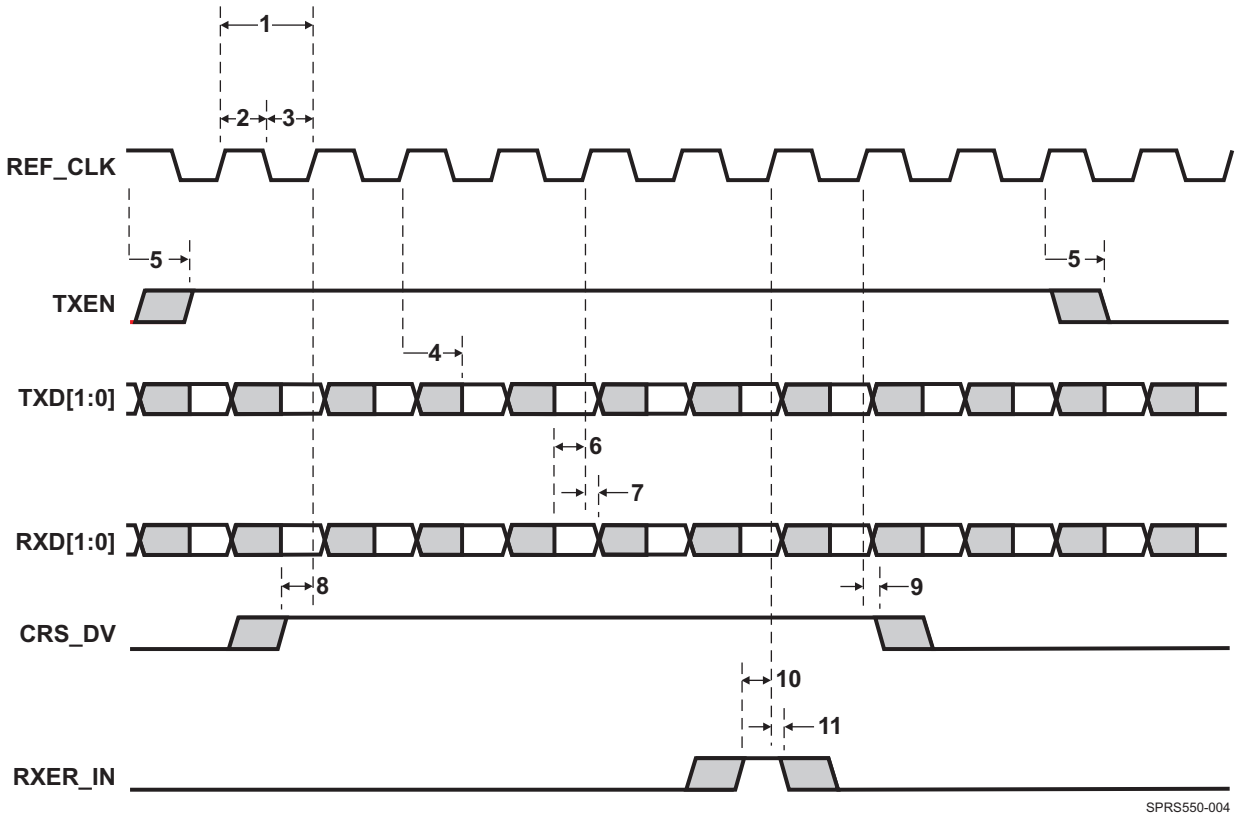

Figure 6-52. RMII Timing Diagram

6.6.8 Universal Asynchronous Receiver/Transmitter (UART)

The AM3517/05 has four UARTs (one with Infrared Data Association [IrDA] and Consumer Infrared [CIR] modes).

Table 6-97. Timing Requirements for UARTx Receive

NO.			1.8V, 3.3V		UNIT
			MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (RXDn)	.96U	1.05U	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit	.96U	1.05U	ns

Table 6-98. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
1	$f_{(baud)}$	UART0 Maximum programmable baud rate $f_{(baud\_15)}$		5	mbps
		UART0 Maximum programmable baud rate $f_{(baud\_30)}$		0.23	
		UART0 Maximum programmable baud rate $f_{(baud\_100)}$		0.115	
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit, 15/30/100 pF	U - 2	U + 2	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit, 15/30/100 pF	U - 2	U + 2	ns

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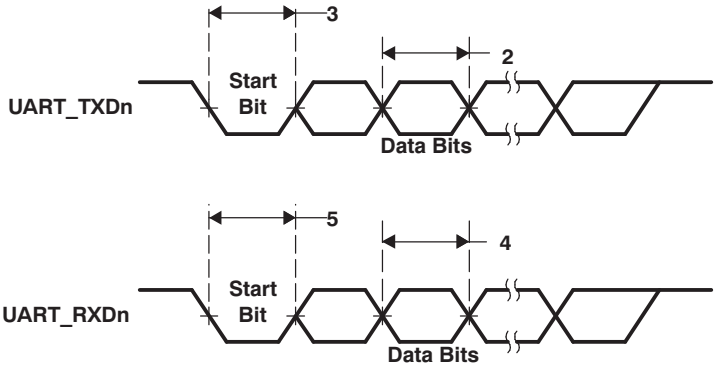

Figure 6-53. UART Transmit/Receive Timing

6.6.8.1 UART IrDA Interface

The IrDA module can operate in three different modes:

- Slow infrared (SIR) (≤115.2 Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)

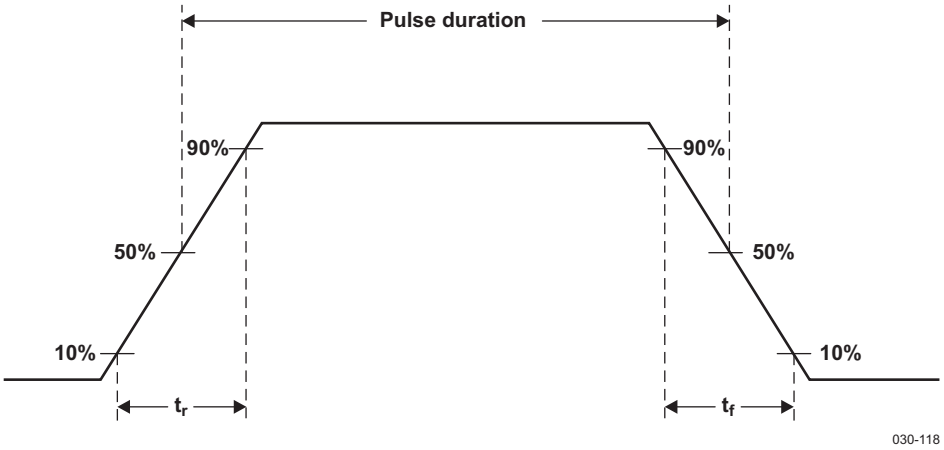

Figure 6-54. UART IrDA Pulse Parameters

6.6.8.1.1 IrDA—Receive Mode

Table 6-99. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
SIR				
2.4 Kbit/s	1.41	78.1	88.55	µs
9.6 Kbit/s	1.41	19.5	22.13	µs
19.2 Kbit/s	1.41	9.75	11.07	µs
38.4 Kbit/s	1.41	4.87	5.96	µs
57.6 Kbit/s	1.41	3.25	4.34	µs
115.2 Kbit/s	1.41	1.62	2.23	µs
MIR				
0.576 Mbit/s	297.2	416	518.8	ns
1.152 Mbit/s	149.6	208	258.4	ns

Table 6-99. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode (continued)

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
FIR				
4.0 Mbit/s (Single pulse)	67	125	164	ns
4.0 Mbit/s (Double pulse)	190	250	289	ns

Table 6-100. UART IrDA—Rise and Fall Time—Receive Mode

	PARAMETER	MAX	UNIT
t_R	Rising time, uart3_rx_irrx	200	ns
t_F	Falling time, uart3_rx_irrx	200	ns

6.6.8.1.2 IrDA—Transmit Mode

Table 6-101. UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
SIR				
2.4 Kbit/s	78.1	78.1	78.1	µs
9.6 Kbit/s	19.5	19.5	19.5	µs
19.2 Kbit/s	9.75	9.75	9.75	µs
38.4 Kbit/s	4.87	4.87	4.87	µs
57.6 Kbit/s	3.25	3.25	3.25	µs
115.2 Kbit/s	1.62	1.62	1.62	µs
MIR				
0.576 Mbit/s	414	416	419	ns
1.152 Mbit/s	206	208	211	ns
FIR				
4.0 Mbit/s (Single pulse)	123	125	128	ns
4.0 Mbit/s (Double pulse)	248	250	253	ns

6.6.9 HDQ / 1-Wire Interfaces

This module is intended to work with both the HDQ and the 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to 1 mechanism where, after any command, the line is pulled high.

6.6.9.1 HDQ Protocol

Table 6-102 and Table 6-103 assume testing over the recommended operating conditions (see Figure 6-55 through Figure 6-58).

Table 6-102. HDQ Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{CYCD}	Bit window	253		s
t_{HW1}	Reads 1		68	
t_{HW0}	Reads 0	180		
t_{RSPS}	Command to host respond time(1)			

(1) Defined by software.

Table 6-103. HDQ Switching Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_B	Break timing		193		s
t_{BR}	Break recovery		63		
t_{CYCH}	Bit window		253		
t_{DW1}	Sends1 (write)		1.3		
t_{DW0}	Sends0 (write)		101		

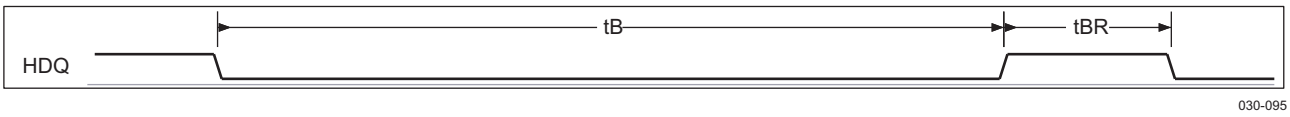

Figure 6-55. HDQ Break (Reset) Timing

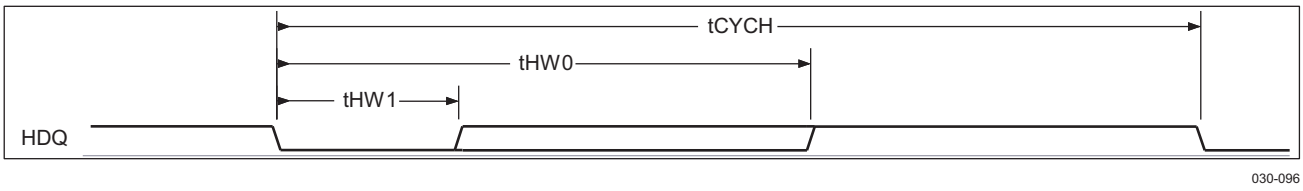

Figure 6-56. HDQ Read Bit Timing (Data)

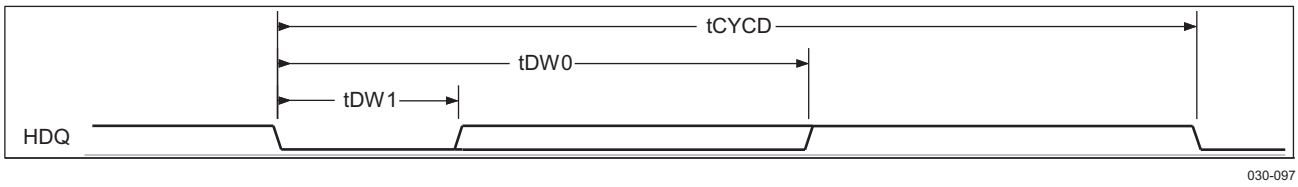

Figure 6-57. HDQ Write Bit Timing (Command/Address or Data)

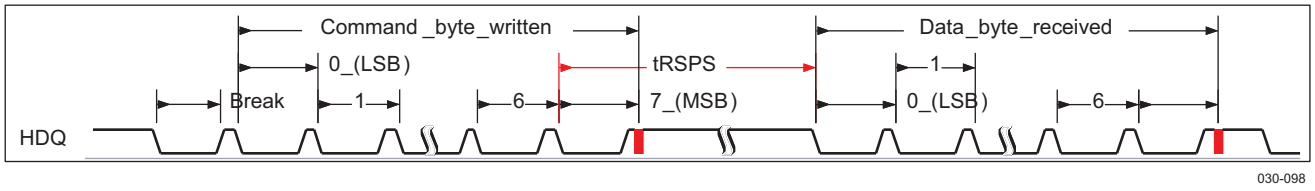

Figure 6-58. HDQ Communication Timing

6.6.9.2 1-Wire Protocol

Table 6-104 and Table 6-105 assume testing over the recommended operating conditions (see Figure 6-59 through Figure 6-61).

Table 6-104. 1-Wire Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{PDH}	Presence pulse delay high		68	s
t_{PDL}	Presence pulse delay low	68 t_{PDH}		
$t_{RDV} + t_{REL}$	Read bit-zero time		102	

Table 6-105. 1-Wire Switching Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{RSTL}	Reset time low		484		s
t_{RSTH}	Reset time high		484		
t_{SLOT}	Write bit cycle time		102		
t_{LOW1}	Write bit-one time		1.3		
t_{LOW0}	Write bit-zero time		101		
t_{REC}	Recovery time		134		
t_{LOWR}	Read bit strobe time		13		

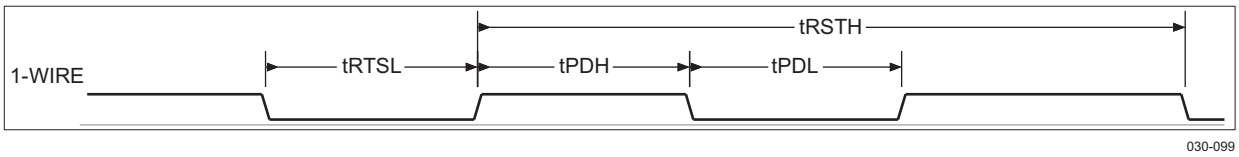

Figure 6-59. 1-Wire Break (Reset) Timing

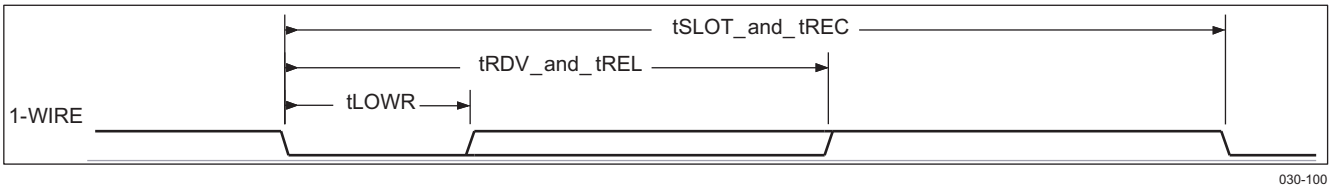

Figure 6-60. 1-Wire Read Bit Timing (Data)

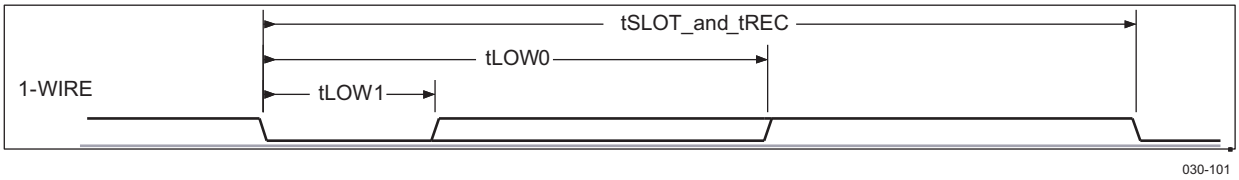

Figure 6-61. 1-Wire Write Bit Timing (Command/Address or Data)

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6.6.10 I²C Interface

The multimaster I²C peripheral provides an interface between two or more devices via an I²C serial bus. The I²C controller supports the multimaster mode which allows more than one device capable of controlling the bus to be connected to it. Each I²C device is recognized by a unique address and can operate as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I²C bus can also be considered as master or slave when performing data transfers. This data transfer is carried out via two serial bidirectional wires:

- An SDA data line
- An SCL clock line

The following sections illustrate the data transfer is in master or slave configuration with 7-bit addressing format. The I²C interface is compliant with Philips I²C specification version 2.1. It supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s) and high-speed mode (up to 3.4Mb/s) .

6.6.10.1 I²C Standard/Fast-Speed Mode

Table 6-106. I²C Standard/Fast-Speed Mode Timings

NO.	PARAMETER(1)		1.8V, 3.3-V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
	f_{SCL}	Clock Frequency, i2cX_scl		100		400	kHz
I1	$t_{w(SCLH)}$	Pulse Duration, i2cX_scl high	4		0.6		s
I2	$t_{w(SCLL)}$	Pulse Duration, i2cX_scl low	4.7		1.3		s
I3	$t_{su(SDAV-SCLH)}$	Setup time, i2cX_sda valid before i2cX_scl active level	250		100(2)		ns
I4	$t_{h(SCLHSDAV)}$	Hold time, i2cX_sda valid after i2cX_scl active level		3.45(3)		0.9(3)	s
I5	$t_{su(SDAL-SCLH)}$	Setup time, i2cX_scl high after i2cX_sda low (for a START(4) condition or a repeated START condition)	4.7		0.6		s
I6	$t_{h(SCLHSDAH)}$	Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)	4		0.6		s
I7	$t_{h(SCLHRSTART)}$	Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)	4		0.6		s
I8	$t_{w(SDAH)}$	Pulse duration, i2cX_sda high between STOP and START conditions	4.7		1.3		s
	$t_{R(SCL)}$	Rise time, i2cX_scl		1000		300	ns
	$t_{F(SCL)}$	Fall time, i2cX_scl		300		300	ns
	$t_{R(SDA)}$	Rise time, i2cX_sda		1000		300	ns
	$t_{F(SDA)}$	Fall time, i2cX_sda		300		300	ns
	CB	Capacitive load for each bus line		60		60	pF

(1) In i2cX, X is equal to 1, 2, or 3.
(2) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{su(SDAV-SCLH)}$ 250 ns must then be met. This is automatically the case if the device does not stretch the low period of the i2cx_scl. If such a device does stretch the low period of the i2cx_scl, it must output the next data bit to the i2cx_sda line $t_{r(SDA)}$ max + $t_{su(SDAV-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C-bus specification) before the i2cx_scl line is released.
(3) The maximum $t_{h(SCLH-SDA)}$ has only to be met if the device does not stretch the low period of the i2cx_scl signal.
(4) After this time, the first clock is generated.

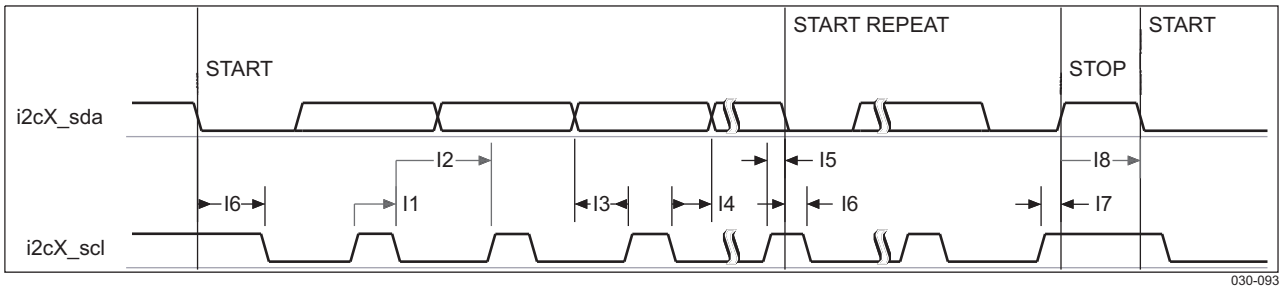

Figure 6-62. I²C Standard/Fast Mode

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6.6.10.2 I²C High-Speed Mode

Table 6-107. I²C HighSpeed Mode Timings(1)(2)

NO.	PARAMETER		1.8V, 3.3V				UNIT
			CB = 60 pF MAX		CB = 400 pF MAX		
			MIN	MAX	MIN	MAX	
	f_{SCL}	Clock frequency, i2cX_scl		3.4		1.7	MHz
I1	$t_{w(SCLH)}$	Pulse duration, i2cX_scl high	60(3)		120(3)		s
I2	$t_{w(SCLL)}$	Pulse duration, i2cX_scl low	160(3)		320(3)		s
I3	$t_{su(SDAV-SCLH)}$	Setup time, i2cX_sda valid before i2cX_scl active level	10		10		ns
I4	$t_{h(SCLHSDAV)}$	Hold time, i2cX_sda valid after i2cX_scl active level		70	0(2)	150	s
I5	$t_{su(SDAL-SCLH)}$	Setup time, i2cX_scl high after i2cX_sda low (for a START(4) condition or a repeated START condition)	160		160		s
I6	$t_{h(SCLHSDAH)}$	Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)	160		160		s
I7	$t_{h(SCLHRSTART)}$	Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)	160		160		ns
	$t_{R(SCL)}$	Rise time, i2cX_scl	10	40		80	ns
	$t_{R(SCL)}$	Rise time, i2cX_scl after a repeated START condition and after a bit acknowledge	10	80		160	ns
	$t_{F(SCL)}$	Fall time, i2cX_scl	10	40		80	ns
	$t_{R(SDA)}$	Rise time, i2cX_sda	10	80		160	ns
	$t_{F(SDA)}$	Fall time, i2cX_sda	10	80		160	ns

(1) In i2cX, X is equal to 1, 2, or 3.
(2) The device provides (via the I²C bus) a hold time of at least 300 ns for the i2cx_sda signal (refer to the fall and rise time of i2cx_scl) to bridge the undefined region of the falling edge of i2cx_scl.
(3) HS-mode master devices generate a serial clock signal with a high to low ratio of 1 to 2. $t_{w(SCLL)} > 2\ t_{w(SCLH)}$.
(4) After this time, the first clock is generated.

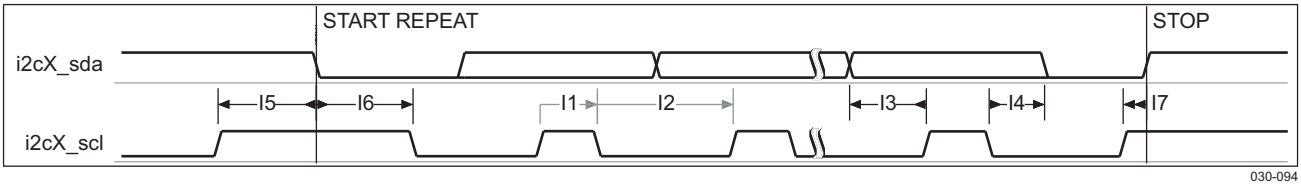

Figure 6-63. I²C High-Speed ModeStep 1Step 2Step 3

(1) HS-mode master devices generate a serial clock signal with a high-to-low ratio of 1 to 2. $t_{w(SCLL)} > 2 \times t_{w(SCLH)}$.
(2) In i2cX, X is equal to 1, 2, or 3.
(3) After this time, the first clock is generated.

Table 6-108. Correspondence Standard vs. TI Timing References

	TI-AM35x	STANDARD-I²C	
		S/F Mode	HS Mode
	f_{SCL}	F_{SCL}	F_{SCLH}
I1	$t_{w(SCLH)}$	T_{HIGH}	T_{HIGH}
I2	$t_{w(SCLL)}$	T_{LOW}	T_{LOW}
I3	$t_{su(SDAV-SCLH)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I4	$t_{h(SCLH-SDAV)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I5	$t_{su(SDAL-SCLH)}$	$T_{SU;STA}$	$T_{SU;STA}$
I6	$t_{h(SCLH-SDAH)}$	$T_{HD;STA}$	$T_{HD;STA}$

Table 6-108. Correspondence Standard vs. TI Timing References (continued)

	TI-AM35x	STANDARD-I²C	
		S/F Mode	HS Mode
I7	$t_{h(SCLH-RSTART)}$	$T_{SU;STO}$	$T_{SU;STO}$
I8	$t_{w(SDAH)}$	T_{BUF}	

6.7 Removable Media Interfaces

6.7.1 High-Speed Multimedia Memory Card (MMC) and Secure Digital IO Card (SDIO) Timing

The MMC/SDIO host controller provides an interface to high-speed and standard MMC, SD memory cards, or SDIO cards. The application interface is responsible for managing transaction semantics. The MMC/SDIO host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit, and checking for syntactical correctness.

There are three MMC interfaces on the AM3517/05:

- MMC/SD/SDIO Interface 1:
  - 1.8-V/3.3-V support
  - 8 bits
- MMC/SD/SDIO Interface 2:
  - 1.8-V/3.3-V support
  - 8 bits
  - 4 bits with external transceiver allowing to support 1.8-V/3.3-V peripherals in 1.8-V mode operation. Transceiver direction control signals are multiplexed with the upper four data bits.
- MMC/SD/SDIO Interface 3:
  - 1.8-V/3.3-V support
  - 8 bits

6.7.1.1 MMC/SD/SDIO in SD Identification Mode

Table 6-110 and Table 6-111 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-109. MMC/SD/SDIO Timing Conditions SD Identification Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
SD Identification Mode				
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance		TBD	pF

Table 6-110. MMC/SD/SDIO Timing Requirements SD Identification Mode(1)(2)(3)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
SD Identification Mode					
MMC/SD/SDIO Interface 1					
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	TBD		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	TBD		ns
MMC/SD/SDIO Interface 2					
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	TBD		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	TBD		ns

(1) Timing parameters are referred to output clock specified in Table 6-111.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-111.
(3) Corresponding figures showing timing parameters are common with other interface modes. (See SD and HS SD modes).

Table 6-110. MMC/SD/SDIO Timing Requirements SD Identification Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
MMC/SD/SDIO Interface 3					
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	TBD		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	TBD		ns

Table 6-111. MMC/SD/SDIO Switching Characteristics SD Identification Mode(1)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
SD Identification Mode					
HSSD1/SD1	$t_{c(clk)}$	Cycle time(2), output clk period	TBD		ns
HSSD2/SD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		ns
HSSD2/SD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD	ns
	$t_{j(clk)}$	Jitter standard deviation(3), output clk		TBD	ps
MMC/SD/SDIO Interface 1					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	ns
MMC/SD/SDIO Interface 2					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	TBD	TBD	ns
MMC/SD/SDIO Interface 3					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	TBD	TBD	ns

(1) Corresponding figures showing timing parameters are common with other interface modes (see SD and HS SD modes).
(2) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(3) The jitter probability density can be approximated by a Gaussian function.

Table 6-112. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-113. Y Parameter

CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

6.7.1.2 MMC/SD/SDIO in High-Speed MMC Mode

Table 6-115 and Table 6-116 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-64 and Figure 6-65).

Table 6-114. MMC/SD/SDIO Timing Conditions High-Speed MMC Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
High-Speed MMC Mode				
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance	TBD		pF

Table 6-115. MMC/SD/SDIO Timing Requirements High-Speed MMC Mode(1)(2)(3)(4)

NO.	PARAMETER		1.8 V, 3.3V		UNIT
			MIN	MAX	
High-Speed MMC Mode					
MMC/SD/SDIO Interface 1					
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		TBD	ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		TBD	ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge		TBD	ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge		TBD	ns
MMC/SD/SDIO Interface 2					
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge		TBD	ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge		TBD	ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge		TBD	ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge		TBD	ns
MMC/SD/SDIO Interface 3					
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge		TBD	ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge		TBD	ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge		TBD	ns

(1) Timing parameters are referred to output clock specified in Table 6-116.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-116.
(3) Corresponding figures showing timing parameters are common with Standard MMC mode (See Figure 6-64 and Figure 6-65)
(4) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

Table 6-115. MMC/SD/SDIO Timing Requirements High-Speed MMC Mode (continued)

NO.	PARAMETER		1.8 V, 3.3V		UNIT
			MIN	MAX	
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge		TBD	ns

Table 6-116. MMC/SD/SDIO Switching Characteristics High-Speed MMC Mode(1)

N O.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
High-Speed MMC Mode					
MMC1	$t_{c(clk)}$	Cycle time(2), output clk period	TBD		ns
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		ns
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output clk		TBD	ps
MMC/SD/SDIO Interface 1					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 2					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 3					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	TBD	TBD	ns

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.
(2) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(3) The jitter probability density can be approximated by a Gaussian function.

Table 6-117. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-118. Y Parameter

CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the TBD.

6.7.1.3 MMC/SD/SDIO in Standard MMC Mode and MMC Identification Mode

Table 6-120 and Table 6-121 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-119. MMC/SD/SDIO Timing Conditions Standard MMC Mode and MMC Identification Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Standard MMC Mode and MMC Identification Mode			
Input Conditions			
t_R	Input signal rise time	TBD	ns
t_F	Input signal fall time	TBD	ns
Output Conditions			
C_{LOAD}	Output load capacitance	TBD	pF

Table 6-120. MMC/SD/SDIO Timing Requirements Standard MMC Mode and MMC Identification Mode(1)(2)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
Standard MMC Mode and MMC Identification Mode							
MMC/SD/SDIO Interface 1							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	TBD		TBD		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	TBD		TBD		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	TBD		TBD		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	TBD		TBD		ns
MMC/SD/SDIO Interface 2							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	TBD		TBD		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	TBD		TBD		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	TBD		TBD		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	TBD		TBD		ns
MMC/SD/SDIO Interface 3							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	TBD		TBD		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	TBD		TBD		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	TBD		TBD		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	TBD		TBD		ns

(1) Timing parameters are referred to output clock specified in Table 6-121.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-121.

Table 6-121. MMC/SD/SDIO Switching Characteristics Standard MMC Mode and MMC Identification Mode

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
MMC Identification Mode							
MMC1	$t_{c(clk)}$	Cycle time(1), output clk period	TBD		TBD		ns
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		TBD		ns
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD		TBD	ns
	$t_{j(clk)}$	Jitter standard deviation(2), output clk		TBD		TBD	ps
Standard MMC Mode							
MMC1	$t_{c(clk)}$	Cycle time(1), output clk period	TBD		TBD		ns
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		TBD		ns
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD		TBD	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output clk		TBD		TBD	ps
MMC/SD/SDIO Interface 1							
	$t_{c(clk)}$	Rise time, output clk		TBD		TBD	ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) The jitter probability density can be approximated by a Gaussian function.

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Table 6-121. MMC/SD/SDIO Switching Characteristics Standard MMC Mode and MMC Identification Mode (continued)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
	$t_{W(clkH)}$	Fall time, output clk		TBD		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	TBD	TBD	TBD	TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	TBD	TBD	TBD	TBD	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		TBD		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	TBD	TBD	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	TBD	TBD	TBD	TBD	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		TBD		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD		TBD	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	TBD	TBD	TBD	TBD	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	TBD	TBD	TBD	TBD	ns

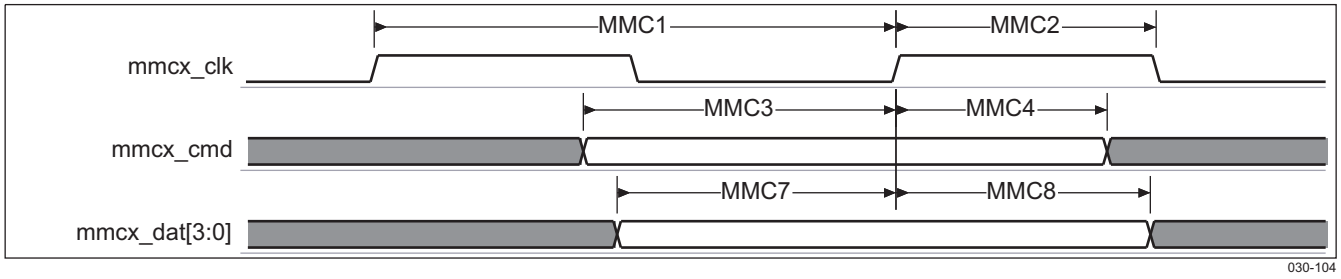
Table 6-122. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-123. Y Parameter

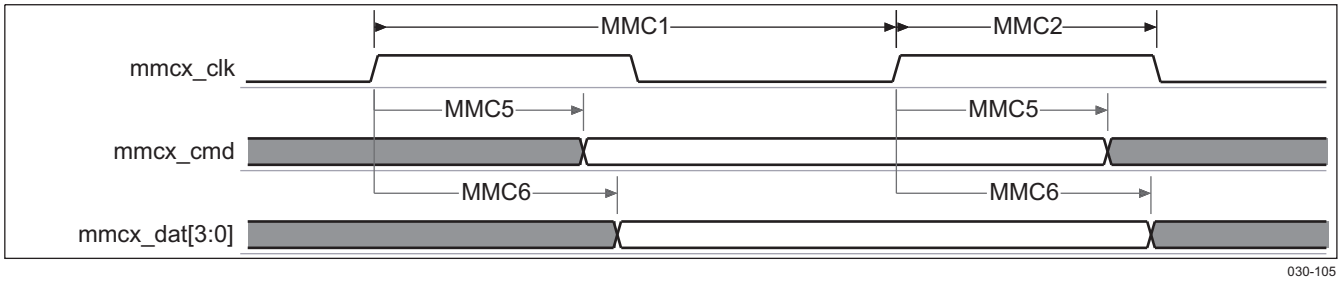
CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the TBD.



In mmcx, x is equal to 1, 2, or 3.

Figure 6-64. MMC/SD/SDIO High-Speed and Standard MMC Modes Data/Command Receive



In mmcx, x is equal to 1, 2, or 3.

Figure 6-65. MMC/SD/SDIO High-Speed and Standard MMC Modes Data/Command Transmit

6.7.1.4 MMC/SD/SDIO in High-Speed SD Mode

Table 6-125 and Table 6-126 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-124. MMC/SD/SDIO Timing Conditions High-Speed SD Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
High-Speed SD Mode				
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance	TBD		pF

Table 6-125. MMC/SD/SDIO Timing Requirements High-Speed SD Mode(1)(2)(3)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
High-Speed SD Mode					
MMC/SD/SDIO Interface 1					
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	TBD		ns

(1) Timing Parameters are referred to output clock specified in Table 6-126.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-126.
(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

Table 6-125. MMC/SD/SDIO Timing Requirements High-Speed SD Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	TBD		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	TBD		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	TBD		ns
MMC/SD/SDIO Interface 2					
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	TBD		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	TBD		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	TBD		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	TBD		ns
MMC/SD/SDIO Interface 3					
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	TBD		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	TBD		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	TBD		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	TBD		ns

Table 6-126. MMC/SD/SDIO Switching Characteristics High-Speed SD Mode

NO.	PARAMETER		1.8 V, 3.3 V		UNIT
			MIN	MAX	
High-Speed SD Mode					
HSSD1	$t_{c(clk)}$	Cycle time(1), output clk period	TBD		ns
HSSD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		ns
HSSD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output clk		TBD	ps
MMC/SD/SDIO Interface 1					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 2					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) The jitter probability density can be approximated by a Gaussian function.

Table 6-126. MMC/SD/SDIO Switching Characteristics High-Speed SD Mode (continued)

NO.	PARAMETER		1.8 V, 3.3 V		UNIT
			MIN	MAX	
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	TBD	TBD	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 3					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	TBD	TBD	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	TBD	TBD	ns

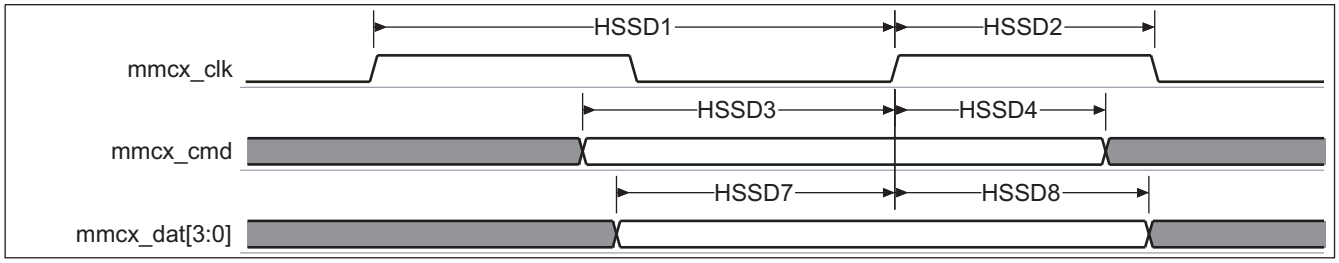
Table 6-127. X Parameters

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-128. Y Parameters

CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the TBD.



In mmcx, x is equal to 1, 2, or 3.

Figure 6-66. MMC/SD/SDIO High-Speed SD Mode Data/Command Receive

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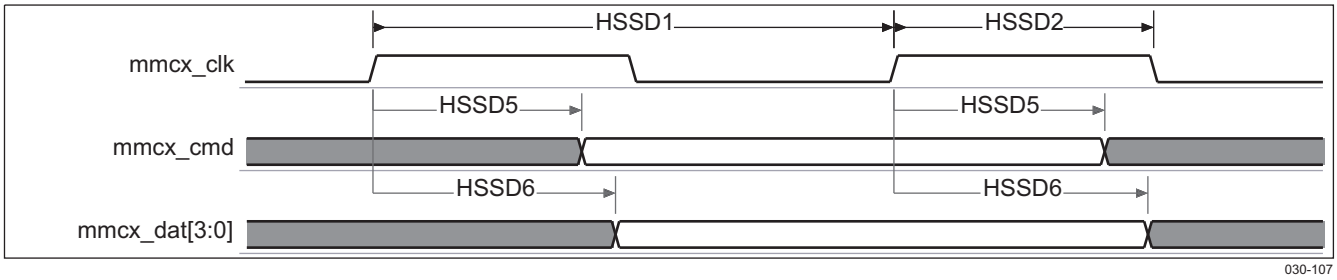

In mmcx, x is equal to 1, 2, or 3.

Figure 6-67. MMC/SD/SDIO High-Speed SD Mode Data/Command Transmit

6.7.1.5 MMC/SD/SDIO in Standard SD Mode

Table 6-130 and Table 6-131 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-68).

Table 6-129. MMC/SD/SDIO Timing Conditions Standard SD Mode

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
Standard SD Mode				
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance	TBD		pF

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Table 6-130. MMC/SD/SDIO Timing Requirements Standard SD Mode(1)(2)(3)

NO.	PARAMETER		1.8 V, 3.3V		UNIT
			MIN	MAX	
Standard SD Mode					
MMC/SD/SDIO Interface 1					
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	TBD		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	TBD		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	TBD		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	TBD		ns
MMC/SD/SDIO Interface 2					
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	TBD		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	TBD		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	TBD		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	TBD		ns
MMC/SD/SDIO Interface 3					
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	TBD		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	TBD		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	TBD		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	TBD		ns

(1) Timing parameters are referred to output clock specified in Table 6-131.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-131.
(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

Table 6-131. MMC/SD/SDIO Switching Characteristics Standard SD Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
Standard SD Mode					
SD1	$t_{c(clk)}$	Cycle time(1), output clk period	TBD		ns
SD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	TBD		ns
SD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	TBD		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		TBD	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output clk		TBD	ps
MMC/SD/SDIO Interface 1					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	TBD	TBD	ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) The jitter probability density can be approximated by a Gaussian function.

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Table 6-131. MMC/SD/SDIO Switching Characteristics Standard SD Mode (continued)

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 2					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	TBD	TBD	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	TBD	TBD	ns
MMC/SD/SDIO Interface 3					
	$t_{c(clk)}$	Rise time, output clk		TBD	ns
	$t_{W(clkH)}$	Fall time, output clk		TBD	ns
	$t_{W(clkL)}$	Rise time, output data		TBD	ns
	$t_{dc(clk)}$	Fall time, output data		TBD	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	TBD	TBD	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	TBD	TBD	ns

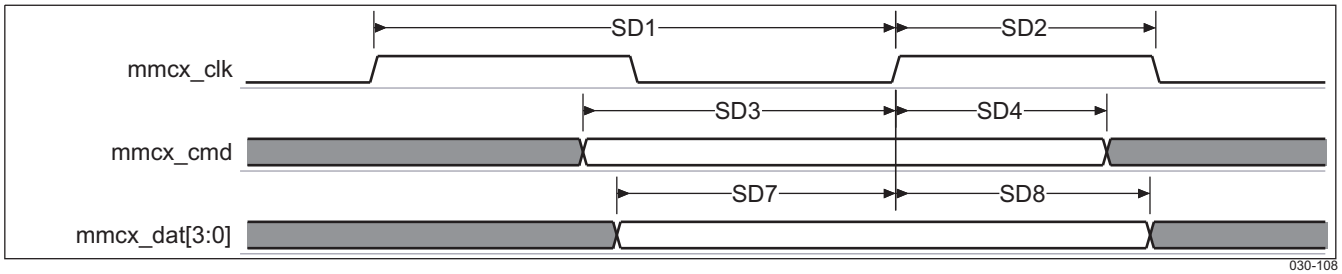
Table 6-132. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-133. Y Parameter

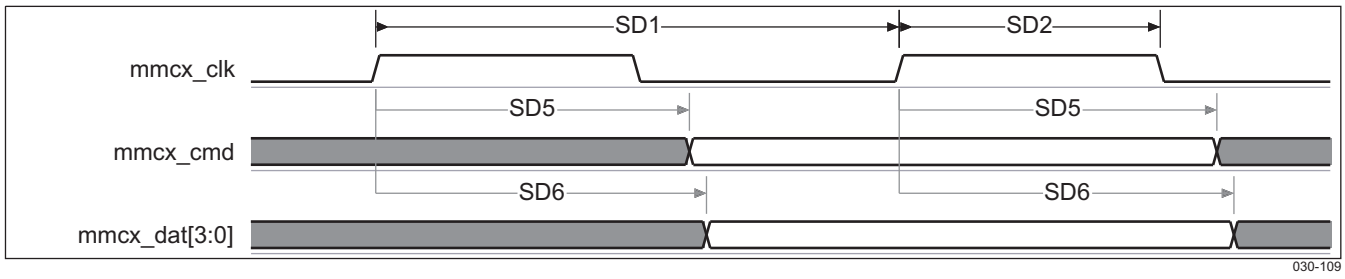
CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the TBD.



In mmcx, x is equal to 1, 2, or 3.

Figure 6-68. MMC/SD/SDIO Standard SD Mode Data/Command Receive



In mmcx, x is equal to 1, 2, or 3.

Figure 6-69. MMC/SD/SDIO Standard SD Mode Data/Command Transmit

6.8 Test Interfaces

The emulation and trace interfaces allow tracing activities of the following CPUs:

- ARM1136JF-STM through an Embedded Trace Macro-cell (ETM11) dedicated to enable real-time trace of the ARM subsystem operations and a Serial Debug Trace Interface (SDTI)

All processors can be emulated via JTAG ports.

6.8.1 Embedded Trace Macro Interface (ETM)

Table 6-134 assumes testing over the recommended operating conditions (see Figure 6-70).

Table 6-134. Embedded Trace Macro Interface Switching Characteristics(1)

NO.	PARAMETER		MIN	MAX	UNIT
f	$1/t_{c(CLK)}$	Frequency, etk_clk		TBD	MHz
ETM0	$t_{c(CLK)}$	Cycle time(2), etk_clk	TBD		ns
ETM1	$t_{W(CLK)}$	Clock pulse width, etk_clk	TBD		ns
ETM2	$t_{d(CLK-CTL)}$	Delay time, etk_clk clock edge to etk_ctl transition	TBD	TBD	ns
ETM3	$t_{d(CLK-D)}$	Delay time, etk_clk clock high to etk_d[15:0] transition	TBD	TBD	ns

(1) The capacitive load is equivalent to 25 pF.
(2) Cycle time is given by considering a jitter of 5%.

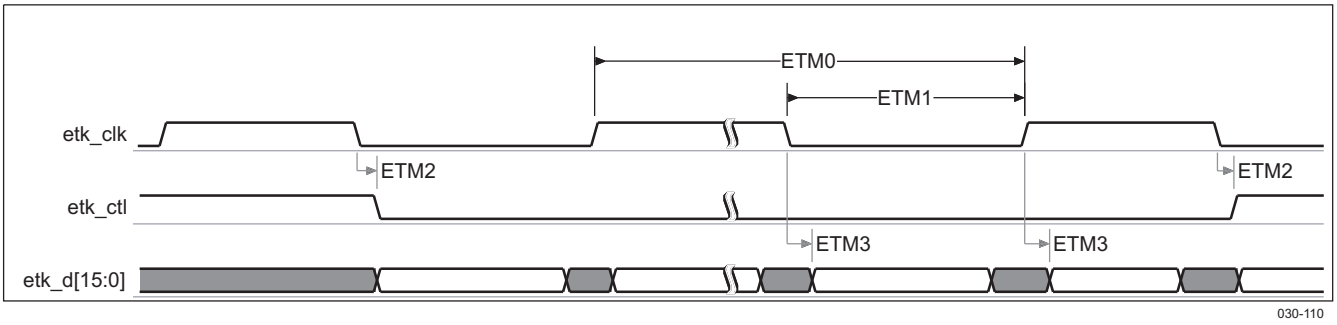


Figure 6-70. Embedded Trace Macro Interface

6.8.2 System Debug Trace Interface (SDTI)

The system debug trace interface (SDTI) module provides real-time software tracing functionality to the AM3517/05 device.

The trace interface has four trace data pins and a trace clock pin.

This interface is a dual-edge interface: the data are available on rising and falling edges of sdti_clk but can be also configured in single edge mode where data are available on falling edge of sdti_clk.

Serial interface operates in clock stop regime: serial clock is not free running, when there is no trace data there is no trace clock.

6.8.2.1 System Debug Trace Interface in Dual-Edge Mode

Table 6-136 assumes testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-71).

Table 6-135. System Debug Trace Interface Timing Conditions – Dual-Edge Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	25	pF

Table 6-136. System Debug Trace Interface Switching Characteristics – Dual-Edge Mode

NO.	PARAMETER			1.15 V		UNIT
				MIN	MAX	
SD1	$t_{c(CLK)}$	Cycle time, sdti_clk period		29		ns
SD2	$t_{w(CLK)}$	Typical pulse duration, sdti_clk high or low		0.5*P (1)		ns
	$t_{dc(CLK)}$	Duty cycle error, sdti_clk		–1.2	1.2	ns
	$t_{R(CLK)}$	Rise time, sdti_clk			5	ns
	$t_{F(CLK)}$	Fall time, sdti_clk			5	ns
SD3	$t_{d(CLK-TxD)}$	Delay time, sdti_clk transition to sdti_txd[3:0] transition	Multiplexing mode on etk pins	2.3	10.9	ns
			Multiplexing mode on jtag_emu pins	2.3	13.9	
	$t_{R(CLK)}$	Rise time, sdti_txd[3:0]			5	ns
	$t_{F(CLK)}$	Fall time, sdti_txd[3:0]			5	ns

(1) P = sdti_clk clock period

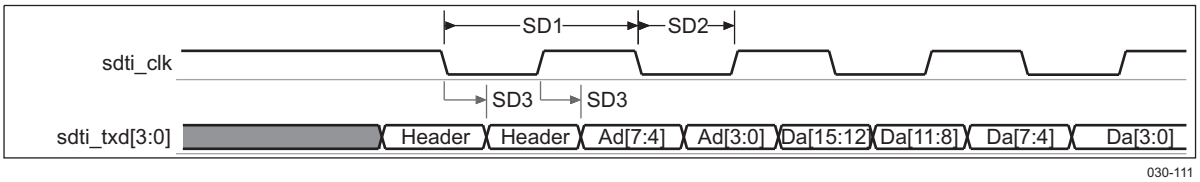


Figure 6-71. System Debug Trace Interface – Dual-Edge Mode

6.8.2.2 System Debug Trace Interface in Single-Edge Mode

Table 6-138 assumes testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-72).

Table 6-137. System Debug Trace Interface Timing Conditions – Single-Edge Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	25	pF

Table 6-138. System Debug Trace Interface Switching Characteristics – Single-Edge Mode

NO.	PARAMETER			1.15 V		UNIT
				MIN	MAX	
SD1	$t_{c(CLK)}$	Cycle time, sdti_clk period		29		ns
SD2	$t_{w(CLK)}$	Typical pulse duration, sdti_clk high or low		0.5*P (1)		ns
	$t_{dc(CLK)}$	Duty cycle error, sdti_clk		–1.2	1.2	ns
	$t_{R(CLK)}$	Rise time, sdti_clk			5	ns
	$t_{F(CLK)}$	Fall time, sdti_clk			5	ns
SD3	$t_{d(CLK-TxD)}$	Delay time, sdti_clk transition to sdti_txd[3:0] transition	Multiplexing mode on etk pins	2.3	26.5	ns
			Multiplexing mode on jtag_emu pins	2.3	33.2	
	$t_{R(CLK)}$	Rise time, sdti_txd[3:0]			5	ns
	$t_{F(CLK)}$	Fall time, sdti_txd[3:0]			5	ns

(1) P = sdti_clk clock period.

PRODUCT PREVIEW

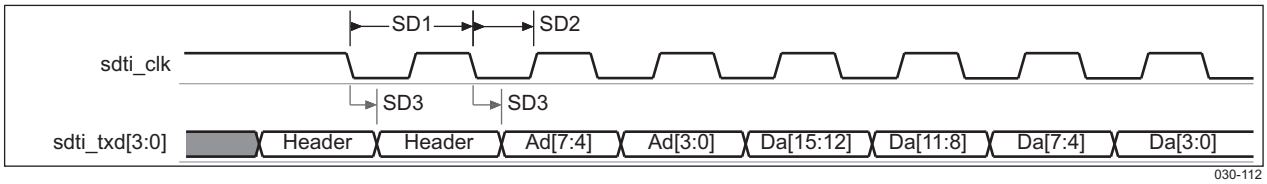


Figure 6-72. System Debug Trace Interface – Single-Edge Mode

6.8.3 JTAG Interfaces

AM3517/05 JTAG TAP controller handles standard IEEE JTAG interfaces. The following sections define the timing requirements for several tools used to test the AM3517/05 processors as:

- Free running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView ICE tool and Lauterbach tool

6.8.3.1 JTAG Free Running Clock Mode

Table 6-140 and Table 6-141 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-73).

Table 6-139. JTAG Timing Conditions Free Running Clock Mode

TIMING CONDITION PARAMETER		1.8 V	3.3 V	
		MAX	MAX	UNIT
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance	TBD	TBD	pF

Table 6-140. JTAG Timing Requirements Free Running Clock Mode(1)

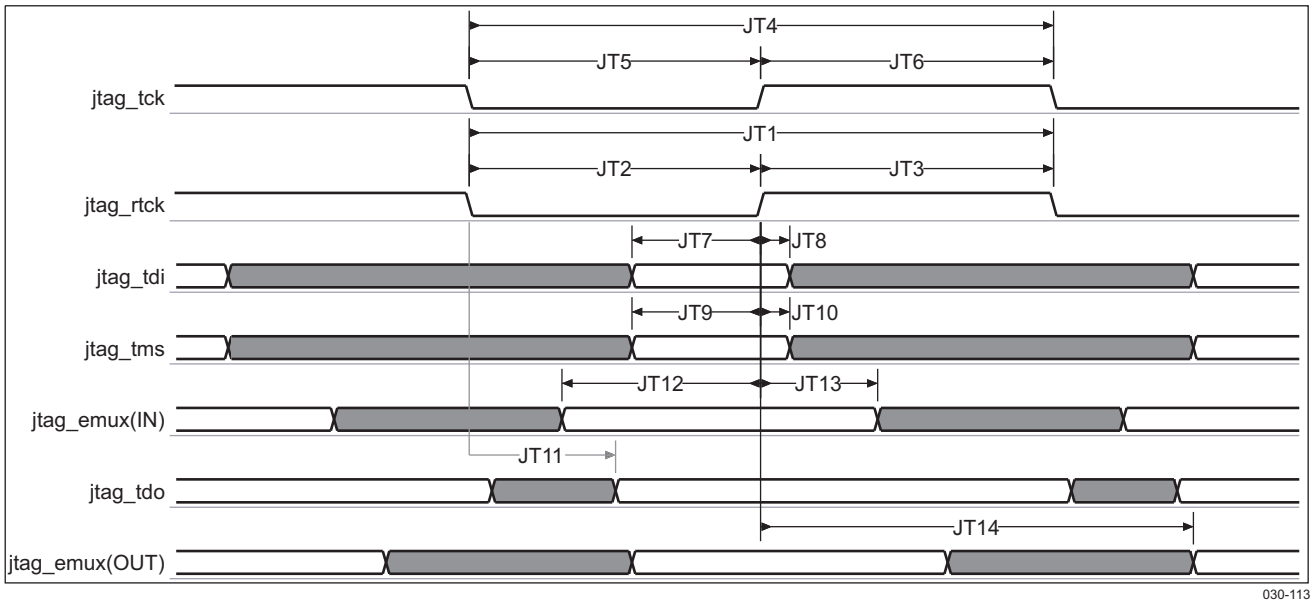
NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
JT4	$t_{c(tck)}$	Cycle time(2), jtag_tck period					ns
JT5	$t_{w(tckL)}$	Typical pulse duration, jtag_tck low	TBD		TBD		ns
JT6	$t_{w(tckH)}$	Typical pulse duration, jtag_tck high	TBD		TBD		ns
	$t_{dc(tck)}$	Duty cycle error, jtag_tck	TBD	TBD	TBD	TBD	ps
	$t_{j(tck)}$	Cycle jitter(3), jtag_tck	TBD	TBD	TBD	TBD	ps
JT7	$t_{su(tdiV-rtckH)}$	Setup time, jtag_tdi valid before jtag_rtck high	TBD		TBD		ns
JT8	$t_{h(tdiV-rtckH)}$	Hold time, jtag_tdi valid after jtag_rtck high	TBD		TBD		ns
JT9	$t_{su(tmsV-rtckH)}$	Setup time, jtag_tms valid before jtag_rtck high	TBD		TBD		ns
JT10	$t_{h(tmsV-rtckH)}$	Hold time, jtag_tms valid after jtag_rtck high	TBD		TBD		ns
JT12	$t_{su(emuxV-rtckH)}$	Setup time, jtag_emux(4) valid before jtag_rtck high	TBD		TBD		ns
JT13	$t_{h(emuxV-rtckH)}$	Hold time,jtag_emux(4) valid after jtag_rtck high	TBD		TBD		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the JTAG module.
(3) Maximum cycle jitter supported by jtag _tck input clock.
(4) x = 0 to 1

Table 6-141. JTAG Switching Characteristics Free Running Clock Mode

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
JT1	$t_{c(rtck)}$	Cycle time(1), jtag_rtck period			TBD		ns
JT2	$t_{w(rtckL)}$	Typical pulse duration, jtag_rtck low	TBD		TBD		ns
JT3	$t_{w(rtckH)}$	Typical pulse duration, jtag_rtck high	TBD		TBD		ns
	$t_{dc(rtck)}$	Duty cycle error, jtag_rtck	TBD	TBD	TBD	TBD	ps
	$t_{j(rtck)}$	Jitter standard deviation(2), jtag_rtck		TBD		TBD	ps
	$t_{R(rtck)}$	Rise time, jtag_rtck		TBD		TBD	ns
	$t_{F(rtck)}$	Fall time, jtag_rtck		TBD		TBD	ns
JT11	$t_{d(rtckL-tdoV)}$	Delay time, jtag_rtck low to jtag_tdo valid	TBD	TBD	TBD	TBD	ns
	$t_{R(tdo)}$	Rise time, jtag_tdo		TBD		TBD	ns
	$t_{F(tdo)}$	Fall time, jtag_tdo		TBD		TBD	ns
JT14	$t_{d(rtckH-emuxV)}$	Delay time, jtag_rtck high to ,jtag_emux(3) valid	TBD	TBD	TBD	TBD	ns
	$t_{R(emux)}$	Rise time, jtag_emux(3)		TBD		TBD	ns
	$t_{F(emux)}$	Fall time, jtag_emux(3)		TBD		TBD	ns

(1) Related with the jtag_rtck maximum frequency.
(2) The jitter probability density can be approximated by a Gaussian function.
(3) x = 0 to 1



In jtag_emux, x is equal to 0 to 1.

Figure 6-73. JTAG Interface Timing Free Running Clock Mode

6.8.3.2 JTAG Adaptive Clock Mode

Table 6-143 and Table 6-144 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-74):

Table 6-142. JTAG Timing Conditions Adaptive Clock Mode

TIMING CONDITION PARAMETER		1.8 V	3.3 V	
		MAX		UNIT
Input Conditions				
t_R	Input signal rise time	TBD	TBD	ns

Table 6-142. JTAG Timing Conditions Adaptive Clock Mode (continued)

TIMING CONDITION PARAMETER		1.8 V	3.3 V	
		MAX		UNIT
t_F	Input signal fall time	TBD	TBD	ns
Output Conditions				
C_{LOAD}	Output load capacitance	TBD	TBD	pF

Table 6-143. JTAG Timing Requirements Adaptive Clock Mode(1)

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
JA4	$t_{c(tck)}$	Cycle time(2), jtag_tck period	TBD		TBD		ns
JA5	$t_{w(tckL)}$	Typical pulse duration, jtag_tck low	TBD		TBD		ns
JA6	$t_{w(tckH)}$	Typical pulse duration, jtag_tck high	TBD		TBD		ns
	$t_{dc(lclk)}$	Duty cycle error, jtag_tck	TBD	TBD	TBD	TBD	ps
	$t_{j(lclk)}$	Cycle jitter(3), jtag_tck	TBD	TBD	TBD	TBD	ps
JA7	$t_{su(tdiV-tckH)}$	Setup time, jtag_tdi valid before jtag_tck high	TBD		TBD		ns
JA8	$t_{h(tdiV-tckH)}$	Hold time, jtag_tdi valid after jtag_tck high	TBD		TBD		ns
JA9	$t_{su(tmsV-tckH)}$	Setup time, jtag_tms valid before jtag_tck high	TBD		TBD		ns
JA10	$t_{h(tmsV-tckH)}$	Hold time, jtag_tms valid after jtag_tck high	TBD		TBD		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the JTAG module.
(3) Maximum cycle jitter supported by jtag _tck input clock.

Table 6-144. JTAG Switching Characteristics Adaptive Clock Mode

NO.	PARAMETER		1.8 V		3.3 V		UNIT
			MIN	MAX	MIN	MAX	
JA1	$t_{c(rtck)}$	Cycle time(1), jtag_rtck period	TBD				ns
JA2	$t_{w(rtckL)}$	Typical pulse duration, jtag_rtck low	TBD		TBD		ns
JA3	$t_{w(rtckH)}$	Typical pulse duration, jtag_rtck high	TBD		TBD		ns
	$t_{dc(rtck)}$	Duty cycle error, jtag_rtck	TBD	TBD	TBD	TBD	ps
	$t_{j(rtck)}$	Jitter standard deviation(2), jtag_rtck		TBD		TBD	ps
	$t_{R(rtck)}$	Rise time, jtag_rtck		TBD		TBD	ns
	$t_{F(rtck)}$	Fall time, jtag_rtck		TBD		TBD	ns
JA11	$t_{d(rtckL-tdoV)}$	Delay time, jtag_rtck low to jtag_tdo valid	TBD	TBD	TBD	TBD	ns
	$t_{R(tdo)}$	Rise time, jtag_tdo,		TBD		TBD	ns
	$t_{F(tdo)}$	Fall time, jtag_tdo		TBD		TBD	ns

(1) Related with the jtag _rtck maximum frequency programmable.
(2) The jitter probability density can be approximated by a Gaussian function.

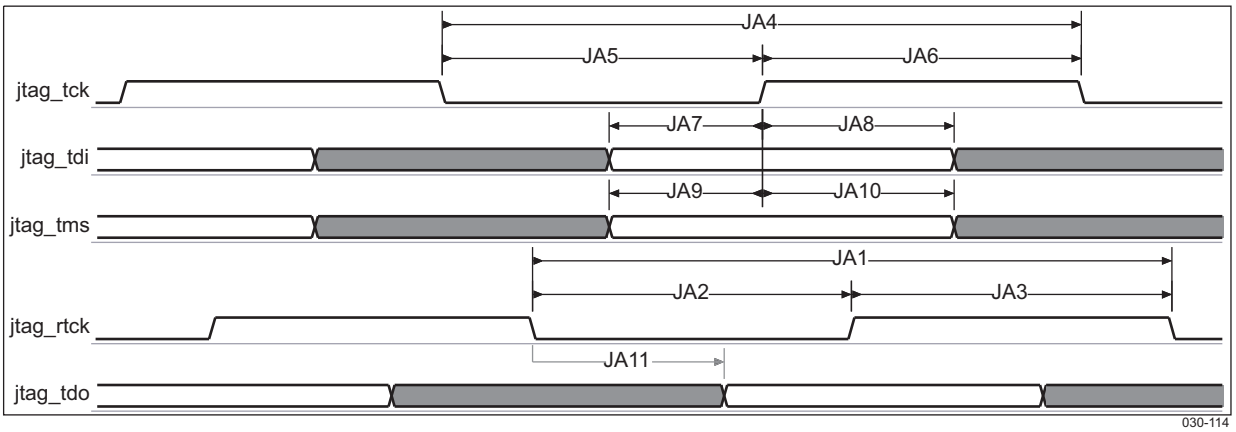


Figure 6-74. JTAG Interface Timing Adaptive Clock Mode

7 PACKAGE CHARACTERISTICS

7.1 Package Thermal Resistance

Table 7-1 provides the thermal resistance characteristics for the recommended package types used on the AM3517/05 Applications Processor.

Table 7-1. AM3517/05 Thermal Resistance Characteristics(1)

Package	Power (W)	R_{JA}(C/W)	R_{JB}(C/W)	R_{JC}(C/W)	Board Type
AM3517/05 (ZCN Pkg.)	TBD	TBD	10.1	TBD	2S2P

(1) R_{JA} (Theta-JA) = Thermal Resistance Junction-to-Ambient, C/W
R_{JB} (Theta-JB) = Thermal Resistance Junction-to-Board, C/W
R_{JC} (Theta-JC) = Thermal Resistance Junction-to-Case, C/W

PRODUCT PREVIEW

7.2 Device Support

7.2.1 Development Support

7.2.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all AM35x processors and support tools. Each device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final devices electrical specifications and may not use production assembly flow. (TMX definition)

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications. (TMP definition)

null Production version of the silicon die that is fully qualified. (TMS definition)

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

Developmental product is intended for internal evaluation purposes.

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TIs standard warranty applies.

Predictions show that prototype devices (X or P), have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For additional description of the device nomenclature markings, see the *AM35x Processor Silicon Errata* (literature number SPRZ306).

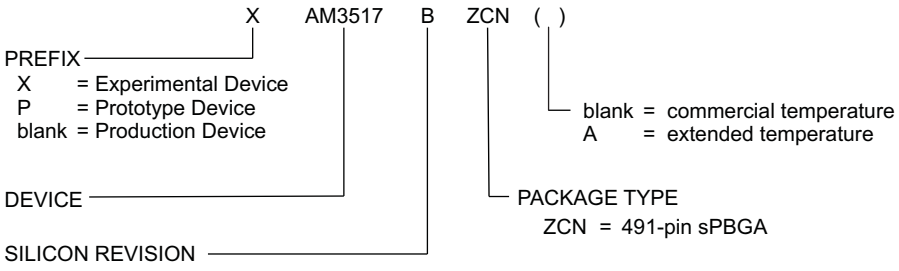


Figure 7-1. Device Nomenclature

7.2.3 Documentation Support

7.2.3.1 Related Documentation from Texas Instruments

The following documents describe the AM3517/05 ARM Microprocessor. Copies of these documents are available on the Internet at www.ti.com. Tip: Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the AM3517/05 ARM Microprocessor, related peripherals, and other technical collateral, is available in the product folder at: www.ti.com.

SPRUGR0 AM35x ARM Microprocessor Technical Reference Manual. Collection of documents providing detailed information on the Sitara™ architecture including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem as well a functional description of the peripherals supported on AM3517/05 devices is also included.

7.2.3.2 Related Documentation from Other Sources

The following documents are related to the AM3517/05 ARM Microprocessor. Copies of these documents can be obtained directly from the internet or from your Texas Instruments representative.

Cortex-A8 Technical Reference Manual. This is the technical reference manual for the Cortex-A8 processor. A copy of this document can be obtained via the internet at http://infocenter.arm.com. Please see the *AM3517/05 ARM Microprocessor Silicon Errata* (literature number SPRZ306) to determine the revision of the Cortex-A8 core used on your device.

ARM Core Cortex™-A8 (AT400/AT401) Errata Notice. Provides a list of advisories for the different revisions of the Cortex-A8 processor. Contact your TI representative for a copy of this document. Please see the *AM3517/05 ARM Microprocessor Silicon Errata* (literature number SPRZ306) to determine the revision of the Cortex-A8 core used on your device.

PACKAGING INFORMATION

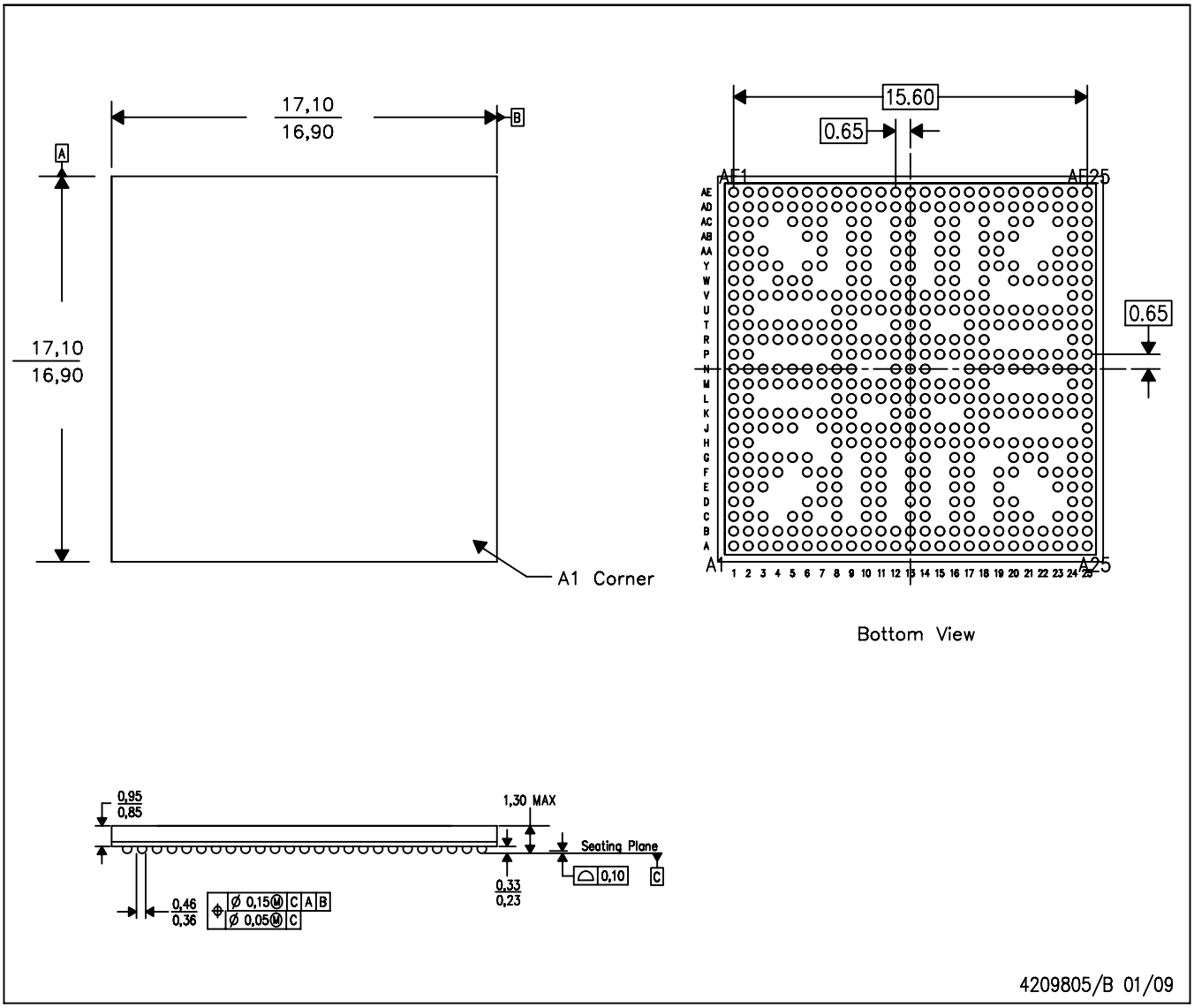
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
XAM3517ZCN	ACTIVE	NFBGA	ZCN	491	90	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZCN (S–PBGA–N491) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. nFBGA package configuration.
D. This is a Pb–free solder ball design.

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DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
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Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
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