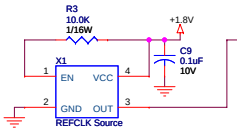
USB3320 Reference Schematic

REFCLK Source

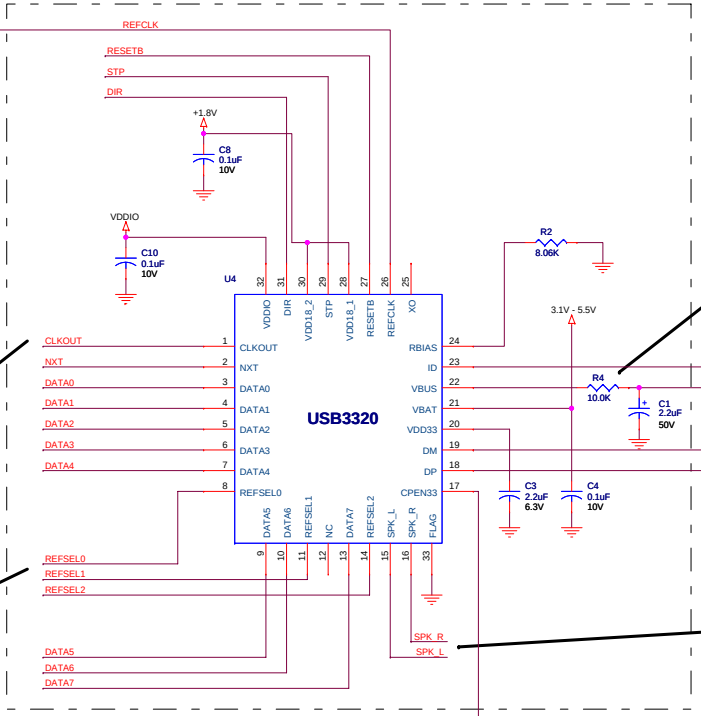
The USB3320 allows for a crystal to be used for the REFCLK source rather than a clock oscillator. For more information on using a crystal with the USB3320, please see section 5.4.1.2 of the USB3320 datasheet.



This portion of the schematic shows components needed for PHY to operate in a USB 2.0 High Speed Device application.

The CLKOUT signal of the USB3320 can be tied to VDDIO to configure the USB3320 for ULPI CLKIN mode. In this mode, the 60MHz ULPI clock is being driven by the link into the REFCLK pin of the USB3320. For more information on ULPI CLKIN mode, please see section 5.4.1.1 of the USB3320 datasheet.

REFSEL[2:0] should be tied to VDDIO or GND to select the REFCLK frequency. Refer to Table 5.10 in the USB3320 datasheet for the selector table. REFSEL[2:0] must all be tied to VDDIO for ULPI CLKIN mode.



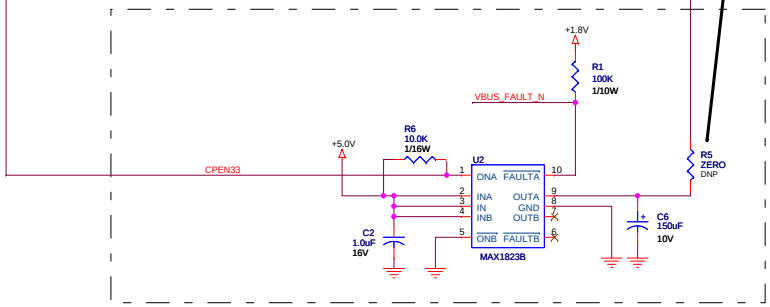
R4	
1K	OTG
10K	Device / Host

R4 must be sized appropriately. See data sheet for instructions on sizing the Rvbus resistor.

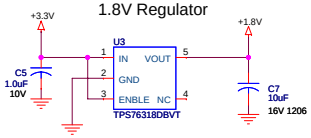
SPK_R and SPK_L are connected to the Integrated USB Switch.
Can be used for:
- UART or Serial Data
- Audio
- Full-Speed Legacy USB 1.1 Data
- Battery Charging

R5	
Zero Ohm	Host / OTG
DNP	Device

A VBUS Source is required for Host and OTG applications.



1.8V Regulator



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